

# Microprocesadores, Tema 6:

Módulos CCP (Capturar / Comparar / PWM)

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# Objetivos

Estudiar los diferentes modos de funcionamiento de los módulos CCP

CCP = Capture/Compare/PWM

Uso de los temporizadores asociados a los módulos CCP

Aplicaciones de los módulos CCP

# Módulos CCP, Características Generales

**Dos módulos: CCPx (x = 1, 2)**

**Registros asociados a cada módulo (lectura/escritura):**

- **CCPRx (CCPRxH:CCPRxL): Registro de datos de 16 bits**
  - En modo captura, CCPRx funciona como Registro de Captura
  - En modo compara, CCPRx funciona como Registro de Comparación
  - En modo PWM, CCPRx funciona determina el Duty Cycle
- **CCPxCON: Registro de control**

**Los módulos CCP hacen uso de los timers:**

CCP/ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

ECCP – Enhanced CCP module (modo PWM mejorado en dispositivos de 40/44 pines)

# Módulos CCP, Registro de Control y Modos

2 estandar (CCP1 y CCP2) en dispositivos de 28 pines. CCP1 mejorado en dispositivos de 40/48 pines (en modo PWM)

**REGISTER 15-1: CCPxCON REGISTER (CCP2 MODULE, CCP1 MODULE IN 28-PIN DEVICES)**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0	
bit 7								bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB1:DCxB0:** PWM Duty Cycle bit 1 and bit 0 for CCP Module x

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSBs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSBs (DCx9:DCx2) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM3:CCPxM0:** CCP Module x Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCP module)

0001 = Reserved

0010 = Compare mode, toggle output on match (CCPIF bit is set)

0011 = Reserved

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode: initialize CCP pin low; on compare match, force CCP pin high (CCPxIF bit is set)

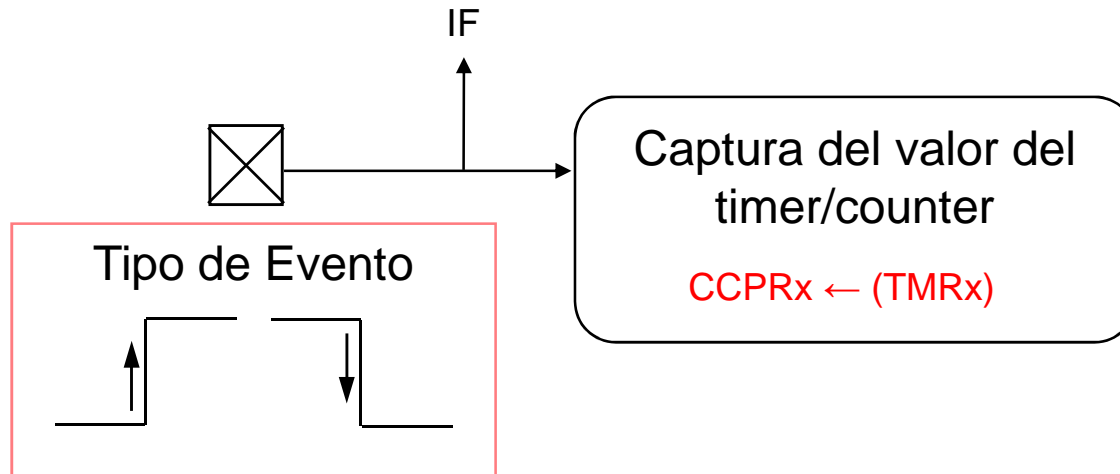
1001 = Compare mode: initialize CCP pin high; on compare match, force CCP pin low (CCPxIF bit is set)

1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCP pin reflects I/O state)

1011 = Compare mode: trigger special event, reset timer, start A/D conversion on CCP2 match (CCPxIF bit is set)

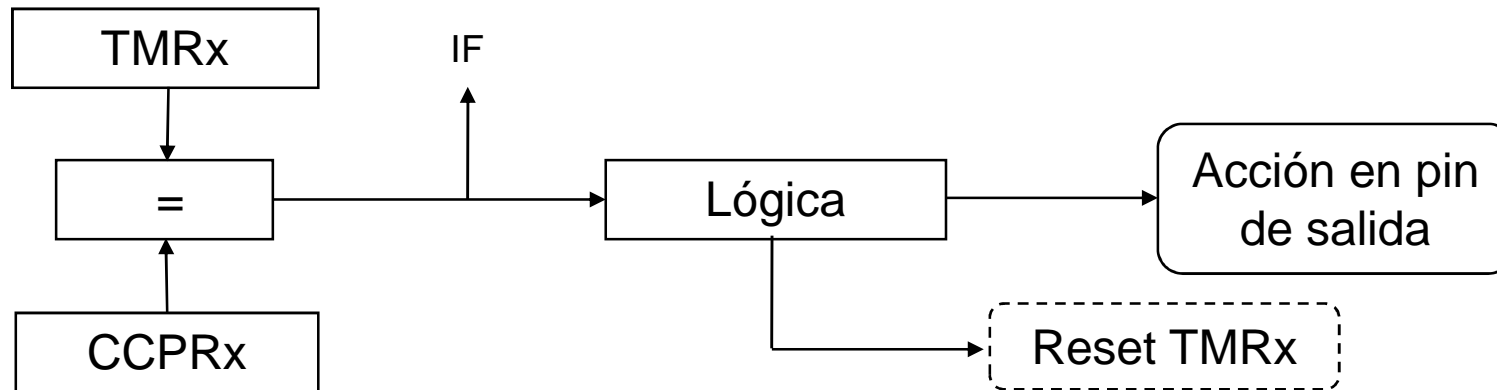
11xx = PWM mode

## Módulos CCP, Modo Captura



**Permite conocer el tiempo en el que ocurre un evento**  
(ej: medida del periodo (o frecuencia) de una señal)

## Módulos CCP, Modo Compare



**Permite generar señales controlando el tiempo**

(ej: retardo, trenes de pulsos)

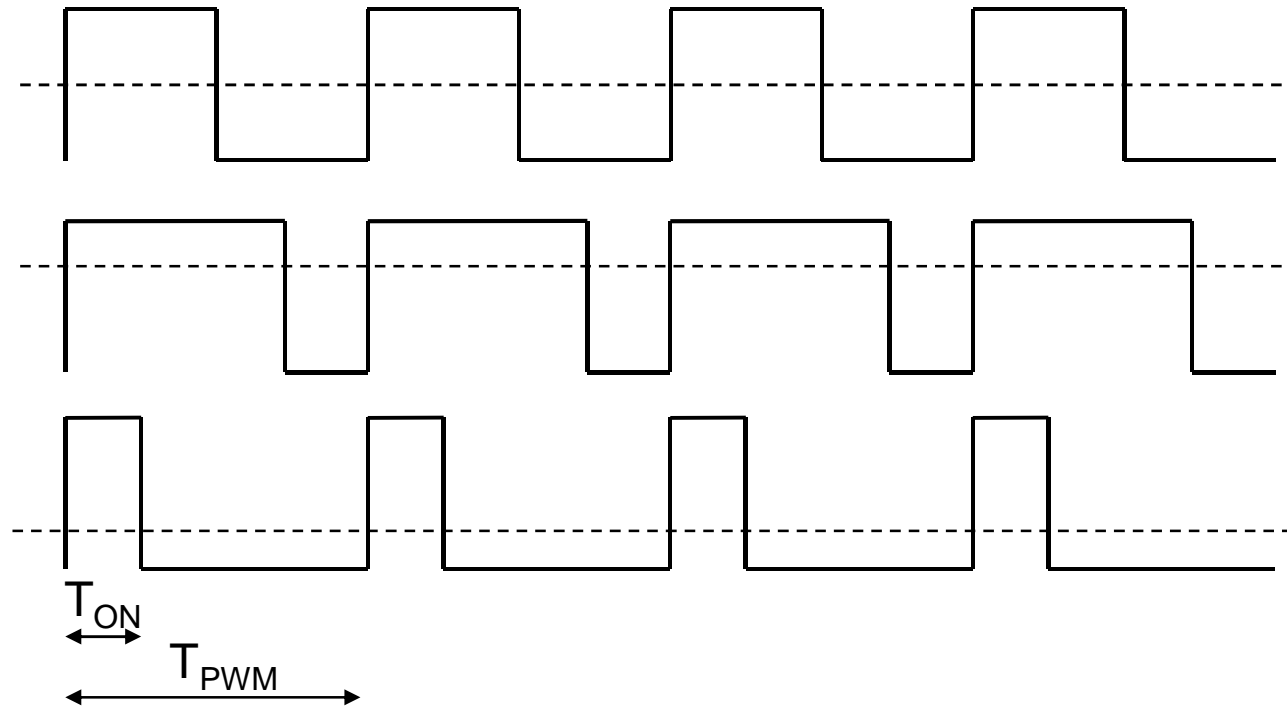
**Se puede utilizar este modo de dos formas:**

- 1.- Permitiendo activación Reset TMRx: intervalos de tiempo constantes
- 2.- Incrementando el registro CCPRx: intervalos de tiempo constantes o variables

## Módulos CCP, Modo PWM

Permite generar una señal PWM

PWM – Pulse Width Modulation (Modulación por ancho de pulso)



Periodo =  $T_{PWM}$ ; Frecuencia,  $F_{PWM} = 1 / T_{PWM}$

Ciclo de trabajo (Duty Cycle) =  $(T_{ON} / T_{PWM}) \times 100$

PWM resolución máxima =  $\log(F_{OSC} / F_{PWM}) / \log(2)$  bits

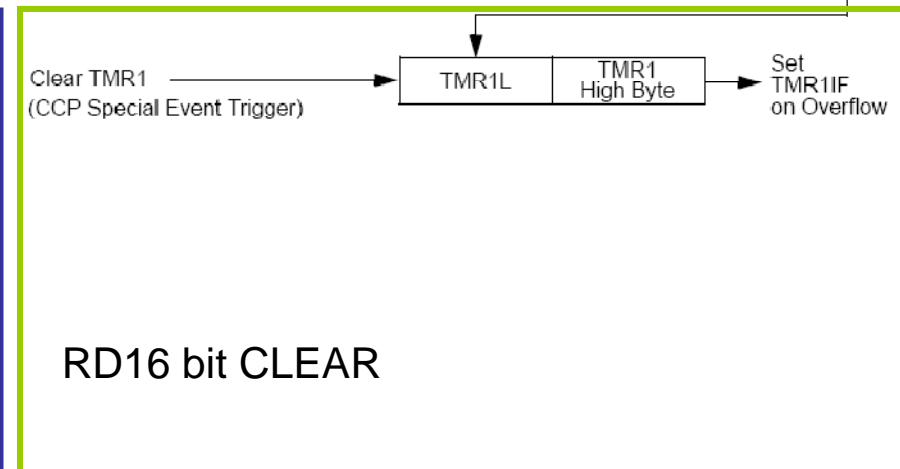
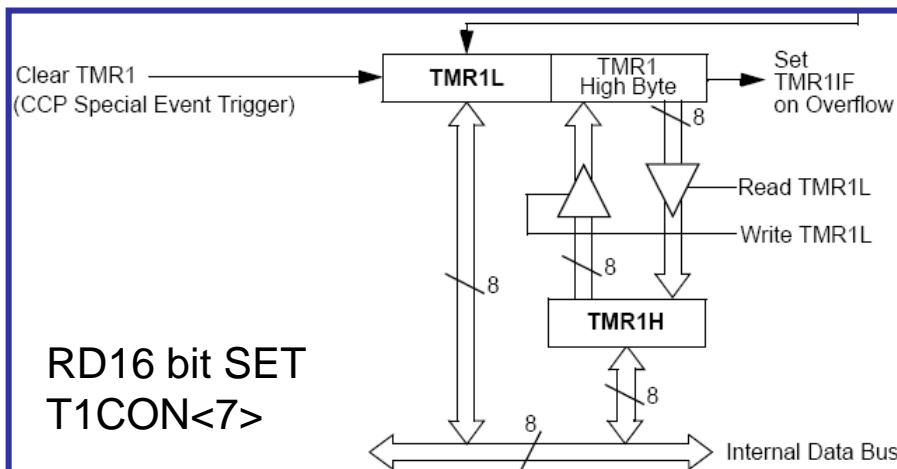
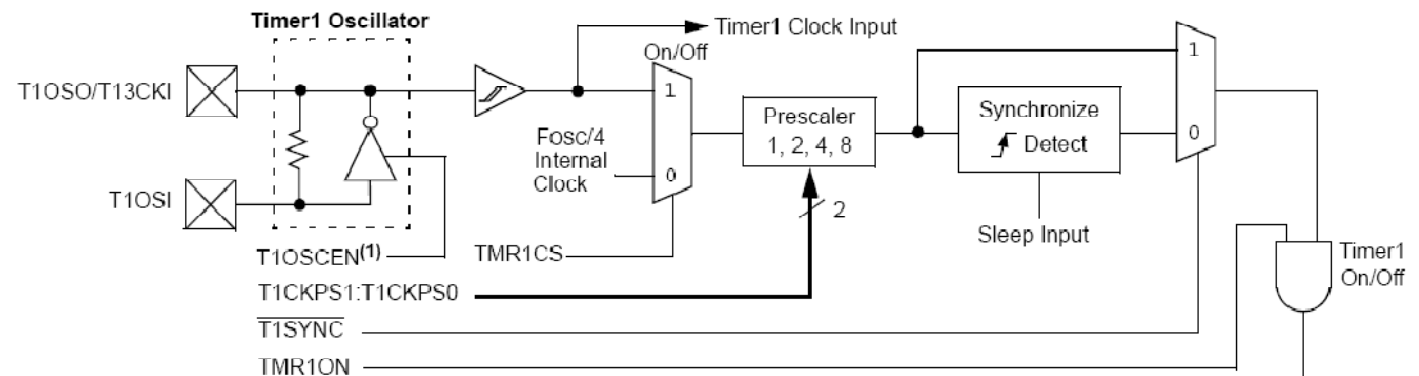
# Timers empleados por los módulos CCP en el PIC , Timer 1

## CARACTERISTICAS

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- Selectable clock source (internal or external) with device clock or TMR1 oscillator internal option
- Interrupt-on-overflow
- **Reset on CCP Special Event Trigger**
- Device clock status flag (T1RUN)

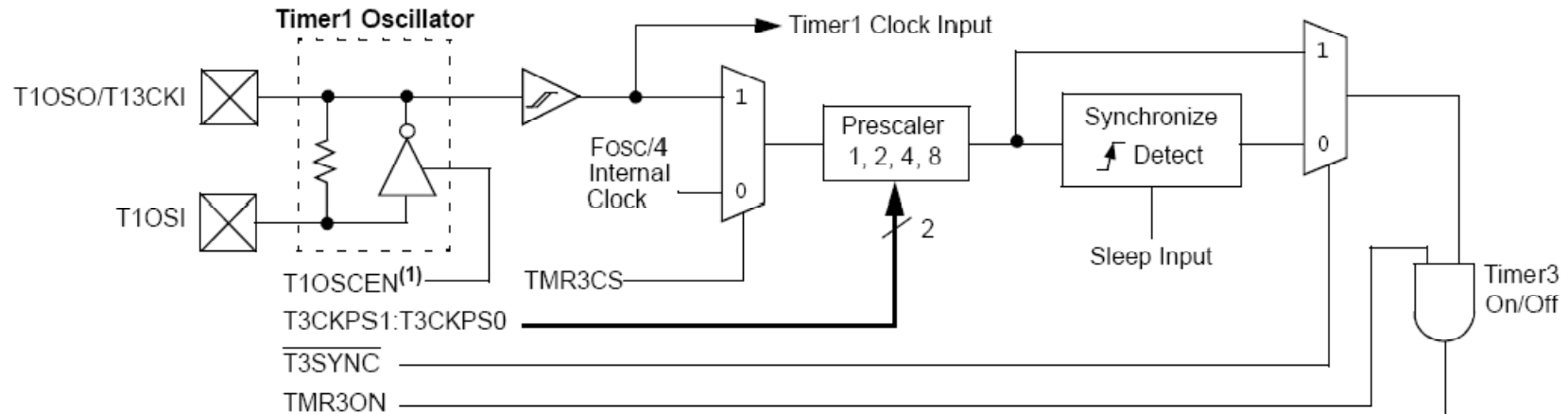
## ESQUEMA

(ver  
**T1CON**  
 en Data  
 Sheet)

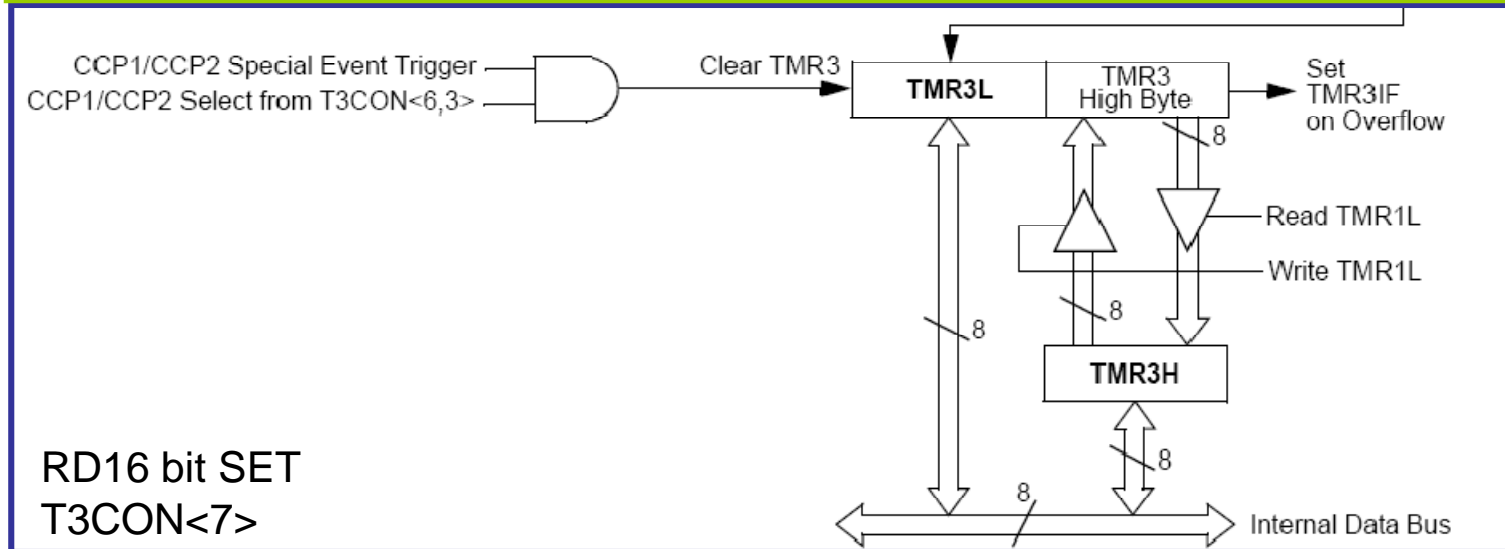




# Timers empleados por los módulos CCP en el PIC , Timer 3



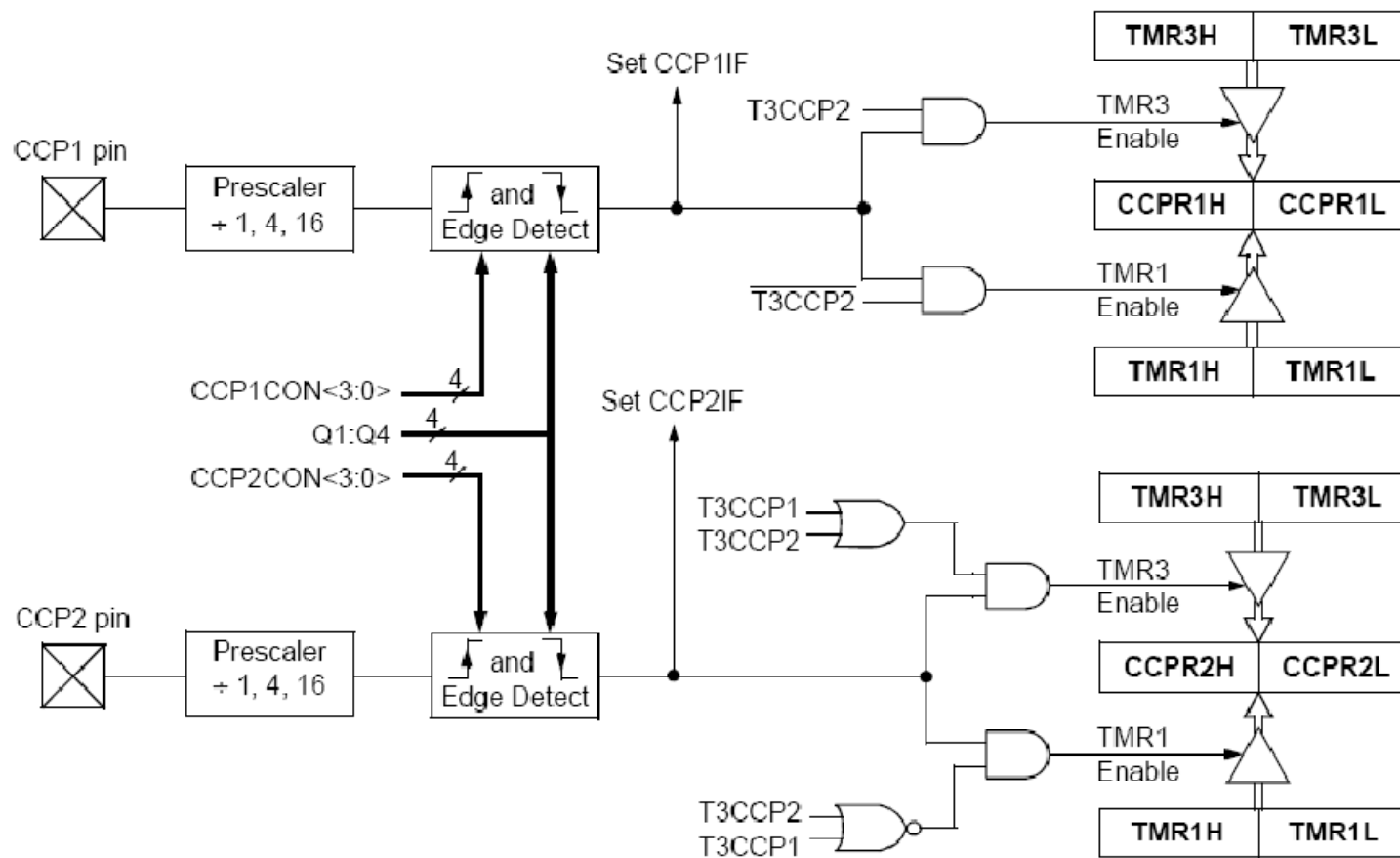
(ver  
**T3CON**  
en Data  
Sheet)



**RD16 bit SET**  
**T3CON<7>**

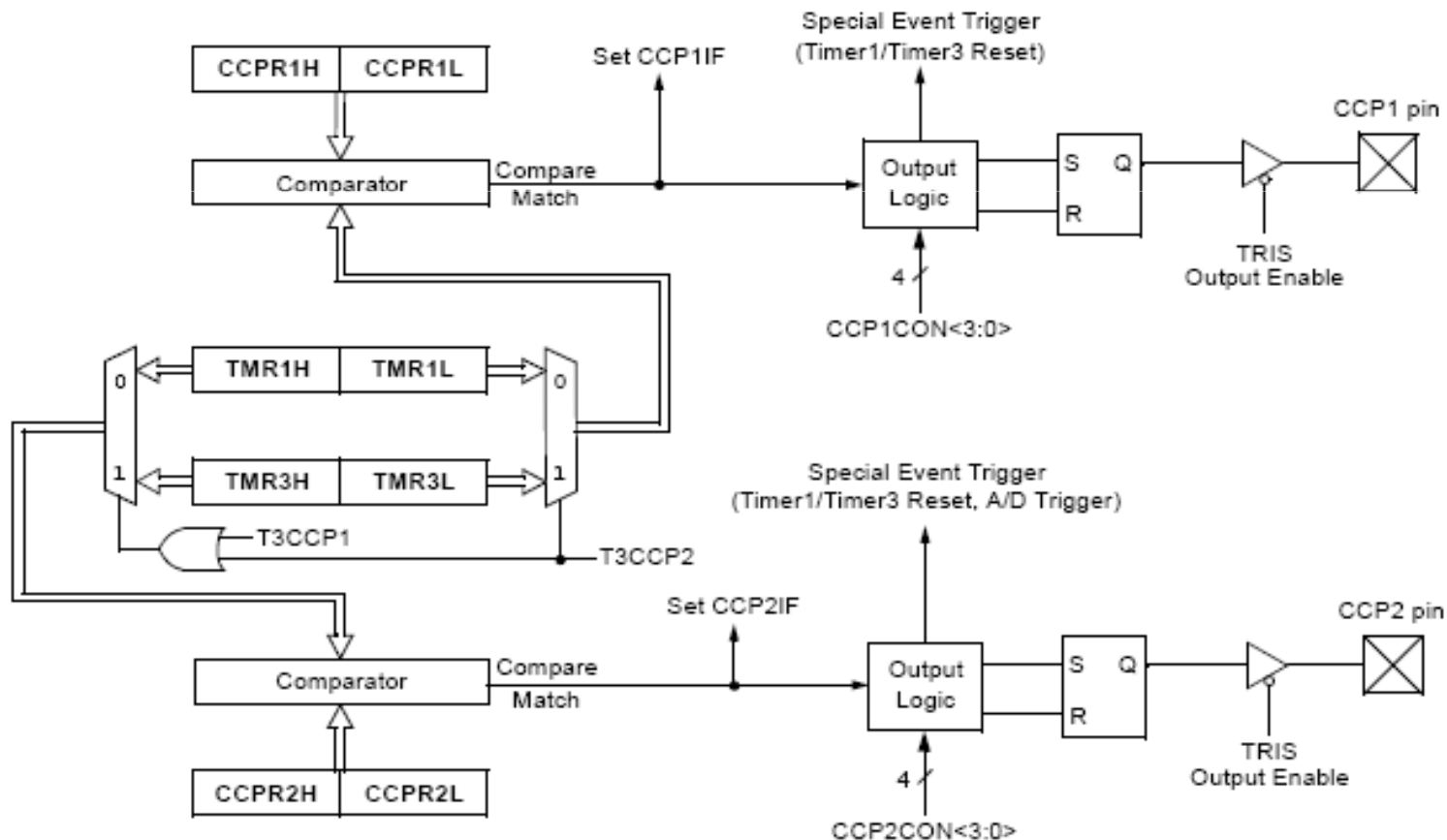
## Módulos CCP en el PIC, Modo Captura

- Utilización de Timer 1 o Timer 3 (temporizador o contador síncrono de 16 bits)
- Evento en pin: Flanco bajada, flanco subida, 4x flanco subida, 16x flanco subida
- Tras evento captura del contenido del timer en CCPRx y activación flag int.



## Módulos CCP en el PIC, Modo Compara

- Utilización de Timer 1 o Timer 3 (temporizador o contador síncrono de 16 bits)
- Compara CCPRx con el contenido del timer, cuando son iguales el pin asociado: se invierte, se pone a nivel alto, se pone a nivel bajo, no se modifica
- Activación flag interrupción que puede generar una interrupción si se activa.
- Posibilidad de puesta a cero del timer



# Módulos Capture y Compare, Registros Asociados

**TABLE 15-3: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1 AND TIME**

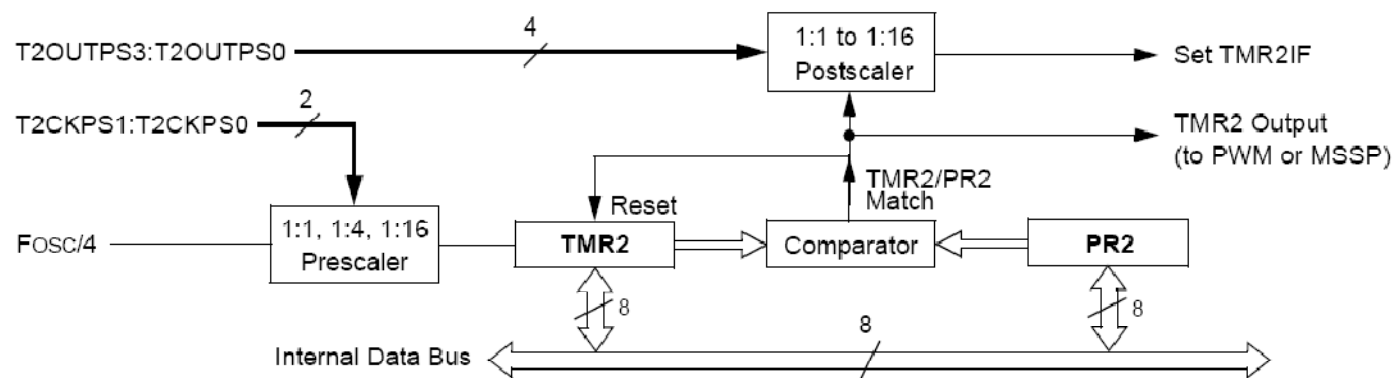
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
RCON	IPEN	SBOREN <sup>(1)</sup>	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
PIR1	PSPIF <sup>(2)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
PIE1	PSPIE <sup>(2)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
IPR1	PSPIP <sup>(2)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP
TRISB	PORTB Data Direction Control Register							
TRISC	PORTC Data Direction Control Register							
TMR1L	Timer1 Register Low Byte							
TMR1H	Timer1 Register High Byte							
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON
TMR3H	Timer3 Register High Byte							
TMR3L	Timer3 Register Low Byte							
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYNC}$	TMR3CS	TMR3ON
CCPR1L	Capture/Compare/PWM Register 1 Low Byte							
CCPR1H	Capture/Compare/PWM Register 1 High Byte							
CCP1CON	P1M1 <sup>(2)</sup>	P1M0 <sup>(2)</sup>	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
CCPR2L	Capture/Compare/PWM Register 2 Low Byte							
CCPR2H	Capture/Compare/PWM Register 2 High Byte							
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0

## Timers empleados por los módulos CCP en el PIC , Timer 2

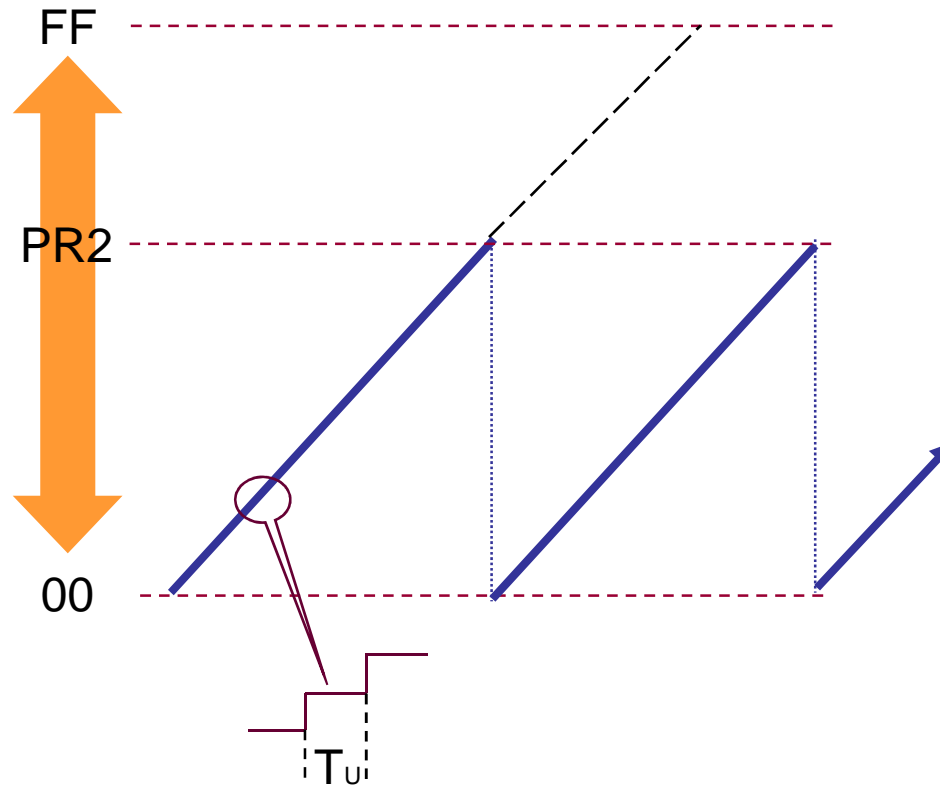
### CARACTERISTICAS

- 8-bit timer and period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- **Interrupt on TMR2-to-PR2 match**
- Optional use as the shift clock for the MSSP module

### ESQUEMA



## Timers empleados por los módulos CCP en el PIC , Timer 2



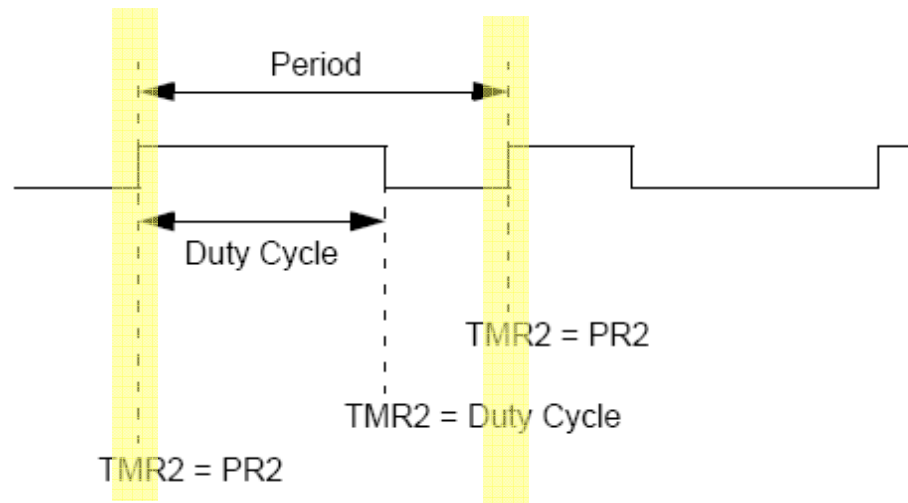
### REGISTROS

(ver T2CON en Data Sheet)

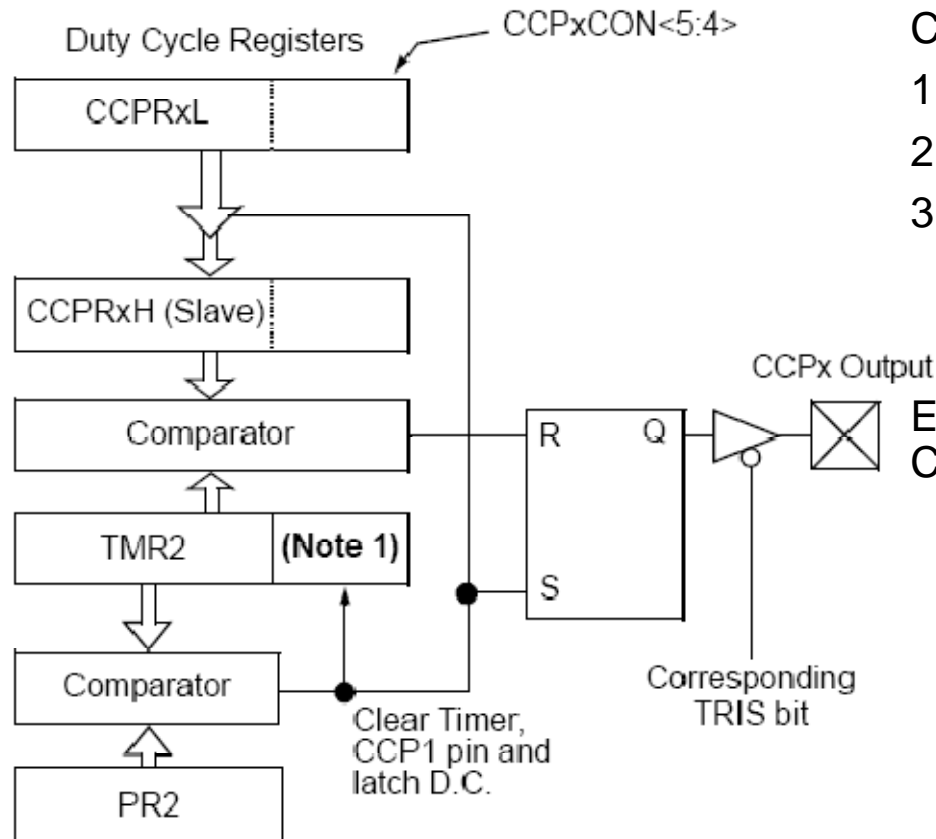
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP
TMR2	Timer2 Register							
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
PR2	Timer2 Period Register							

# Módulo PWM

- Base de tiempos establecida por Timer 2
- **Periodo PWM** especificado en registro PR2 (8 bits)  
Periodo PWM =  $[(PR2)+1] \cdot 4 \cdot T_{osc} \cdot (PMR2 \text{ valor preescalado})$
- **Ciclo de trabajo PWM** especificado en **CCPRxL : CCPxCON<5:4>**  
(resolución hasta 10 bits)  
PWM DC =  $(CCPRxL:CCPxCON<5:4>) \cdot T_{osc} \cdot (PMR2 \text{ valor preescalado})$



# Módulo PWM



Cuando TMR2 se iguala a PR2:

1. Reset de TMR2
2. Puesta a 1 del pin del módulo CCPx
3. Precarga de CCPRxL en CCPRxH

El pin del CCPx se pone a cero cuando CCPRxH:2-bit latch es igual a TMR2:2-bit Q



# Módulos CCP, Interacciones entre módulos

**TABLE 15-2: INTERACTIONS BETWEEN CCP1 AND CCP2 FOR TIMER RESOURCES**

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Each module can use TMR1 or TMR3 as the time base. The time base can be different for each CCP.
Capture	Compare	CCP2 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Automatic A/D conversions on trigger event can also be done. Operation of CCP1 could be affected if it is using the same timer as a time base.
Compare	Capture	CCP1 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Operation of CCP2 could be affected if it is using the same timer as a time base.
Compare	Compare	Either module can be configured for the Special Event Trigger to reset the time base. Automatic A/D conversions on CCP2 trigger event can be done. Conflicts may occur if both modules are using the same time base.
Capture	PWM <sup>(1)</sup>	None
Compare	PWM <sup>(1)</sup>	None
PWM <sup>(1)</sup>	Capture	None
PWM <sup>(1)</sup>	Compare	None
PWM <sup>(1)</sup>	PWM	Both PWMs will have the same frequency and update rate (TMR2 interrupt).