

Microprocesadores, Tema 9:

Módulo ADC

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Objetivos

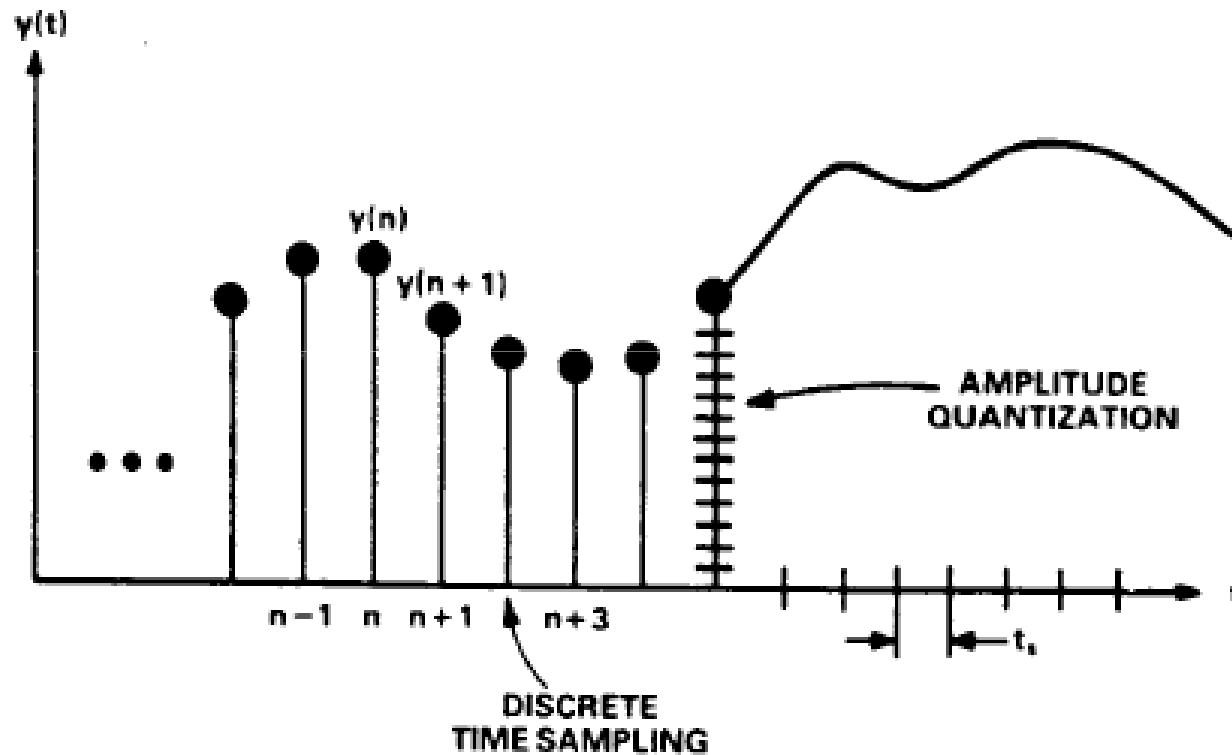
Principios básicos de la conversión AD

El módulo ADC del PIC

Librerías disponibles en C

Principios de Conversión AD, Discretización

Discretización en dos variables



Discretización de amplitud:

Se representa un número discreto de valores de tensión
(Cuantificación)

Discretización temporal:

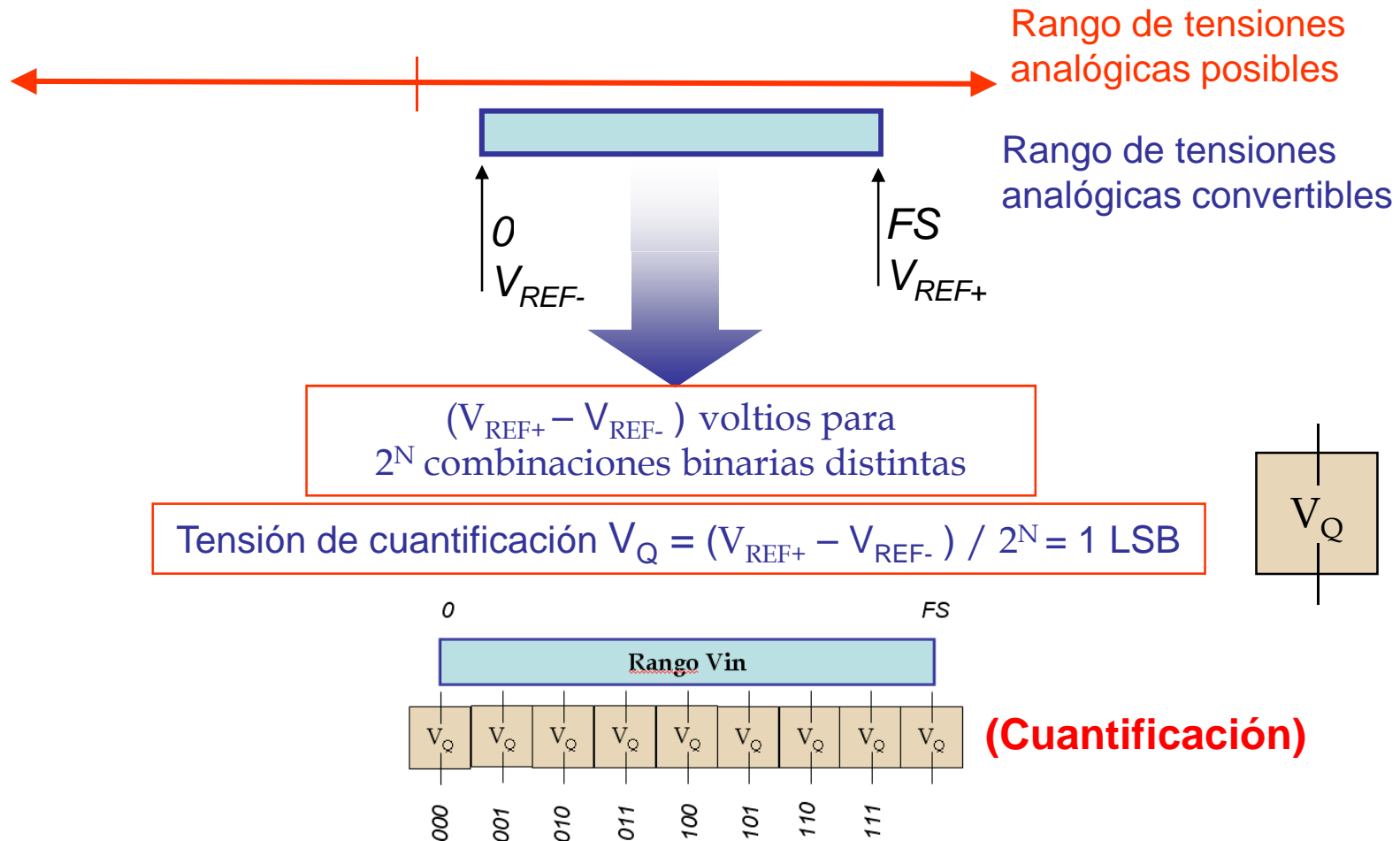
Se toma el valor de tensión en instantes discretos de tiempo

(Muestreo)

Principios de Conversión AD, Discretización de Amplitud

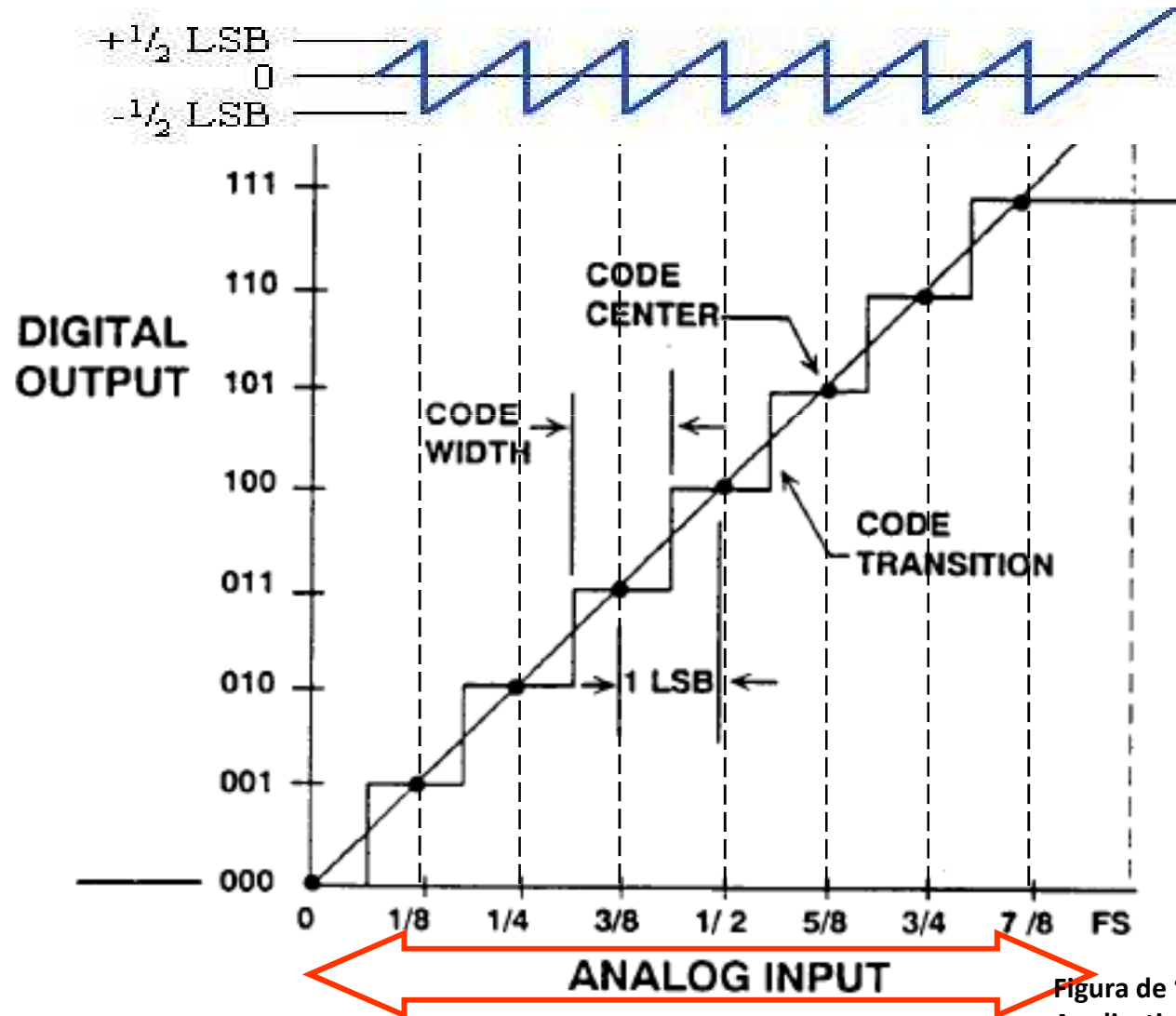
Discretización de amplitud (RESOLUCION):

La tensión se representa con un número de bits N , dando lugar a 2^N combinaciones distintas que nos permite representar 2^N valores discretos de tensión



Principios de Conversión AD, Discretización de Amplitud

Función de Transferencia con N = 3:



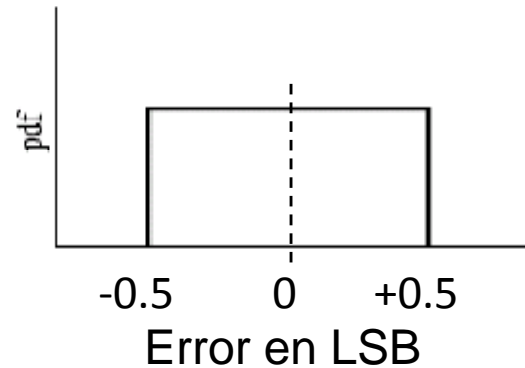
Error de Cuantificación

$$V_{IN} = V_Q \sum_{k=0}^{N-1} b_k 2^k + \epsilon$$

Figura de "Fundamentals of Sampled Data Systems"
Application Note AN-282
Analog Devices

Principios de Conversión AD, Discretización de Amplitud

Efecto del Ruido introducido en la señal por el proceso de Cuantificación

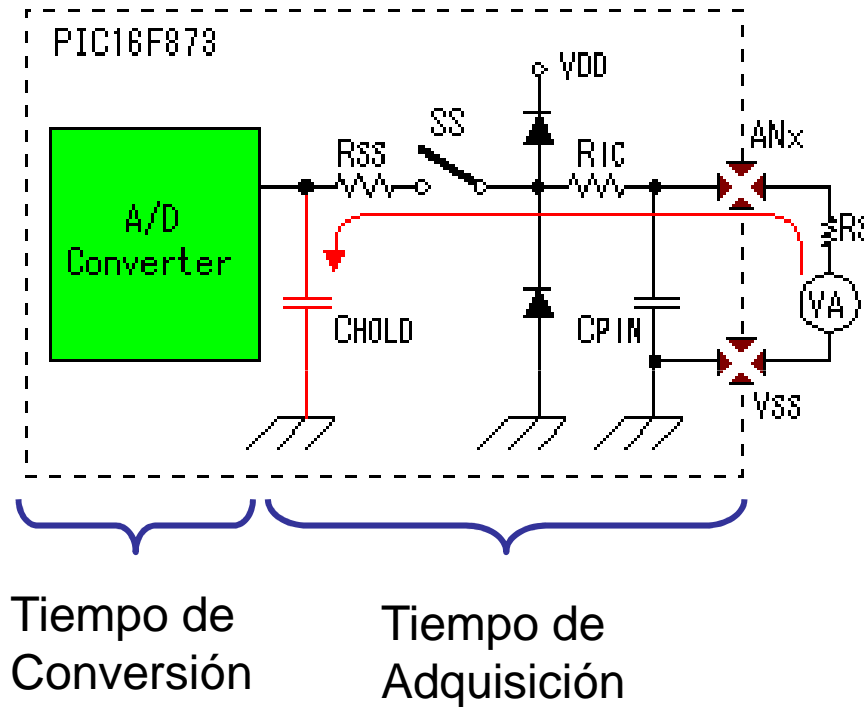


$$\text{SNR} = 20 \log \left(\frac{V_{\text{rms}}}{\sqrt{E(\epsilon^2)}} \right) = 20 \log(2^N \sqrt{1.5}) = 6.02N + 1.76 \text{ dB}$$

| resolution | signal-to-noise ratio |
|------------|-----------------------|
| 6 bits | 37.9 dB |
| 8 bits | 49.9 dB |
| 10 bits | 62.0 dB |
| 12 bits | 74.0 dB |
| 14 bits | 86.0 dB |
| 16 bits | 98.1 dB |

Principios de Conversión AD, Discretización Temporal

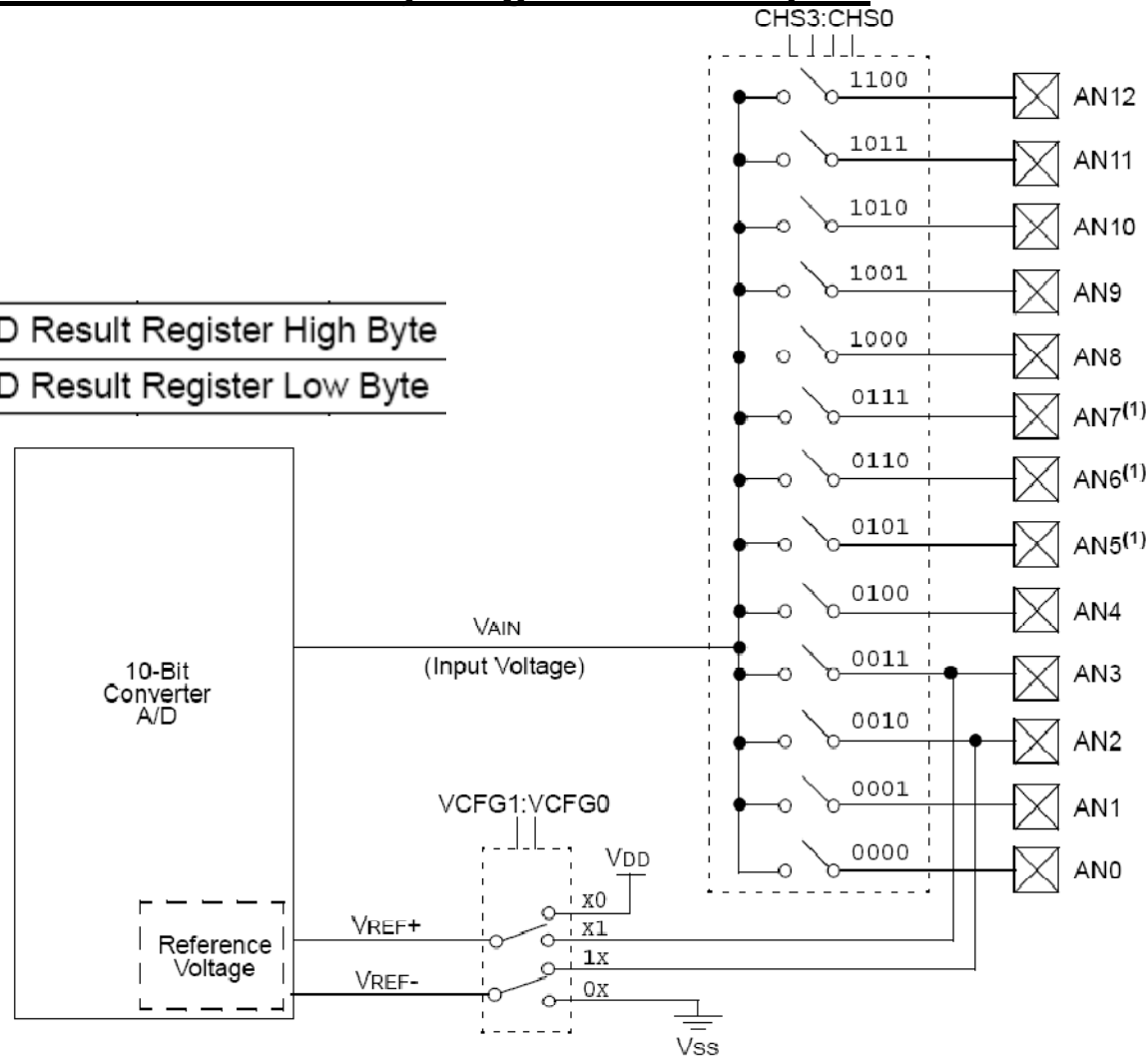
Sample and Hold:



Módulos ADC del PIC, Diagrama de Bloques

Registros de Control del Conversor y Diagrama de Bloques

| | |
|--------|-------------------------------|
| ADCON0 | |
| ADCON1 | |
| ADCON2 | |
| ADRESH | A/D Result Register High Byte |
| ADRESL | A/D Result Register Low Byte |



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.

Módulos ADC del PIC, Función de los Pines

REGISTER 19-2: ADCON1: A/D CONTROL REGISTER 1

| | | | | | | | |
|-------|-----|-------|-------|----------------------|--------------------|--------------------|--------------------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 ⁽¹⁾ | R/W ⁽¹⁾ | R/W ⁽¹⁾ | R/W ⁽¹⁾ |
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | bit 0 | | | |

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (VREF- source)
 1 = VREF- (AN2)
 0 = VSS

bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)
 1 = VREF+ (AN3)
 0 = VDD

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

| PCFG3: PCFG0 | AN12 | AN11 | AN10 | AN9 | AN8 | AN7 ⁽²⁾ | AN6 ⁽²⁾ | AN5 ⁽²⁾ | AN4 | AN3 | AN2 | AN1 | AN0 |
|---------------------|------|------|------|-----|-----|--------------------|--------------------|--------------------|-----|-----|-----|-----|-----|
| 0000 ⁽¹⁾ | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111 ⁽¹⁾ | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input

D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

Módulos ADC del PIC, Control de la Conversión

REGISTER 19-1: ADCON0: A/D CONTROL REGISTER 0

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | |
|-------|-----|-------|-------|-------|-------|---------|-------|-------|
| — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/DONE | ADON | |
| bit 7 | | | | | | | | bit 0 |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
 0001 = Channel 1 (AN1)
 0010 = Channel 2 (AN2)
 0011 = Channel 3 (AN3)
 0100 = Channel 4 (AN4)
 0101 = Channel 5 (AN5)^(1,2)
 0110 = Channel 6 (AN6)^(1,2)
 0111 = Channel 7 (AN7)^(1,2)
 1000 = Channel 8 (AN8)
 1001 = Channel 9 (AN9)
 1010 = Channel 10 (AN10)
 1011 = Channel 11 (AN11)
 1100 = Channel 12 (AN12)
 1101 = Unimplemented⁽²⁾
 1110 = Unimplemented⁽²⁾
 1111 = Unimplemented⁽²⁾

Note 1: These channels are not implemented on 28-pin devices.

2: Performing a conversion on unimplemented channels will return a floating input measurement.

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress
 0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
 0 = A/D converter module is disabled

Módulos ADC del PIC, Tiempo de Conversión

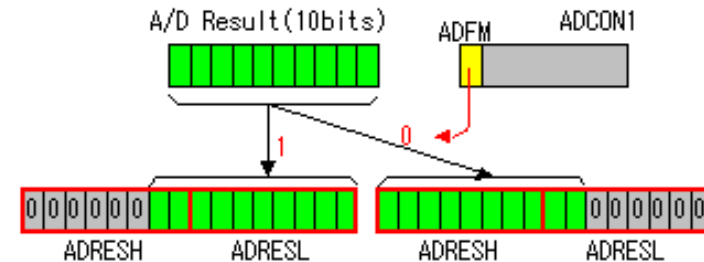
REGISTER 19-3: **ADCON2: A/D CONTROL REGISTER 2**

| | | | | | | | |
|-------|-----|-------|-------|-------|-------|-------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

- bit 7 **ADFM:** A/D Result Format Select bit
 1 = Right justified
 0 = Left justified
- bit 6 **Unimplemented:** Read as '0'
- bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
 111 = 20 TAD
 110 = 16 TAD
 101 = 12 TAD
 100 = 8 TAD
 011 = 6 TAD
 010 = 4 TAD
 001 = 2 TAD
 000 = 0 TAD⁽¹⁾

Tiempo de
Adquisición

- bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
 111 = FRC (clock derived from A/D RC oscillator)⁽¹⁾
 110 = Fosc/64
 101 = Fosc/16
 100 = Fosc/4
 011 = FRC (clock derived from A/D RC oscillator)⁽¹⁾
 010 = Fosc/32
 001 = Fosc/8
 000 = Fosc/2



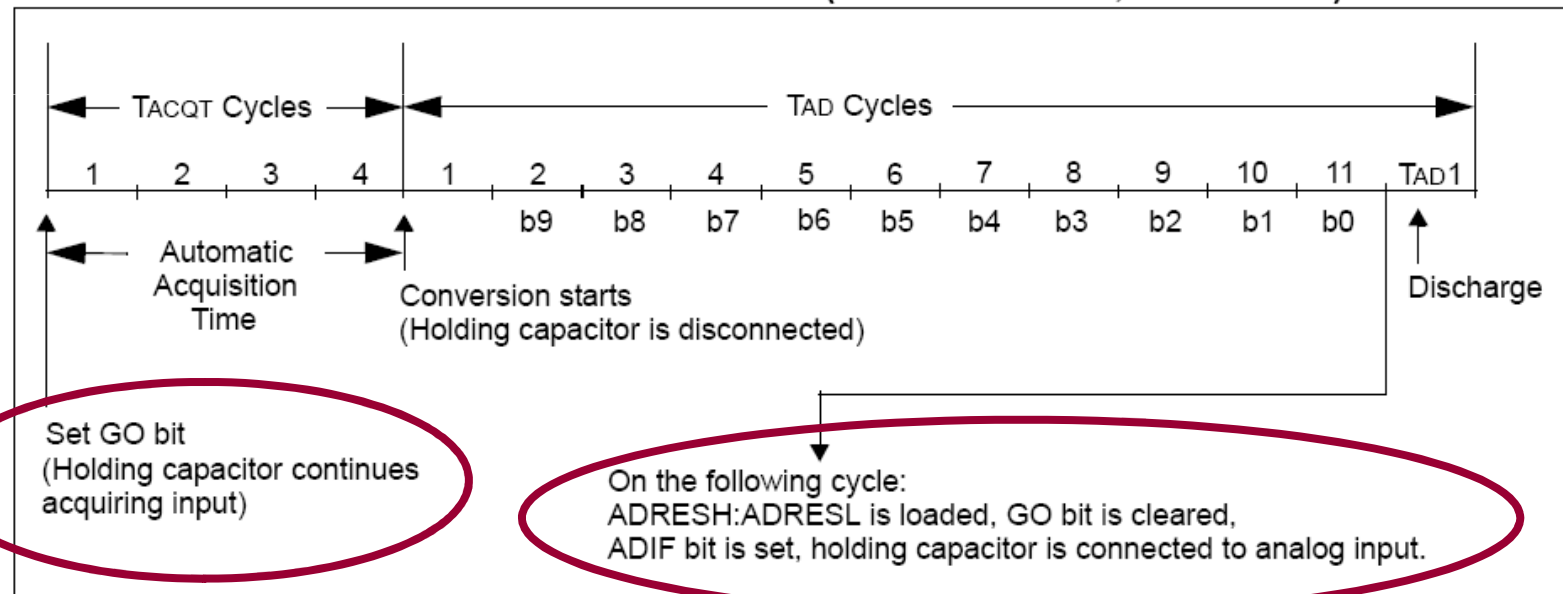
T_{AD}
 Tiempo de
Conversión

Note 1: If the A/D FRC clock source is selected, a delay of one T_{cy} (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

Módulos ADC del PIC, Tiempo de Conversión

The A/D conversion time per bit is defined as T_{AD} . The A/D conversion requires 11 T_{AD} per 10-bit conversion.

FIGURE 19-5: A/D CONVERSION T_{AD} CYCLES ($ACQT<2:0> = 010$, $T_{ACQ} = 4 T_{AD}$)



Inicio Conversión

Fin Conversión

Módulos ADC del PIC, Tiempo de Conversión

T_{AD}

For correct A/D conversions, the A/D conversion clock (T_{AD}) must be as short as possible, but greater than the minimum T_{AD} (see parameter 130 for more information).

T_{ACQ}

EQUATION 19-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

$$T_{AMP} = 0.2 \mu s$$

$$T_{COFF} = \begin{matrix} (\text{Temp} - 25^\circ\text{C})(0.02 \mu s/^\circ\text{C}) \\ (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu s/^\circ\text{C}) \\ 1.2 \mu s \end{matrix}$$

Temperature coefficient is only required for temperatures $> 25^\circ\text{C}$. Below 25°C , $T_{COFF} = 0$ ms.

$$T_C = \begin{matrix} -(\text{CHOLD})(R_{IC} + R_{SS} + R_S) \ln(1/2047) \\ -(25 \text{ pF})(1 \text{ k}\Omega + 2 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0004883) \\ 1.05 \mu s \end{matrix}$$

$$T_{ACQ} = \begin{matrix} 0.2 \mu s + 1 \mu s + 1.2 \mu s \\ 2.4 \mu s \end{matrix}$$

Módulos ADC del PIC, Proceso

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
 - Set $\overline{\text{GO/DONE}}$ bit (ADCON0 register)
5. Wait for A/D conversion to complete, by either:
 - Polling for the $\overline{\text{GO/DONE}}$ bit to be clearedOR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T_{AD} . A minimum wait of $2 T_{AD}$ is required before the next acquisition starts.

ADC en el C18, Librerías

| Función | Descripción |
|------------|--------------------------------|
| BusyADC | Hay una conversión en curso? |
| CloseADC | Apaga el conversor ADC |
| ConvertADC | Inicia una conversión |
| OpenADC | Configura el Conversor |
| ReadADC | Lee una muestra |
| SetChanADC | Selección del canal de entrada |