

UNIVERSIDAD CARLOS III DE MADRID



# PRACTICE MANUAL: PHYSICAL DESIGN

## *Integrated Circuits and Microelectronics*

Celia López Ongil  
Luis Entrena Arrontes  
Almudena Lindoso Muñoz  
Marta Portela García  
Enrique San Millán Heredia  
Mario García Valderas

These practices consist on performing the design of simple integrated circuits at physical level. For this purpose, we will use the tool Microwind that is a free tool available from the web site [www.microwind.org](http://www.microwind.org).

### 1. PRACTICE 1: PARITY ERROR DETECTOR

Parity bit is the simplest mechanism for performing error detection. It consists on adding an additional bit to the data word to transmit or store. The resulting data word must contain an even number of 1's (even parity) or an odd number of 1's (odd parity). In this practice, the student must design at layout level a circuit able to detect parity errors in 3-bits data words, 2-bits for data and 1 bit corresponding to the parity bit.

The steps to follow are:

- Obtain the logic equations for the parity error function  $P_{err}$ . Take into account the necessary considerations in order to design an optimum circuit.
- Draw the design schematic based in the equations obtained in the previous point.
- Draw the transistor schematic. Justify the chosen implementation (transmission gates, pass transistors or complementary logic).
- Develop the layout design by using Microwind. Check the design rules. Simulate the circuit in order to test its behavior.

### 2. PRÁCTICA 2: MAJORITY VOTER

The aim of this practice is the design of a majority voter circuit. It must calculate the result ( $vot$ ) of voting three inputs. Additionally to the three inputs to vote ( $A, B, C$ ), the circuit has a fourth input that is the expected value ( $exp$ ) for the result  $vot$ . The circuit must generate an output named  $error$  what is active when the voting result differs from the expected data.

The steps to follow are:

- Obtain the logic equations for outputs  $vot$  and  $error$ .
- Draw the design schematic based in the equations obtained in the previous point.
- Draw the transistor schematic. XOR cells must be designed with transmission gates and the rest of logic cells with CMOS logic and without using transmission gates.
- Develop the layout design by using Microwind. Check the design rules. Simulate the circuit in order to test its behavior.