Microprocessor based digital Systems

The PIC 18F Architecture

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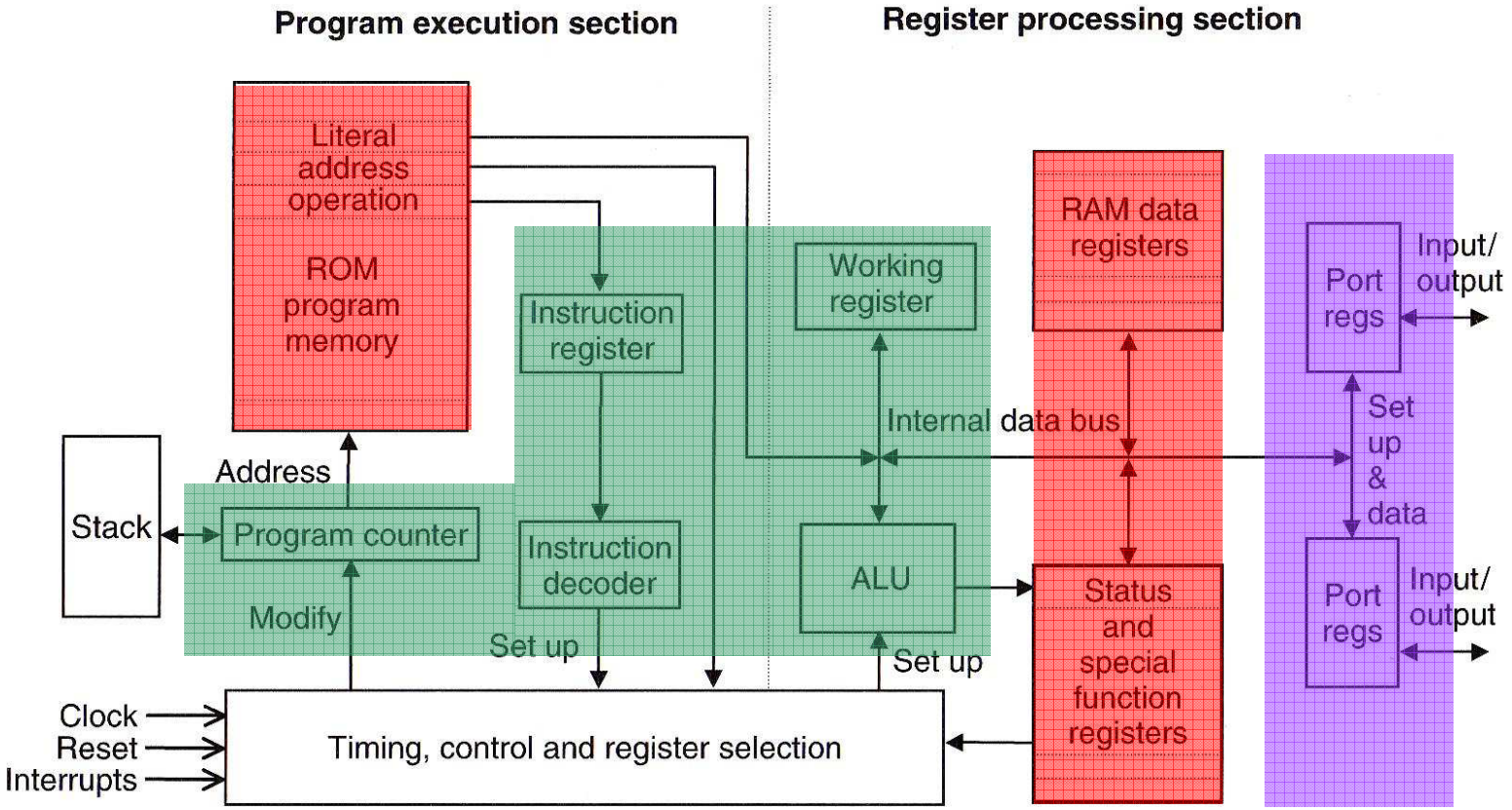
Schamatic Block Diagram



"PIC microcontrollers: An introduction to Microelectronics"
M. Bates
Elsevier/Newnes 2004

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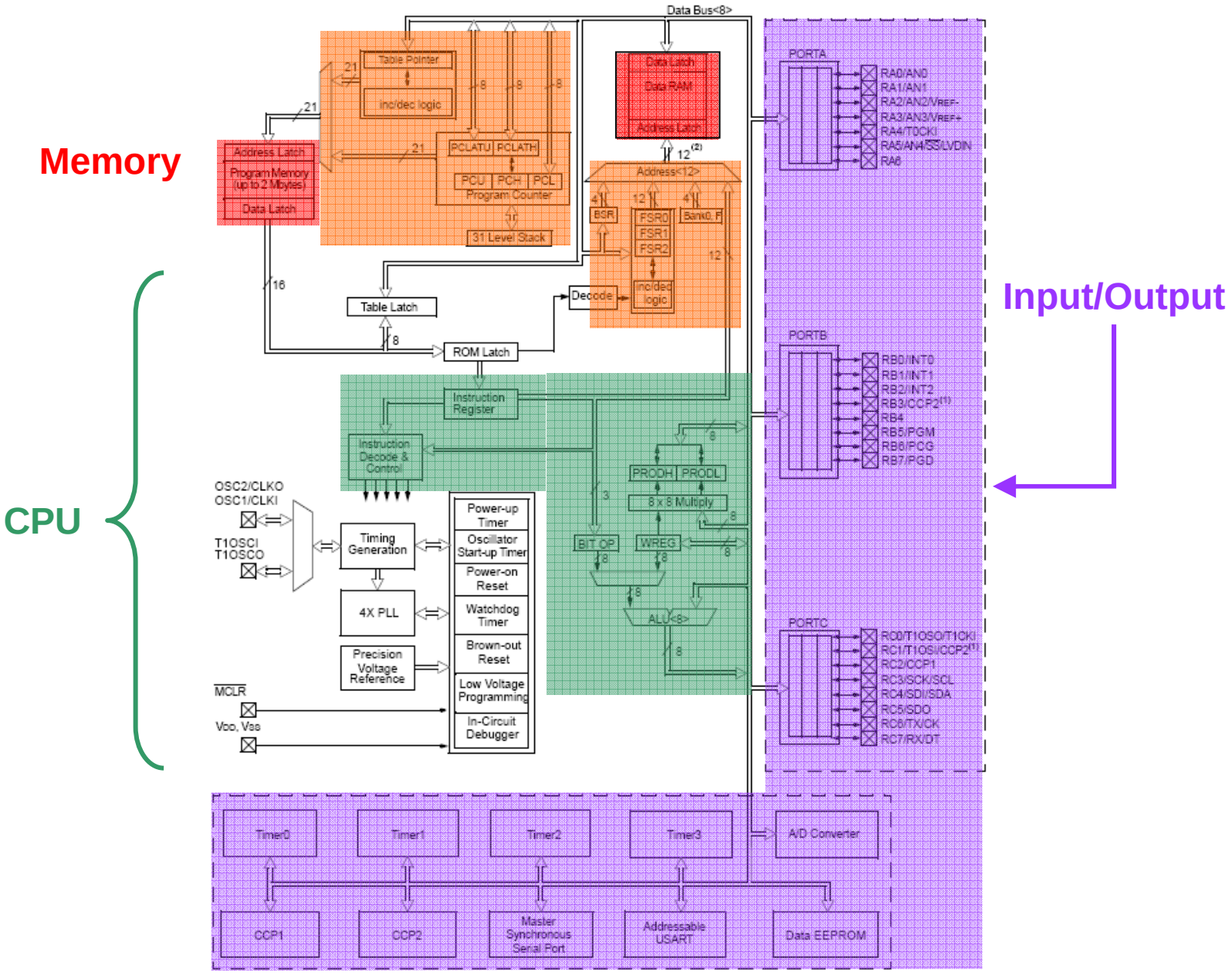
Con permiso de MICROCHIP

PIC 18 Architecture Data Path



MEMORY: General Characteristics

Harvard Architecture:

1. **PROGRAM Memory,** - - - - - - - - - - - > stores: **INSTRUCTIONS & DATA**

2. **DATA Memory**, - - - - - - - - - - - > stores: **DATA**
   composed of two main areas:

   2.1 RAM Area, with:
   22 specific file registers (**SFR**) – PIC 18F Control Registers
   36 general purpose registers (**GPR**) – Temporal storage

   2.2 EEPROM Area, with 64 bytes for storage of non-volatile CONFIG data

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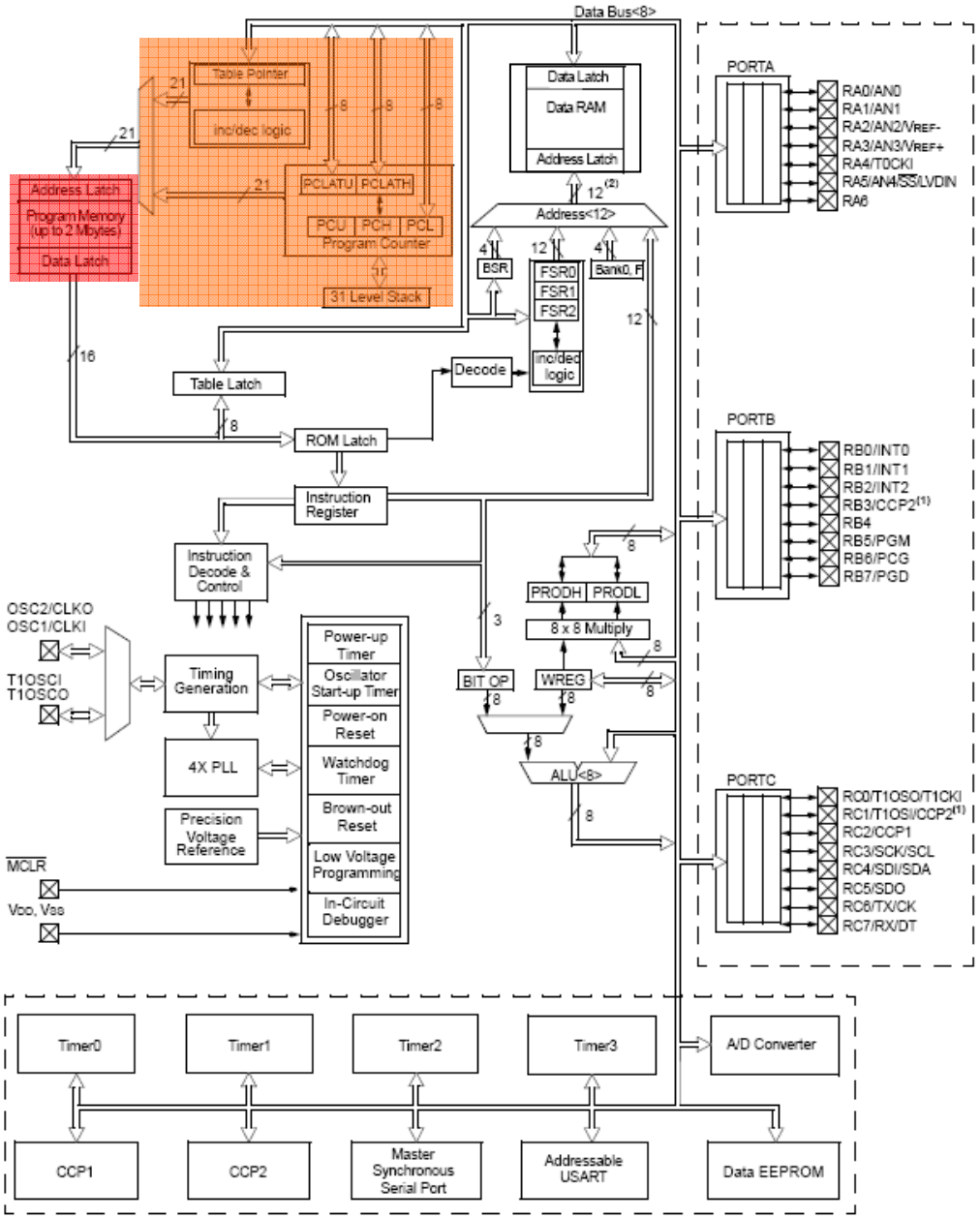
PROGRAM Memory: Organization

Program Memory



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PROGRAM Memory: Organization

Memory Map

Prog. Memory Data Units

Instruction 16 bits

Data 8 bits

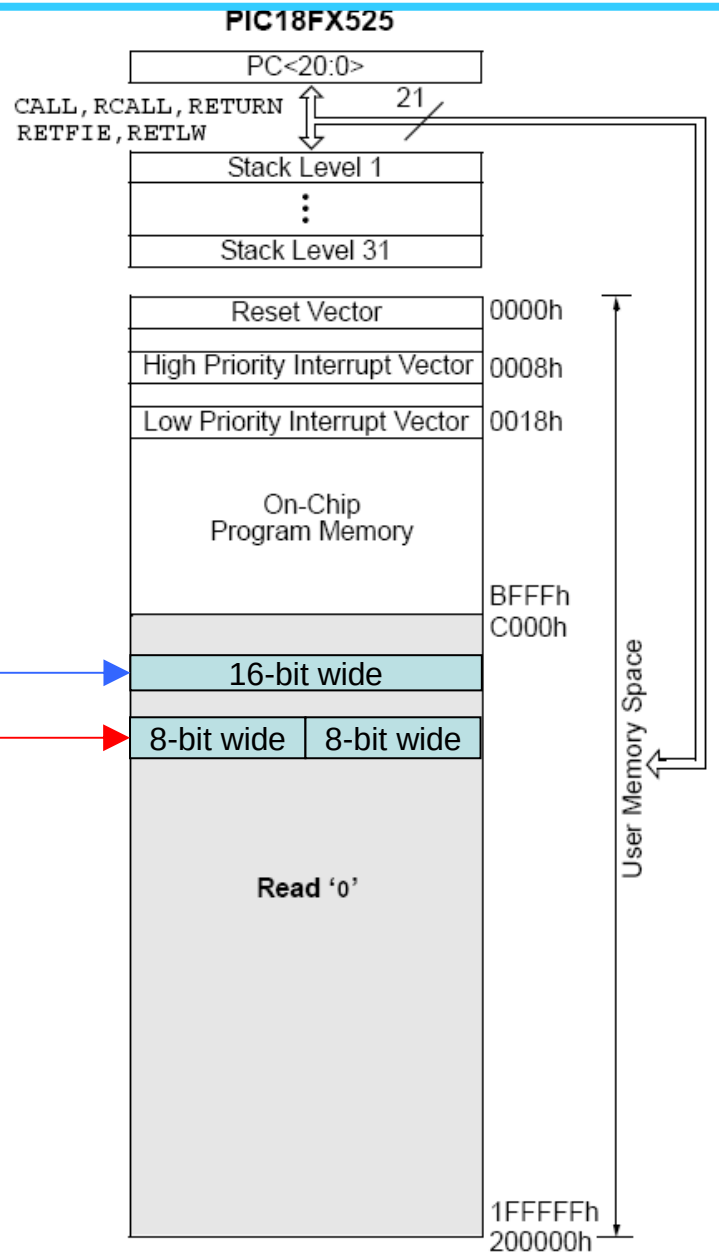
Prog. Memory addresses

Each byte (8 bits) has its own address

0000 0001
0002 0003

Special Memory Locations

0000h = RESET vector
0008h = HP Interrupt vector
0018h = LP Interrupt vector



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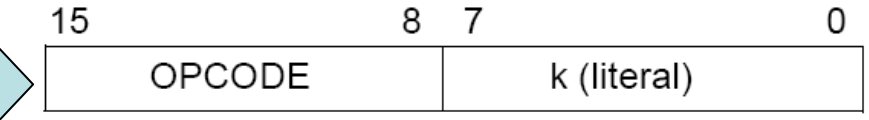
PROGRAM Memory: Organization

21-bit address!

Literal operations



k = 8-bit immediate value

MOVLW	**Move Literal to W**
Syntax:	MOVLW k
Operands:	$0 \le k \le 255$
Operation:	$k \rightarrow W$
Status Affected:	None
Encoding:	0000 1110 kkkk kkkk
Description:	The eight-bit literal ‘k’ is loaded into W.

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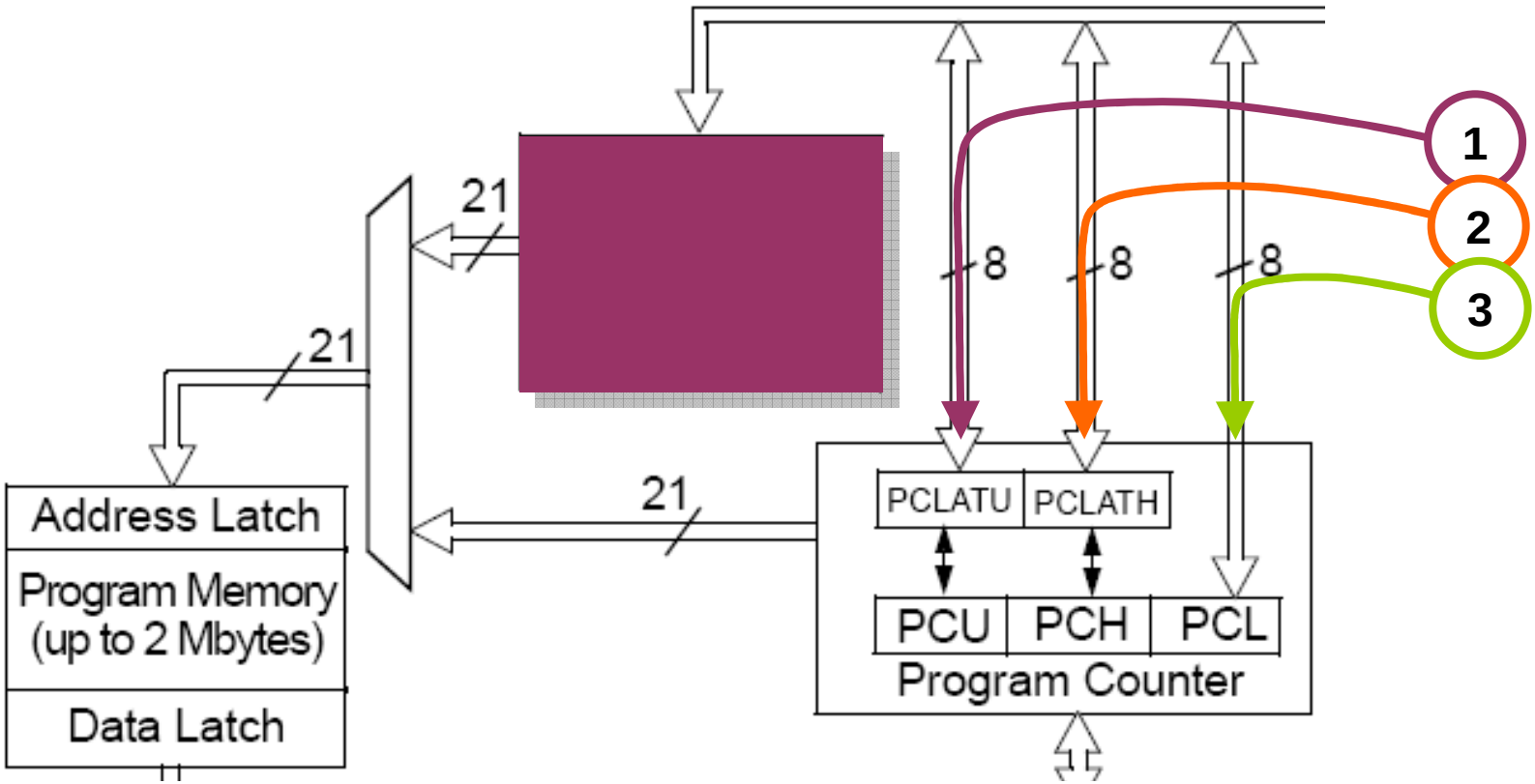
PROGRAM Memory: Addressing Instructions

Instrucction Addressing: Program Counter



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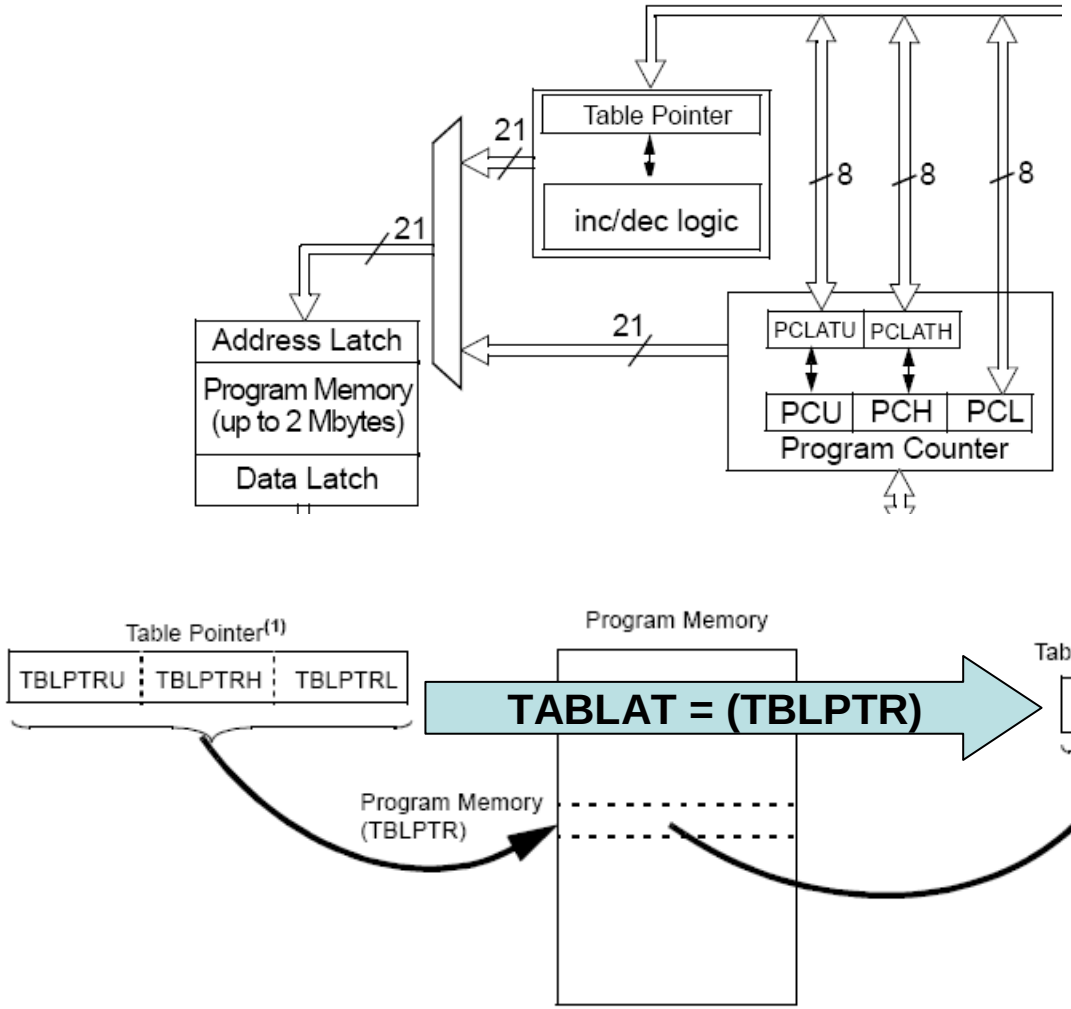
PROGRAM Memory: Addressing Data

Addressing Data (in PROGRAM memory): Pointing data in Memory (**POINTERS**)



Related Instructions

TBLRD*

TABLAT = (TBLPTR)

TBLRD*+

TABLAT = (TBLPTR)
TBLPTR = (TBLPTR)+1

TBLRD*-

TABLAT = (TBLPTR)
TBLPTR = (TBLPTR)-1

TBLRD+*

TBLPTR = (TBLPTR)+1
TABLAT = (TBLPTR)

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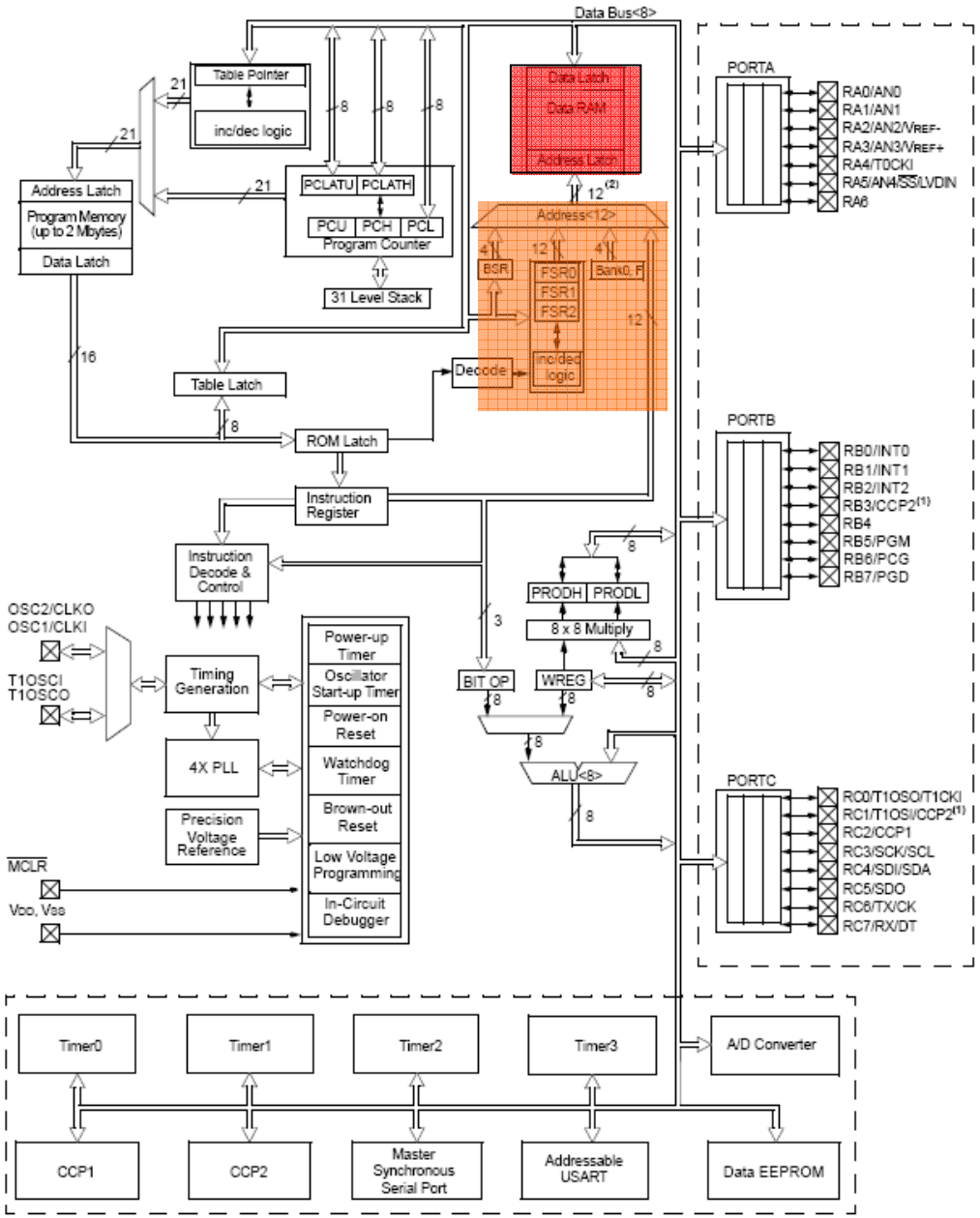
DATA Memory: Organization

Data Memory



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DATA Memory: Organization

Size:

12 (4+8) bit Addresses:
4096 positions

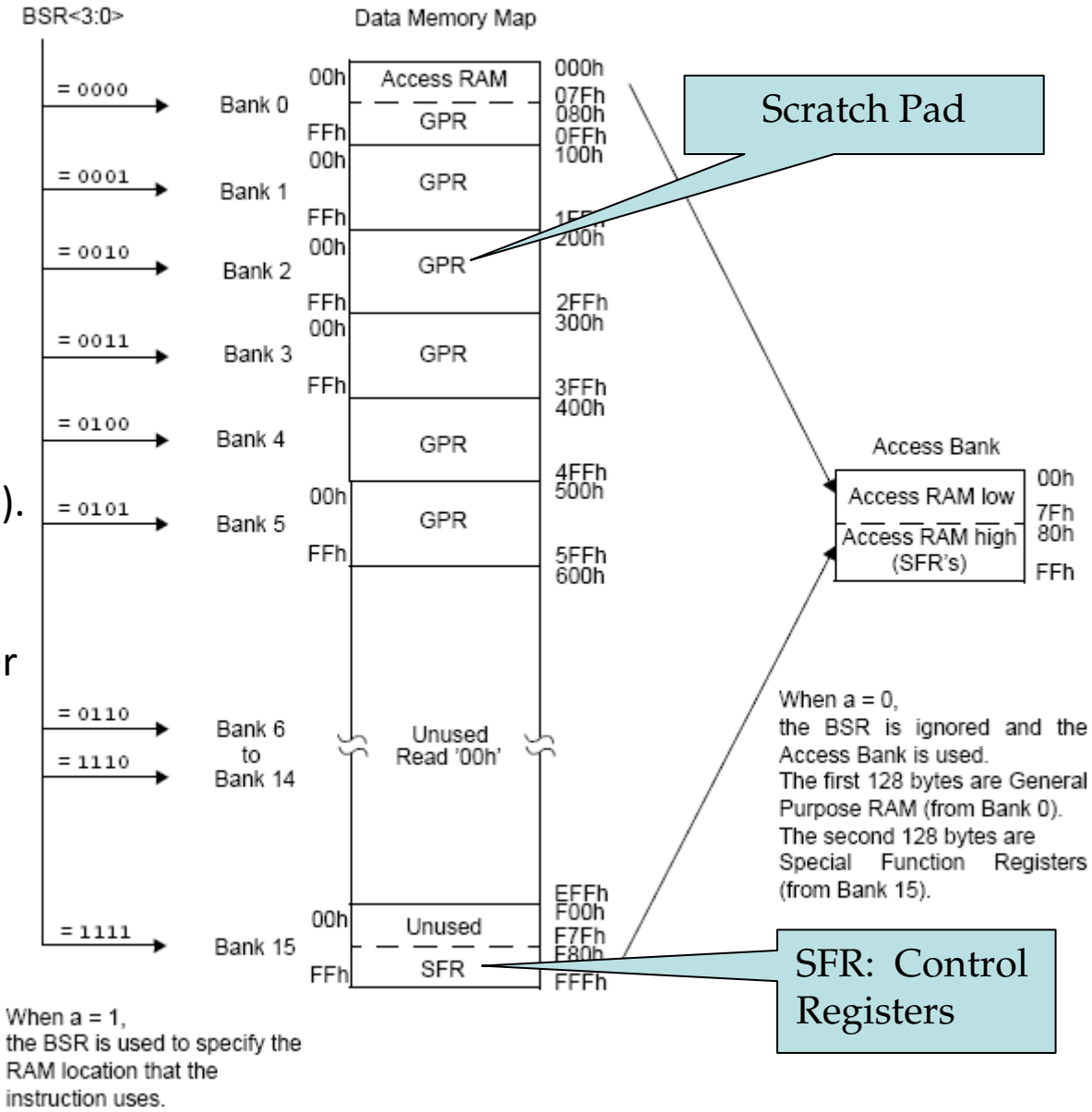
Organization:

Banked: 16 banks (4)
each with 256 bytes (8).

Bank Select (BSR<3:0>):
4 bits from Bank Select Register select active bank

Notice

SFR area, last 32 positions in bank 15.



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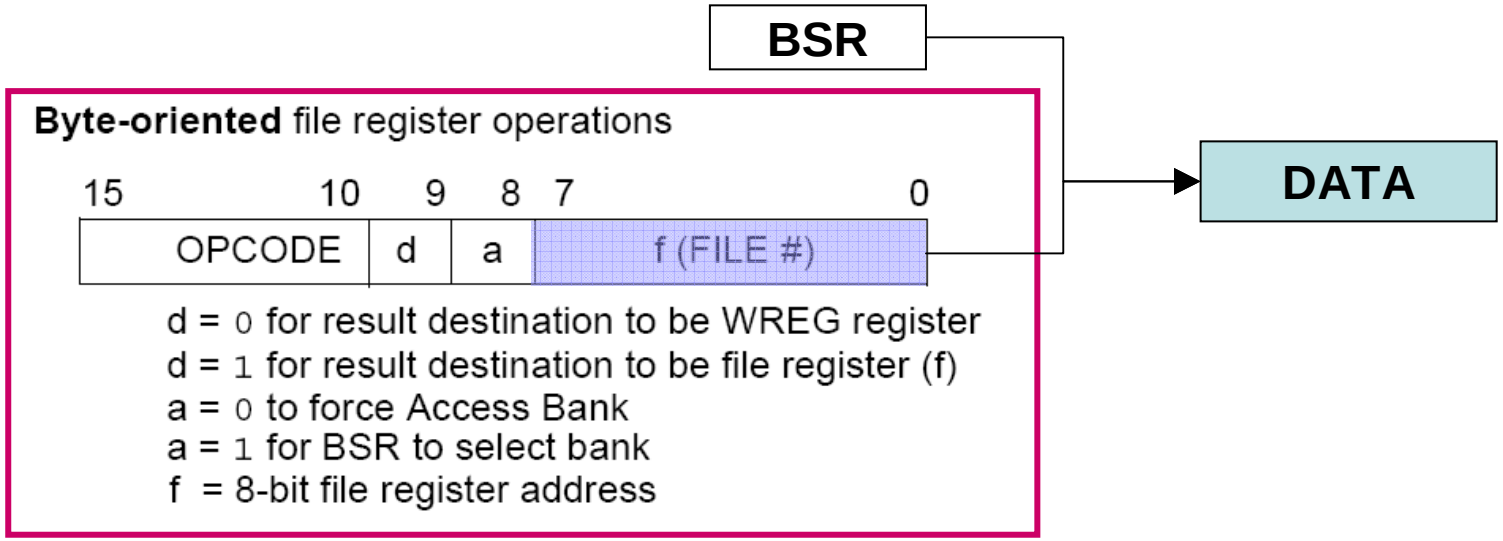
DATA Memory: Organization



MOVWF	**Move W to f**
Syntax:	MOVWF f {,a}
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]
Operation:	(W) → f
Status Affected:	None
Encoding:	0110 111a ffff ffff

Example of data movement

Set the value of a RAM register:

```
MOVLW   valor
MOVWF   F
```

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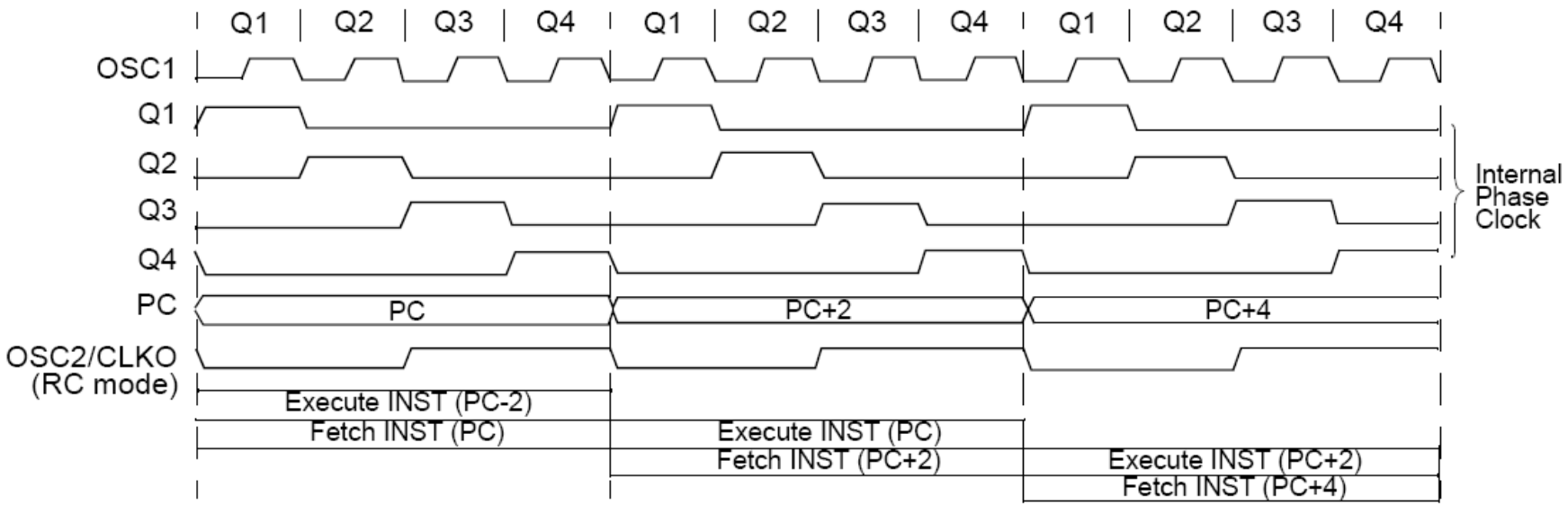
Pipeline: Parallel Processing



f_{OSC} = 8 MHz → T_{OSC} = 125 ns → T_{cyc} = 500 ns

f_{OSC_MAX} =20 MHz → T_{OSC} = 50 ns → T_{cyc} = 200 ns

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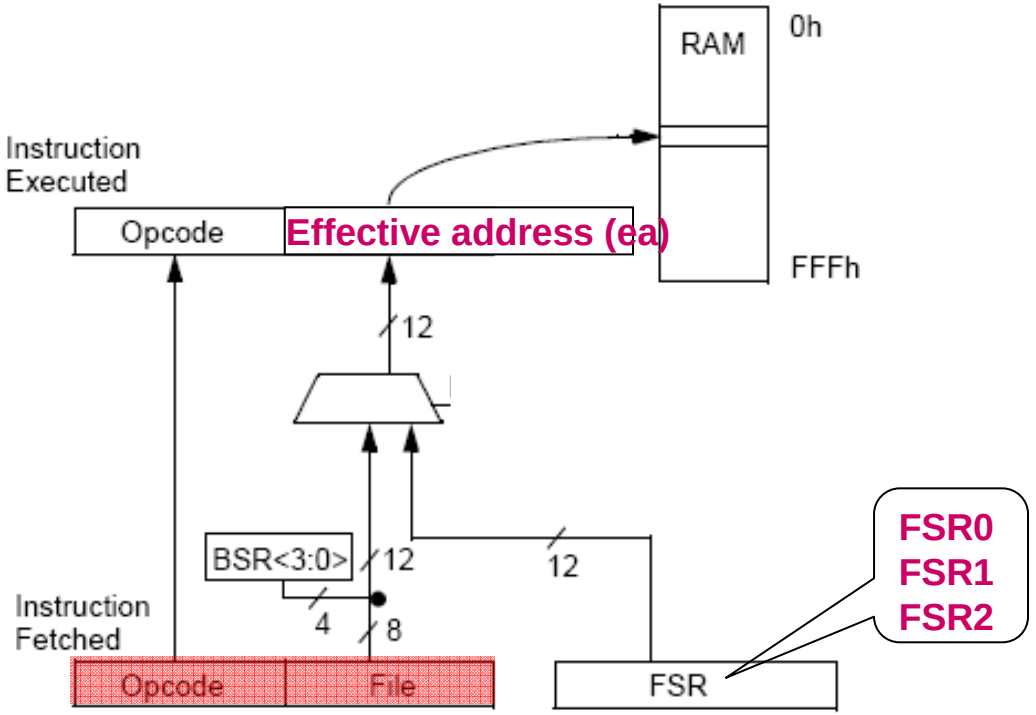
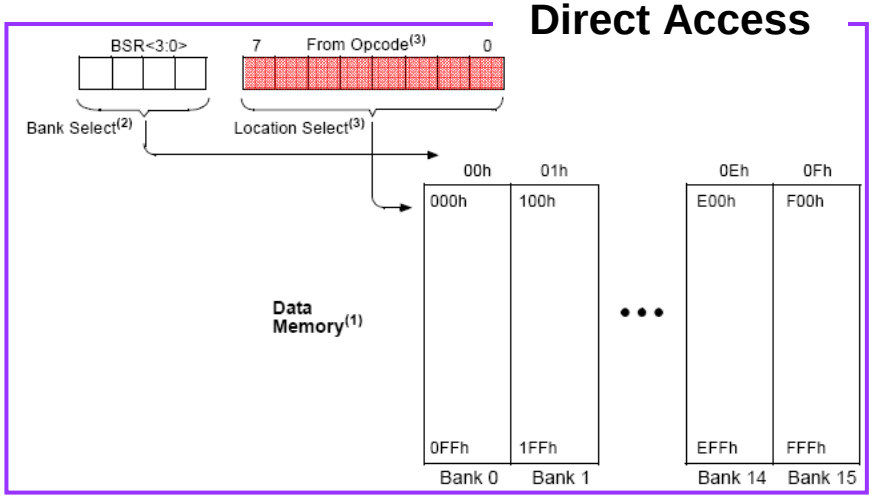
DATA Memory: Data Access



Direct Access



Indirect Access

POSTDEC	de = (FSRx) FSRx = (FSRx)-1
POSTINC	de = (FSRx) FSRx = (FSRx)+1
PREINC	
PLUSW	de = (FSRx) + (W)

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DATA Memory: SFR Area

Stack

PC

Indirect Access FSR0

IO Ports

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(3)	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2(3)	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2(3)	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2(3)	FBCh	CCPR2H	F9Ch	—
FFBh	PCLATU	FDBh	PLUSW2(3)	FBBh	CCPR2L	F9Bh	—
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	—
FF9h	PCL	FD9h	FSR2L	FB9h	—	F99h	—
FF8h	TBLPTRU	FD8h	STATUS	FB8h	—	F98h	—
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	—	F97h	—
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	—	F96h	TRISE(2)
FF5h	TABLAT	FD5h	T0CON	FB5h	—	F95h	TRISD(2)
FF4h	PRODH	FD4h	—	FB4h	—	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	—
FF0h	INTCON3	FD0h	RCON	FB0h	—	F90h	—
FEFh	INDF0(3)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—
FEEh	POSTINC0(3)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—
FEDh	POSTDEC0(3)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(2)
FECh	PREINC0(3)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(2)
FEBh	PLUSW0(3)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	—	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	—
FE7h	INDF1(3)	FC7h	SSPSTAT	FA7h	EECON2	F87h	—
FE6h	POSTINC1(3)	FC6h	SSPCON1	FA6h	EECON1	F86h	—
FE5h	POSTDEC1(3)	FC5h	SSPCON2	FA5h	—	F85h	—
FE4h	PREINC1(3)	FC4h	ADRESH	FA4h	—	F84h	PORTE(2)
FE3h	PLUSW1(3)	FC3h	ADRESL	FA3h	—	F83h	PORTD(2)
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	—	FA0h	PIE2	F80h	PORTA

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DATA Memory: SFR Area (Processor Registers)

STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	N	OV	Z	DC	C
bit 7							bit 0

Unimplemented: Read as '0'

N: Negative bit
This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative (ALU MSB = 1).
1 = Result was negative
0 = Result was positive

OV: Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

DC: Digit carry/$\overline{\text{borrow}}$ bit
For ADDWF, ADDLW, SUBLW, and SUBWF instructions
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

Note: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the bit 4 or bit 3 of the source register.

C: Carry/$\overline{\text{borrow}}$ bit
For ADDWF, ADDLW, SUBLW, and SUBWF instructions
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: For $\overline{\text{borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

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DATA Memory: SFR Area (I/O Ports)

F96h	TRISE(2)
F95h	TRISD(2)
F94h	TRISC
F93h	TRISB
F92h	TRISA
F91h	—
F90h	—
F8Fh	—
F8Eh	—
F8Dh	LATE(2)
F8Ch	LATD(2)
F8Bh	LATC
F8Ah	LATB
F89h	LATA
F88h	—
F87h	—
F86h	—
F85h	—
F84h	PORTE(2)
F83h	PORTD(2)
F82h	PORTC
F81h	PORTB
F80h	PORTA