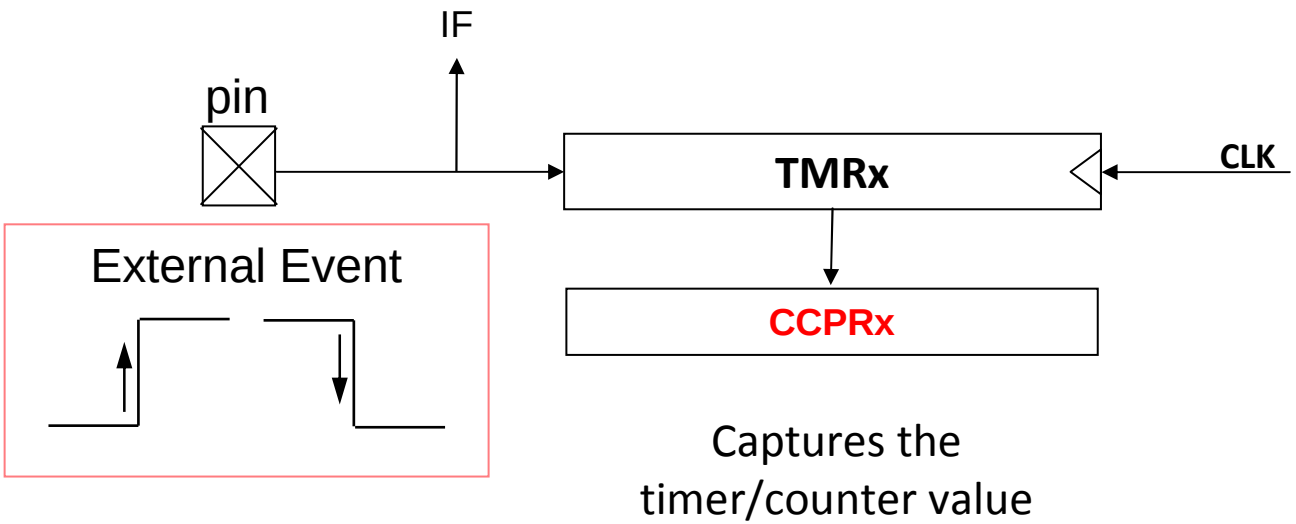
Microprocessor based digital Systems

Advanced Timer Functions (Capture / Compare / PWM)

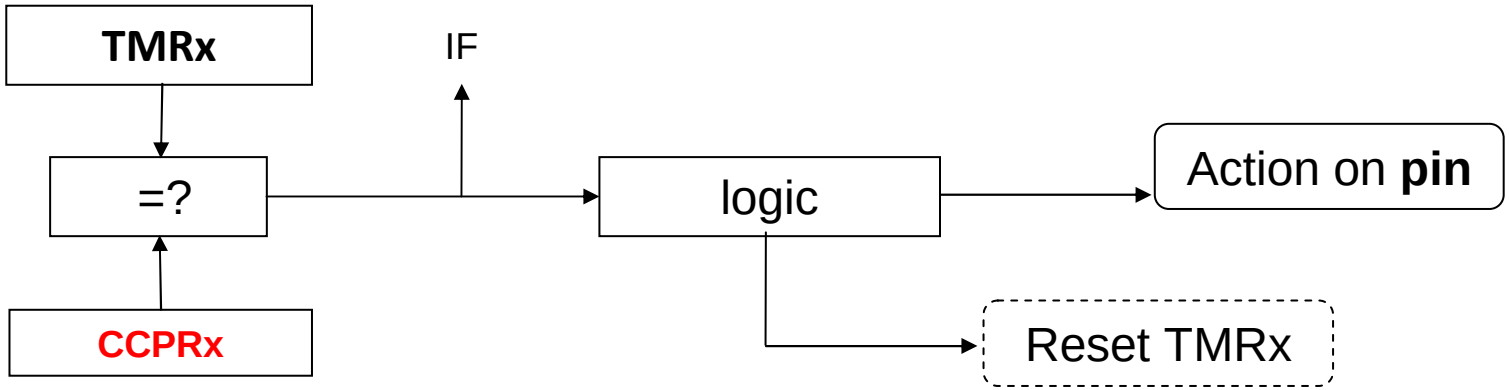
Guillermo Carpintero
Marta Ruiz
Universidad **Carlos III** de Madrid

Capture Function



Gives a reference on the instant in which the event takes place
(Application: measure the period of a given signal)

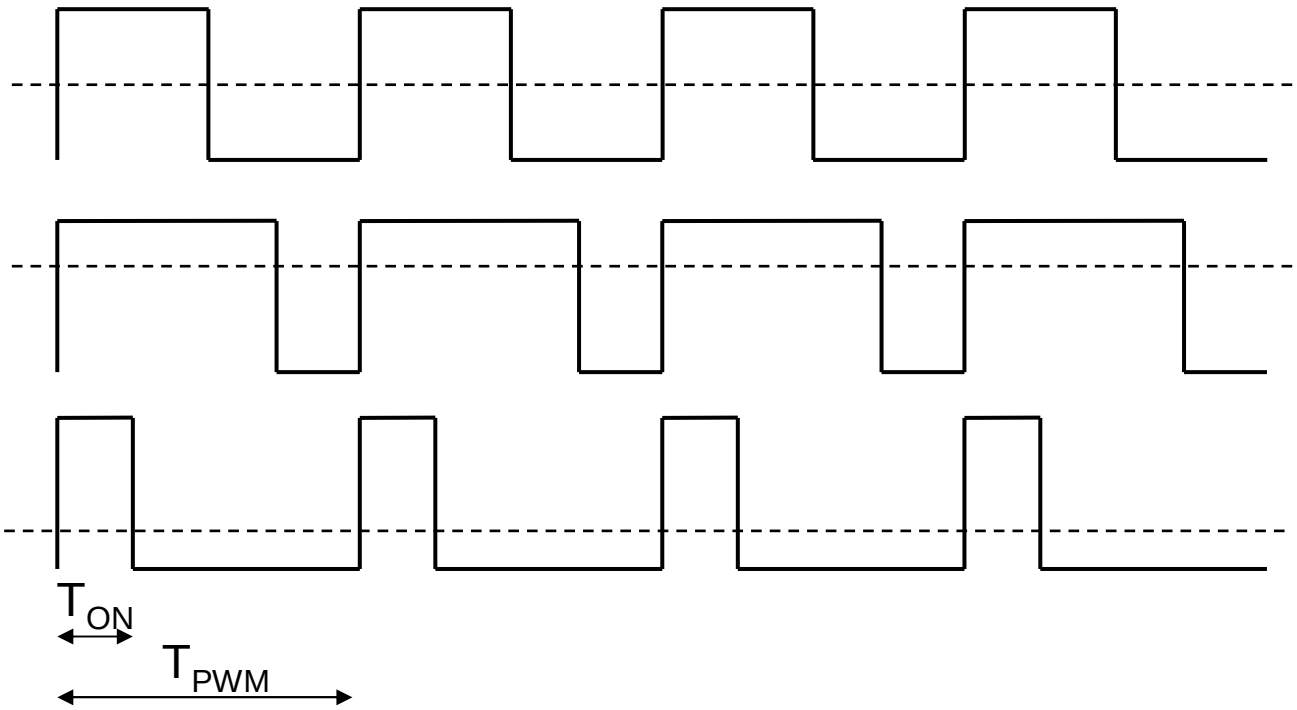
Compare Function



Generates equally spaced time intervals
(Application: Delays, Pulse Trains)

Pulse Width Modulation (PWM) Function

Generates (automatically) a PWM signal



Period = T_{PWM}

Frecuency, $F_{PWM} = 1/ T_{PWM}$

Duty Cycle = $(T_{ON} / T_{PWM}) \times 100$

What is the CCP module?

It is a peripheral that allows to control the timers to achieve the described functions

Timer 1 **Timer 3**	+	**CCP**	= **Capture** **Compare**
Timer 1			**PWM**

CCP modes and timers:

CCP/ECCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2

CCP Modules, General Characteristics

Two modules: **CCPx (x = 1, 2)**

Associated Registers:

- **CCPRx (CCPRxH:CCPRxL): 16bit Data Reg**
  - -In Capture: CCPRx stores the timer counter on appearance of the event
  - -In Compare: CCPRx holds the constant data to compare
  - -In PWM, CCPRx defines the DC (Duty Cycle)

- **CCPxCON: Control Reg**
  - -Selects the CCP operation mode

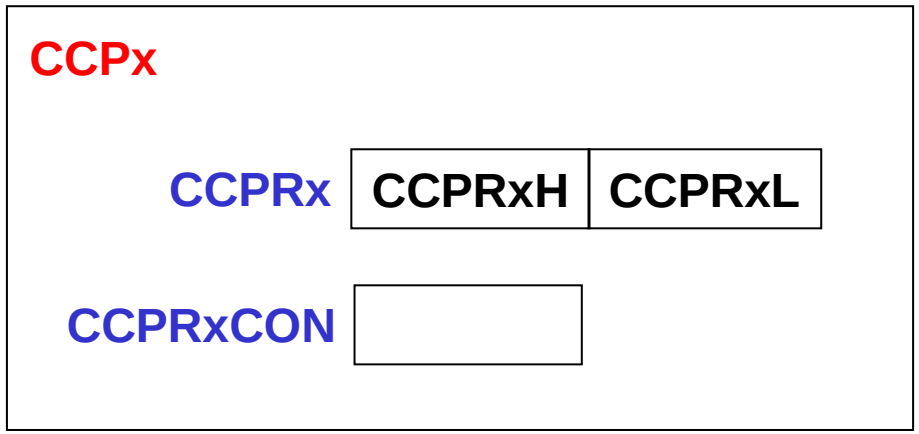


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

CCP Module, Control Reg

REGISTER 15-1: CCPxCON REGISTER (CCP2 MODULE, CCP1 MODULE IN 28-PIN DEVICES)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **DCxB1:DCxB0**: PWM Duty Cycle bit 1 and bit 0 for CCP Module x

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two LSbs (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight MSbs (DCx9:DCx2) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM3:CCPxM0**: CCP Module x Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCP module)
0001 = Reserved
0010 = Compare mode, toggle output on match (CCPIF bit is set)
0011 = Reserved
0100 = Capture mode, every falling edge
0101 = Capture mode, every rising edge
0110 = Capture mode, every 4th rising edge
0111 = Capture mode, every 16th rising edge
1000 = Compare mode: initialize CCP pin low; on compare match, force CCP pin high (CCPxIF bit is set)
1001 = Compare mode: initialize CCP pin high; on compare match, force CCP pin low (CCPxIF bit is set)
1010 = Compare mode: generate software interrupt on compare match (CCPxIF bit is set, CCP pin reflects I/O state)
1011 = Compare mode: trigger special event, reset timer, start A/D conversion on CCP2 match (CCPxIF bit is set)
11xx = PWM mode

Types of detected events

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

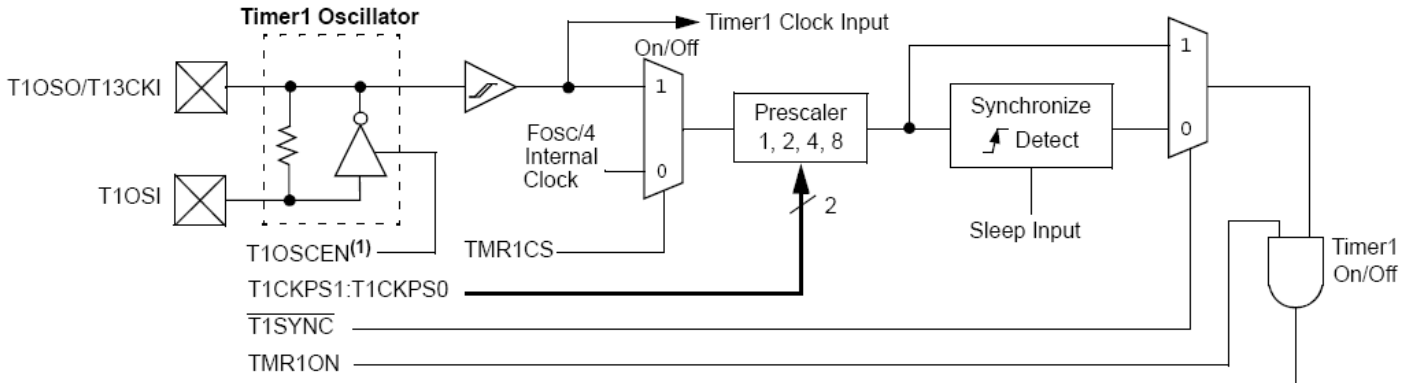
CCP Module Timers, Timer 1

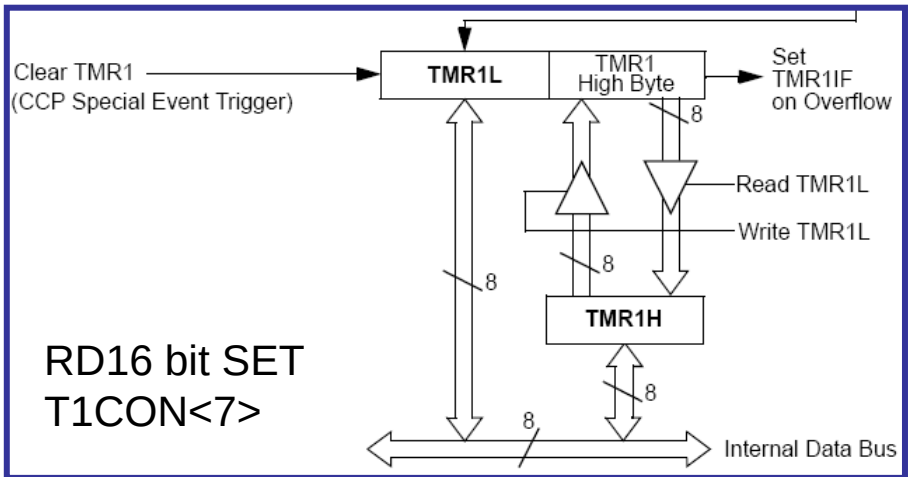
CHARACTERISTICS

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR1H and TMR1L)
- Selectable clock source (internal or external) with device clock or TMR1 oscillator internal option
- Interrupt-on-overflow
- **Reset on CCP Special Event Trigger**
- Device clock status flag (T1RUN)

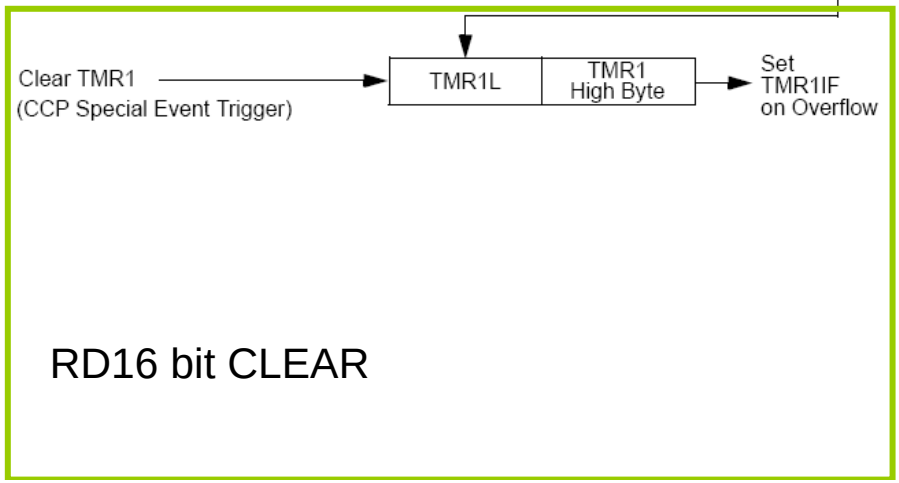
SCHEMATIC

(see **T1CON** in Data Sheet)





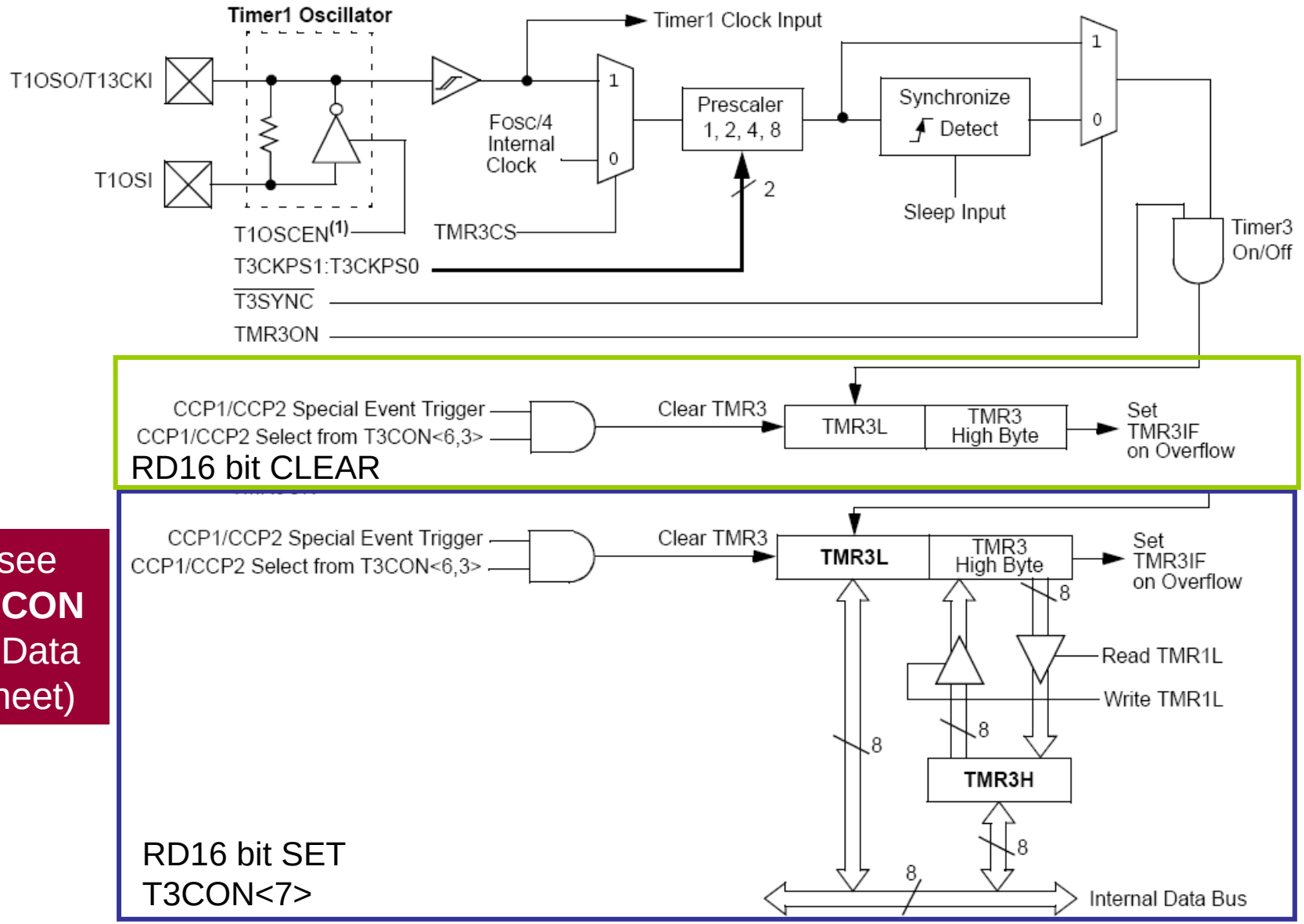
RD16 bit SET
T1CON<7>



RD16 bit CLEAR

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

CCP Module Timers, Timer 3



(see **T3CON** in Data Sheet)

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

CCP Module Timers, Capture Combination

- Employs Timer 1 or Timer 3 (16 bit timer/counter)
- Event on Pin: Rising Edge, Falling Edge, 4x or 16x rising edges
- After capture event, interrupt flag is set.

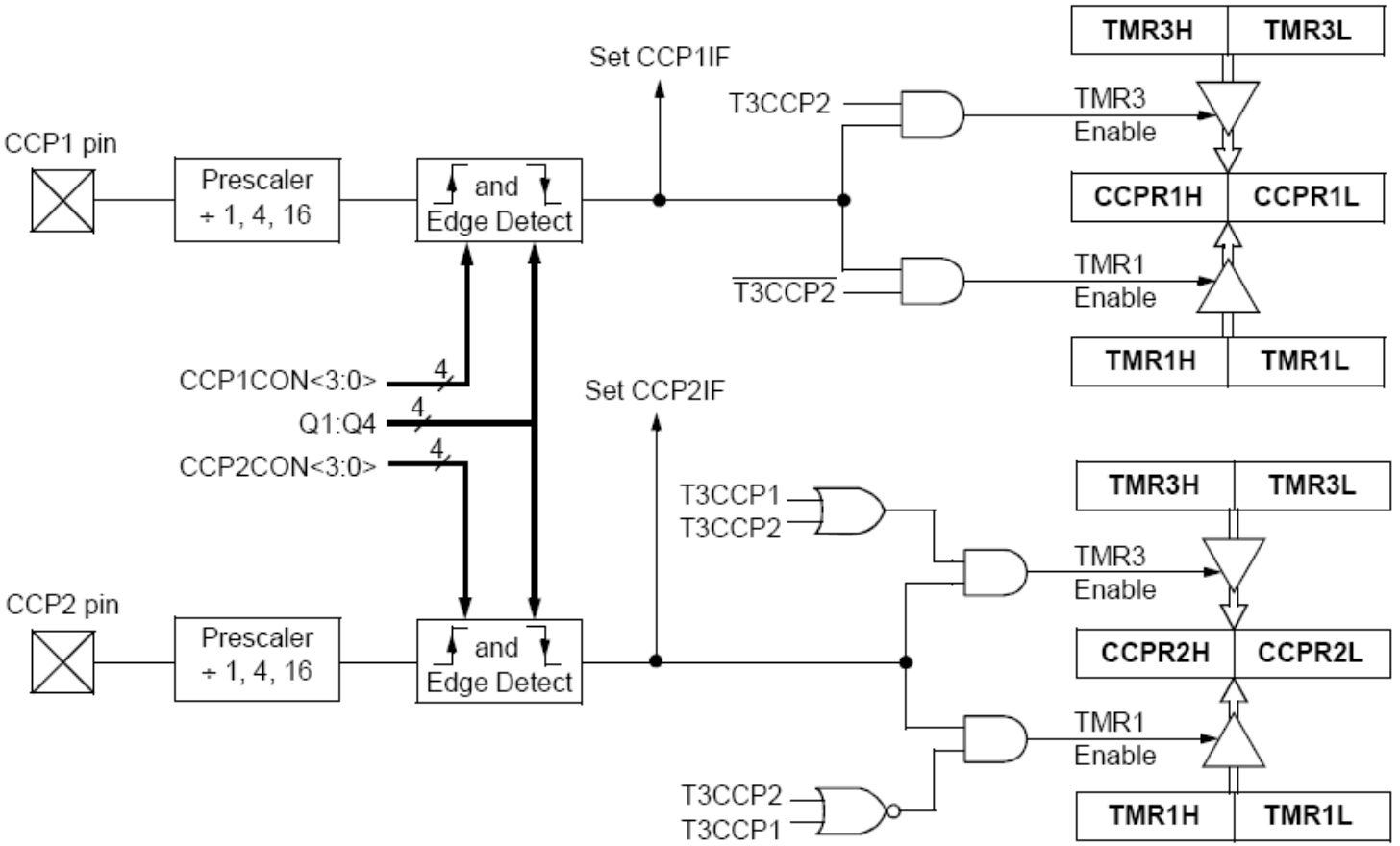


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

CCP Module Timers, Compare Combination

- Employs Timer 1 or Timer 3 (16 bit timer/counter)
- Compares CCPRx with the Timer counter content. Upon coincidence, the associated pin can either be inverted, set high, clear low, does not change
- Upon coincidence, and interrupt flag is set high.
- Timer can be Reset

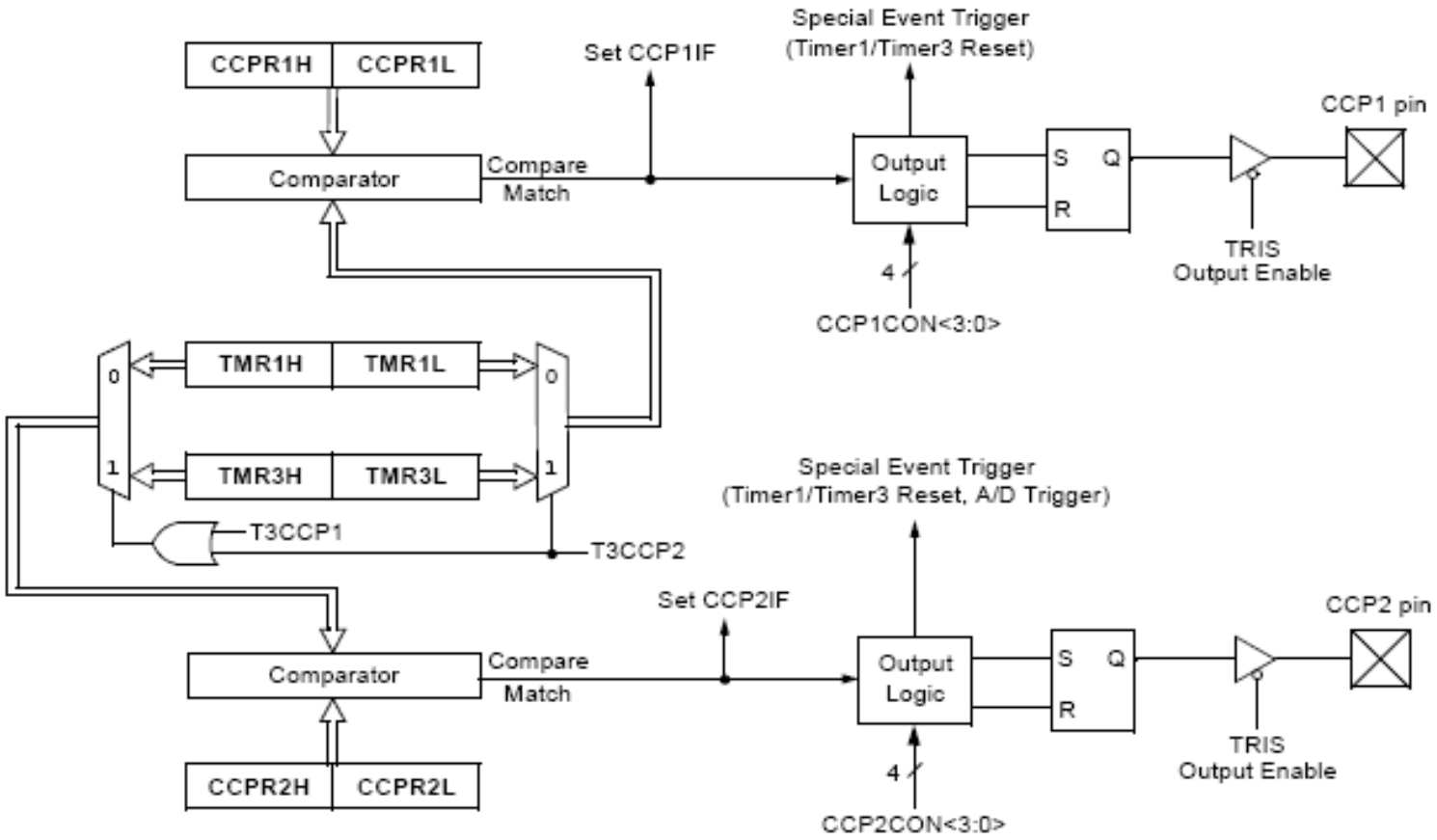


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

CCP Module, Associated Registers

TABLE 15-3: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1 AND TIME

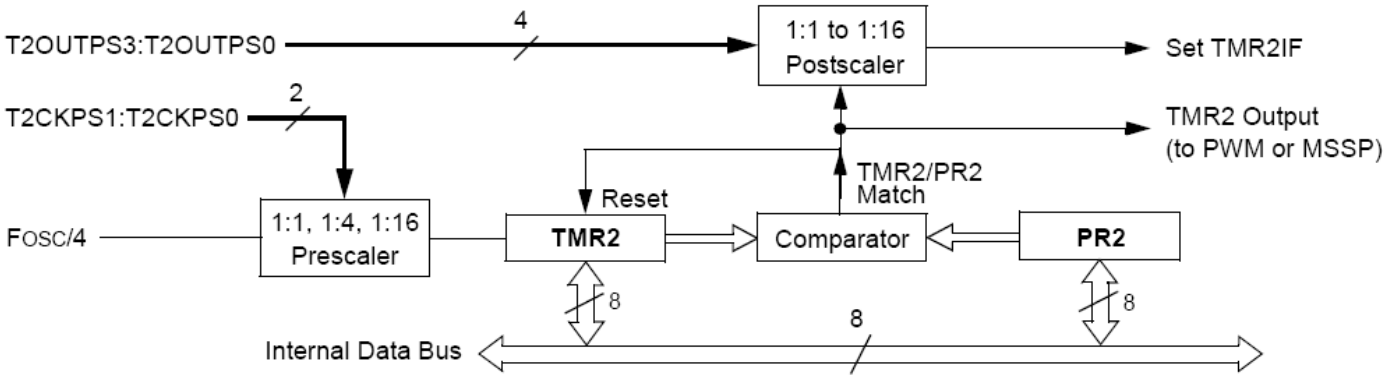
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
RCON	IPEN	SBOREN(1)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
PIR1	PSPIF(2)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
PIE1	PSPIE(2)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
IPR1	PSPIP(2)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP
PIR2	OSCFIF	CMIF	—	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF
PIE2	OSCFIE	CMIE	—	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE
IPR2	OSCFIP	CMIP	—	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP
TRISB	PORTB Data Direction Control Register							
TRISC	PORTC Data Direction Control Register							
TMR1L	Timer1 Register Low Byte							
TMR1H	Timer1 Register High Byte							
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON
TMR3H	Timer3 Register High Byte							
TMR3L	Timer3 Register Low Byte							
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYNC}$	TMR3CS	TMR3ON
CCPR1L	Capture/Compare/PWM Register 1 Low Byte							
CCPR1H	Capture/Compare/PWM Register 1 High Byte							
CCP1CON	P1M1(2)	P1M0(2)	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
CCPR2L	Capture/Compare/PWM Register 2 Low Byte							
CCPR2H	Capture/Compare/PWM Register 2 High Byte							
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

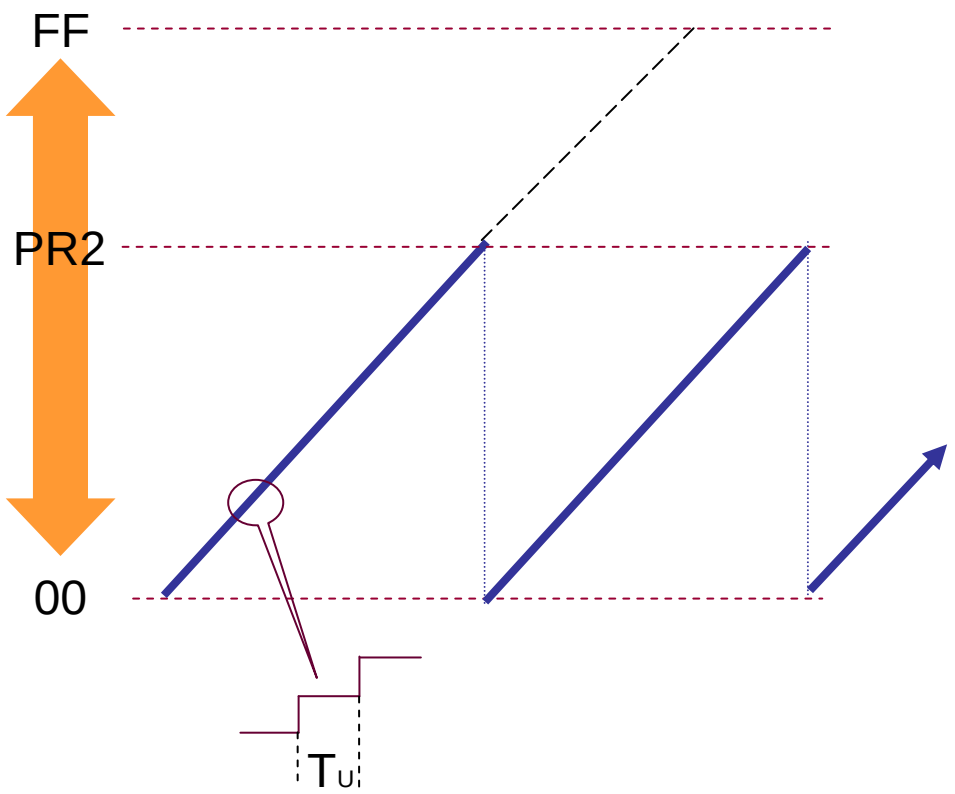
CCP Module Timers, Timer 2

CHARACTERISTICS

- 8-bit timer and period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- **Interrupt on TMR2-to-PR2 match**
- Optional use as the shift clock for the MSSP module



CCP Module Timers, Timer 2



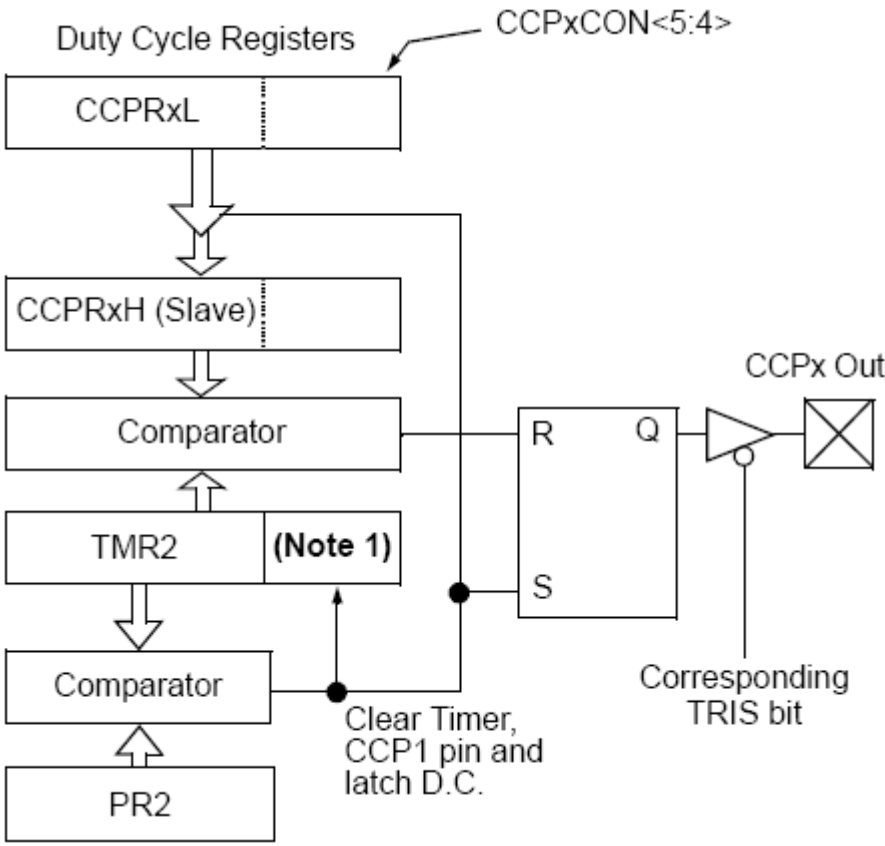
REGISTERS

INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF
PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
IPR1	PSPIP(1)	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP
TMR2	Timer2 Register							
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
PR2	Timer2 Period Register							

(see **T2CON** in Data Sheet)

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

CCP Module Timers, Compare Combination



When TMR2 equals PR2:

1. TMR2 Reset
2. CCPx module pin set **HIGH**
3. Reload CCPRxH with CCPRxL content

CCPx module pin is set **LOW** when CCPRxH = TMR2

CCP Module Timers, Compare Combination

- Time base is established by Timer 2

- **PWM Period** given by PR2 register (8 bits)
  PWM Period = [(PR2)+1]·4·Tosc·(PMR2 Prescale value)

- **PWM DC** set by **CCPRxL** : **CCPxCON<5:4>** (10 bit resolution)
  PWM DC = (CCPRxL:CCPxCON<5:4>)·Tosc·(PMR2 Prescale value)

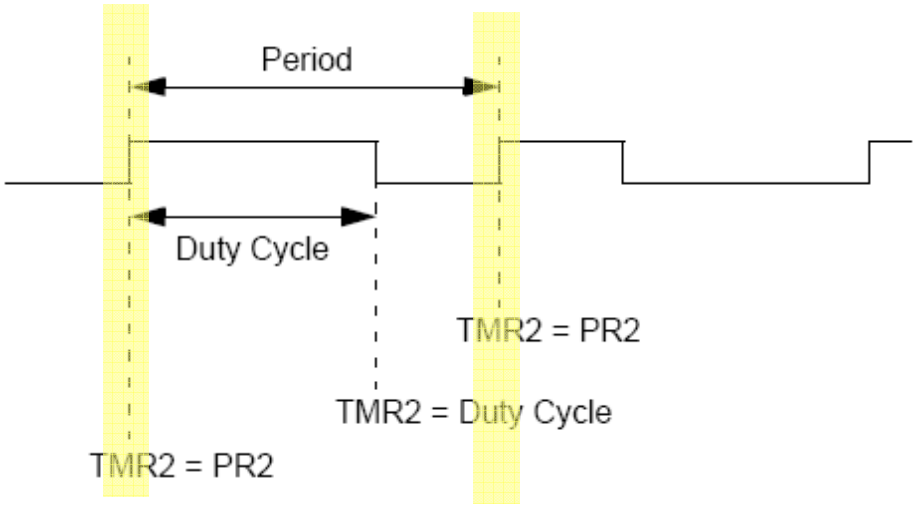


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

CCP Module, Interactions

TABLE 15-2: INTERACTIONS BETWEEN CCP1 AND CCP2 FOR TIMER RESOURCES

CCP1 Mode	CCP2 Mode	Interaction
Capture	Capture	Each module can use TMR1 or TMR3 as the time base. The time base can be different for each CCP.
Capture	Compare	CCP2 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Automatic A/D conversions on trigger event can also be done. Operation of CCP1 could be affected if it is using the same timer as a time base.
Compare	Capture	CCP1 can be configured for the Special Event Trigger to reset TMR1 or TMR3 (depending upon which time base is used). Operation of CCP2 could be affected if it is using the same timer as a time base.
Compare	Compare	Either module can be configured for the Special Event Trigger to reset the time base. Automatic A/D conversions on CCP2 trigger event can be done. Conflicts may occur if both modules are using the same time base.
Capture	PWM(1)	None
Compare	PWM(1)	None
PWM(1)	Capture	None
PWM(1)	Compare	None
PWM(1)	PWM	Both PWMs will have the same frequency and update rate (TMR2 interrupt).