Microprocessor based digital Systems

The Analog Converter

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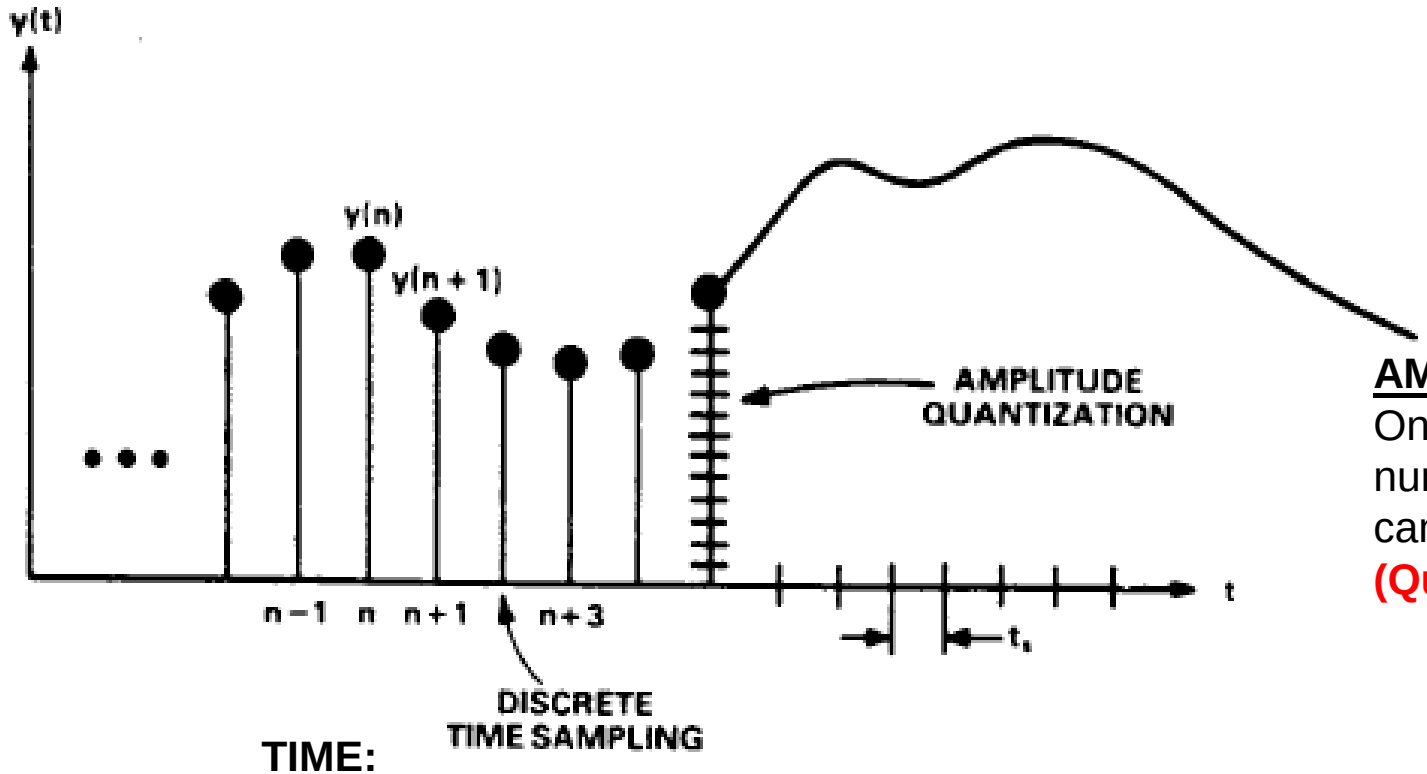
Analog World, Digital World

Discretization Process



AMPLITUDE:
Only a discrete number of values can be represented **(Quantification)**

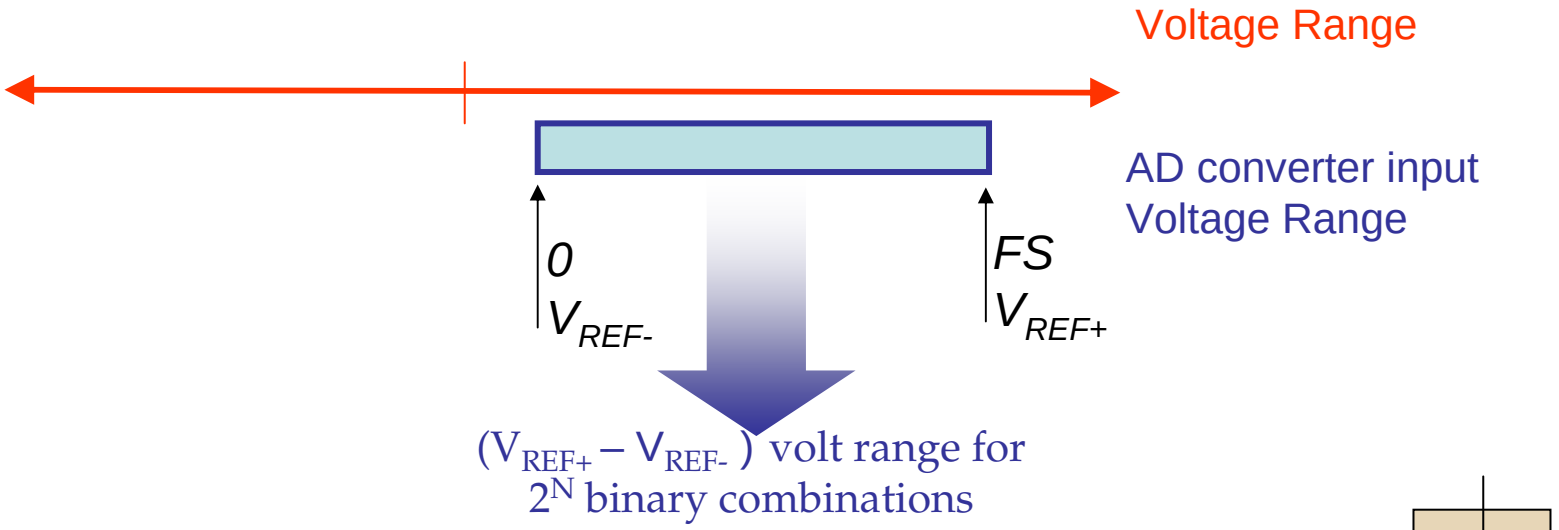
TIME:
Only the value at fixed time instants can be taken **(Sampling)**

Figure from "Fundamentals of Sampled Data Systems"
Application Note AN-282
Analog Devices

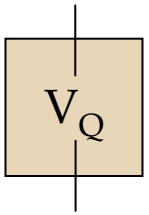
AD Conversion, Amplitude

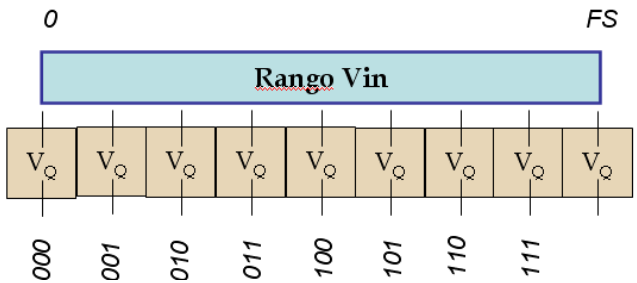
RESOLUTION:

Voltage is represented by a fixed number of bits N, having just 2^N different combinations available to represent **2^N different voltage levels**



Quantification Voltage $V_Q = (V_{REF+} - V_{REF-}) / 2^N$ = 1 LSB

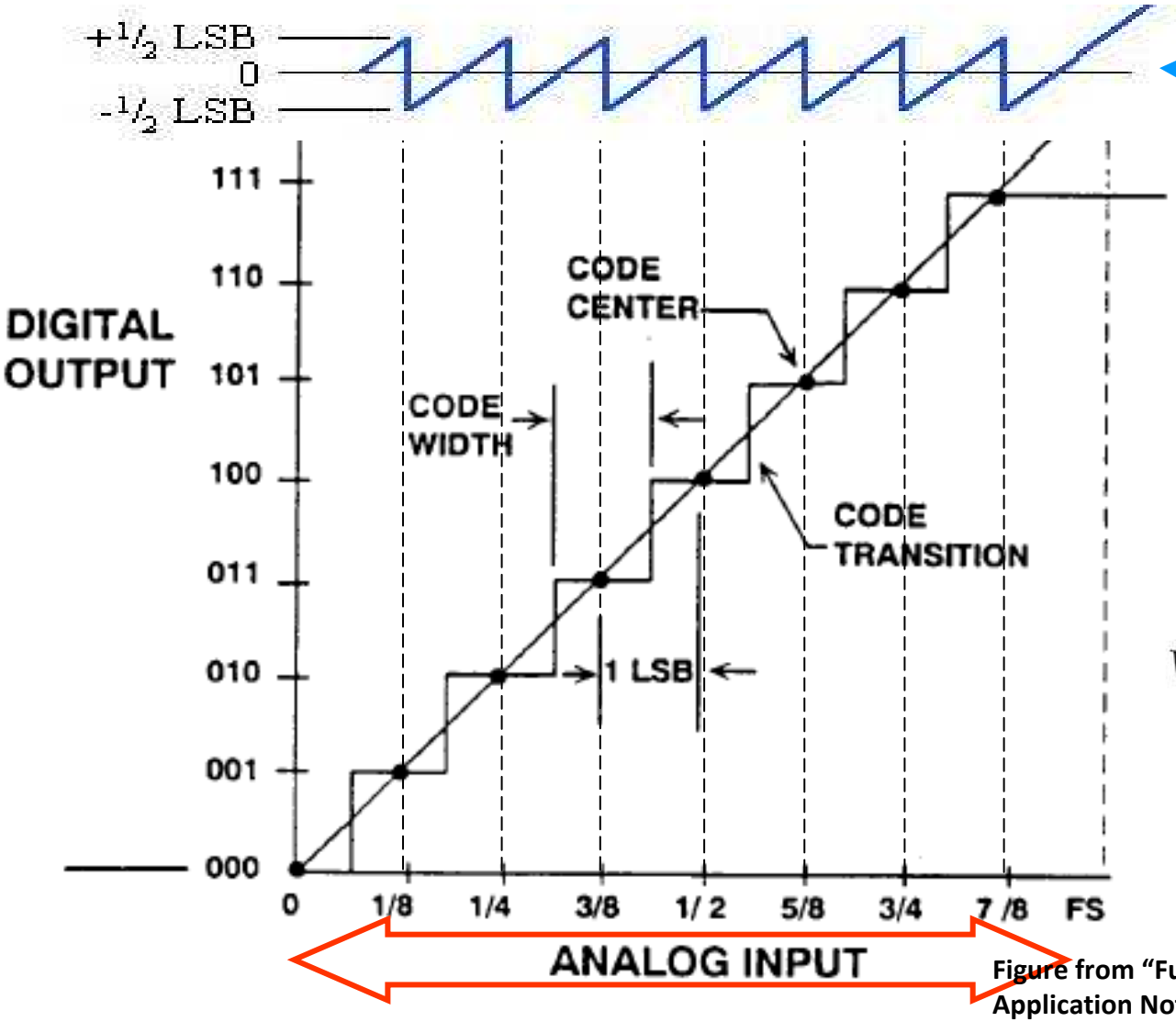




(Quantification)

AD Conversion, Amplitude Error

AD transfer function with N = 3:

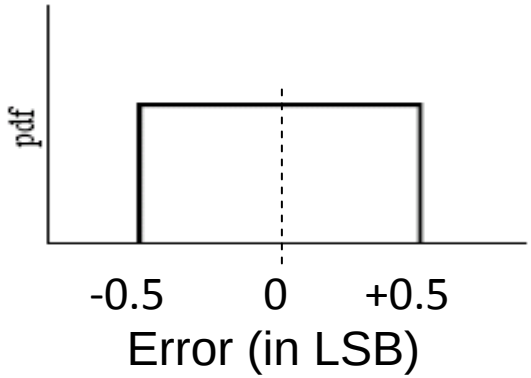


Quantification Error

$$V_{IN} = V_Q \sum_{k=0}^{N-1} b_k 2^k + \epsilon$$

Figure from "Fundamentals of Sampled Data Systems"
Application Note AN-282
Analog Devices

AD Conversion, Amplitude Error Effect



$$\mathrm{SNR} = 20\log\left(\frac{V_{\mathrm{rms}}}{\sqrt{E(\epsilon^2)}}\right) = 20\log(2^N\sqrt{1.5}) = 6.02N + 1.76 \text{ dB}$$

resolution	signal-to-noise ratio
6 bits	37.9 dB
8 bits	49.9 dB
10 bits	62.0 dB
12 bits	74.0 dB
14 bits	86.0 dB
16 bits	98.1 dB

AD Conversion, Time

Sample and Hold:

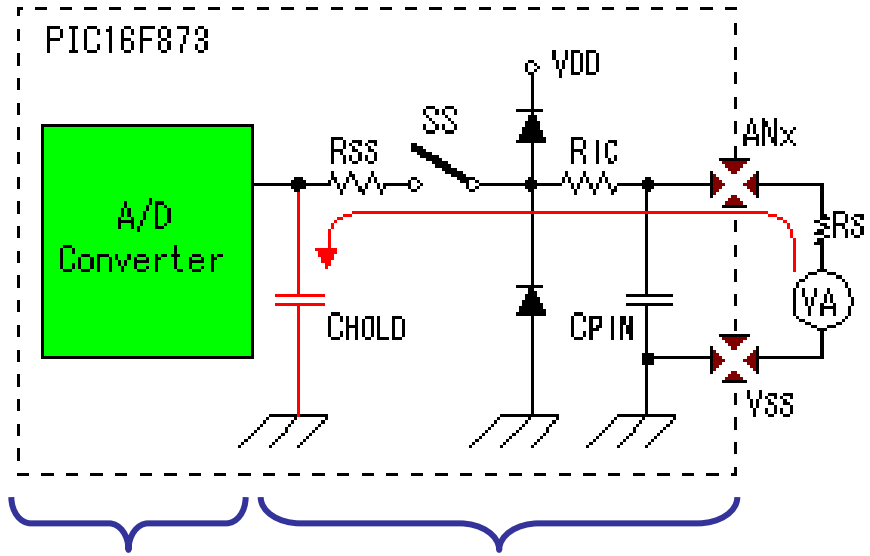
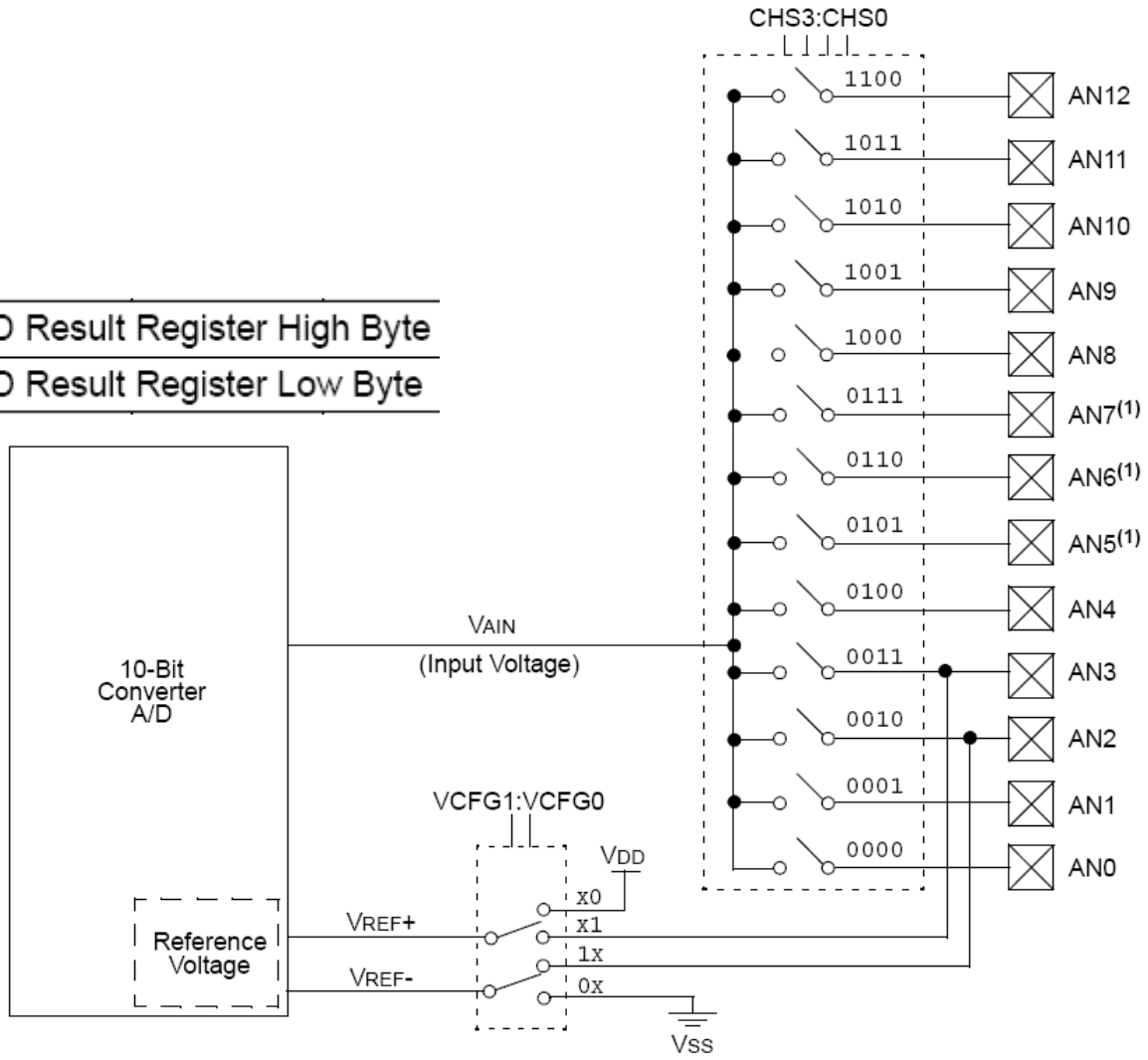


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

AD Module, Block Diagram

ADCON0
ADCON1
ADCON2

ADRESH	A/D Result Register High Byte
ADRESL	A/D Result Register Low Byte



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
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AD Module, Control Registers

REGISTER 19-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

AD Module, Control Registers

REGISTER 19-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented(2)
1110 = Unimplemented(2)
1111 = Unimplemented(2)

Note 1: These channels are not implemented on 28-pin devices.

2: Performing a conversion on unimplemented channels will return a floating input measurement.

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
0 = A/D converter module is disabled

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
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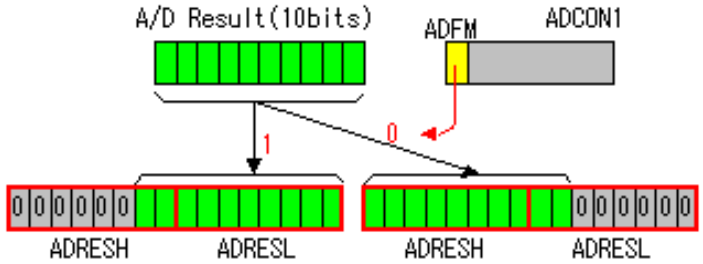
AD Module, Control Registers

REGISTER 19-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0



bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as ‘0’

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

Acquisition Time

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

T_{AD}

Conversion Time

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
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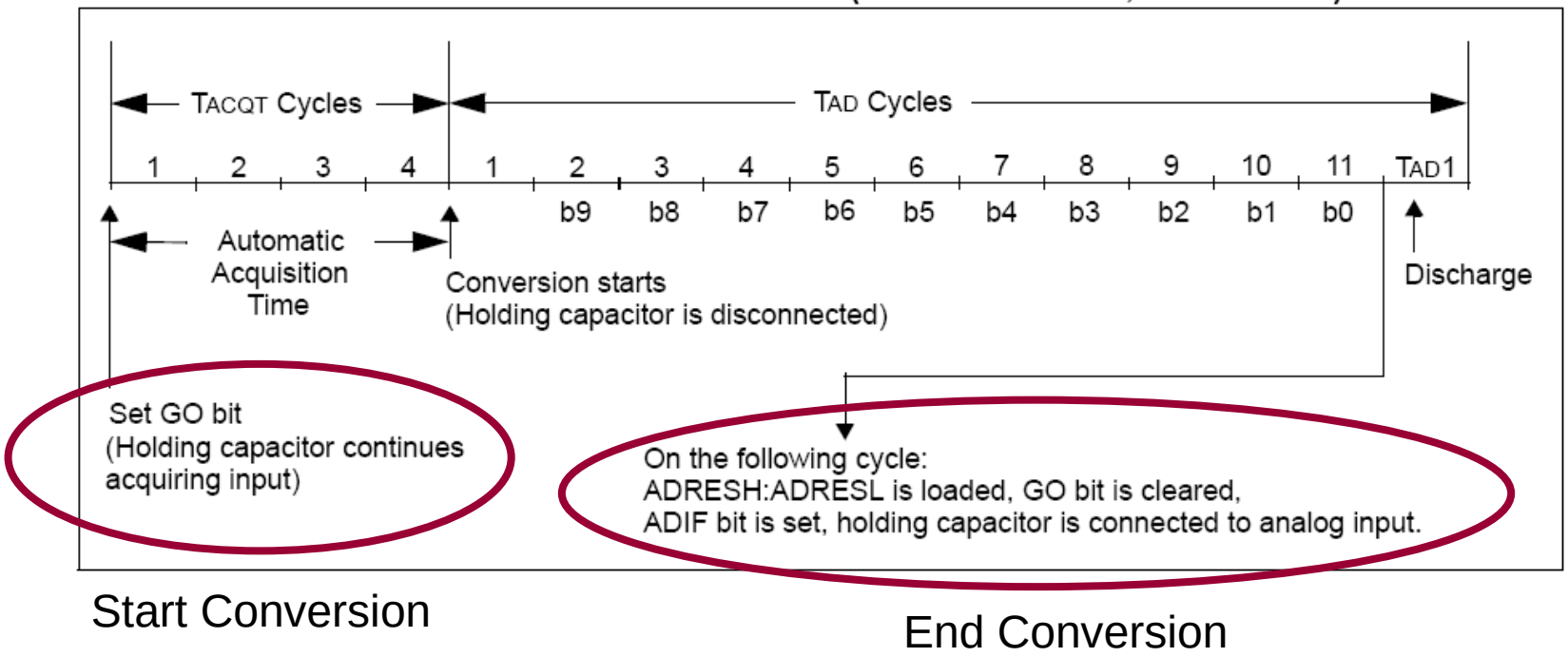
AD Module, Time between samples

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 10-bit conversion.

FIGURE 19-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



Start Conversion

End Conversion

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
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AD Module, Time between samples

T_{AD}

For correct A/D conversions, the A/D conversion clock (T_{AD}) must be as short as possible, but greater than the minimum T_{AD} (see parameter 130 for more information).

T_{ACQ}

EQUATION 19-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$

$T_{AMP} = 0.2\ \mu s$

$T_{COFF} = (Temp - 25°C)(0.02\ \mu s/°C)$
$(85°C - 25°C)(0.02\ \mu s/°C)$
$1.2\ \mu s$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, T_{COFF} = 0 ms.

$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S)\ \ln(1/2047)$
$-(25\ pF)\ (1\ k\Omega + 2\ k\Omega + 2.5\ k\Omega)\ \ln(0.0004883)$
$1.05\ \mu s$

$T_{ACQ} = 0.2\ \mu s + 1\ \mu s + 1.2\ \mu s$
$2.4\ \mu s$

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
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AD Module, Conversion Steps

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0 register)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

AD Module, C18 Libraries

Funcion	Description
BusyADC	Is there a sample being taken?
CloseADC	Turn off ADC module
ConvertADC	Start a new conversion
OpenADC	Configure the ADC module
ReadADC	Reads a sample
SetChanADC	Select the input channel