Microprocessor based digital Systems

Serial Communications: USART

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Communication Standards

Standard Serial Comm Protocols

Interface	Format	Num. Devices	Separation max.	Transm Speed (bits/seg)
RS-232	Serial Asinc.	2	15 – 30 m	20k
IrDA	Serial Asinc.	2	2 m	115k
SPI	Serial Sinc.	8	3 m	2.1M
I2C	Serial Sinc.	40	5.5 m	400k
USB	Serial Asinc.	127	5 m	12M

Serial Comms, Fundamentals

Serial Communication Characteristics

The physical layer can only transport one bit at a time.

It is used when the transmission takes place further than a few meters.

Requires complex controllers and protocols:

- Transmitter must turn bytes into bits
- Receiver must turn bits into bytes

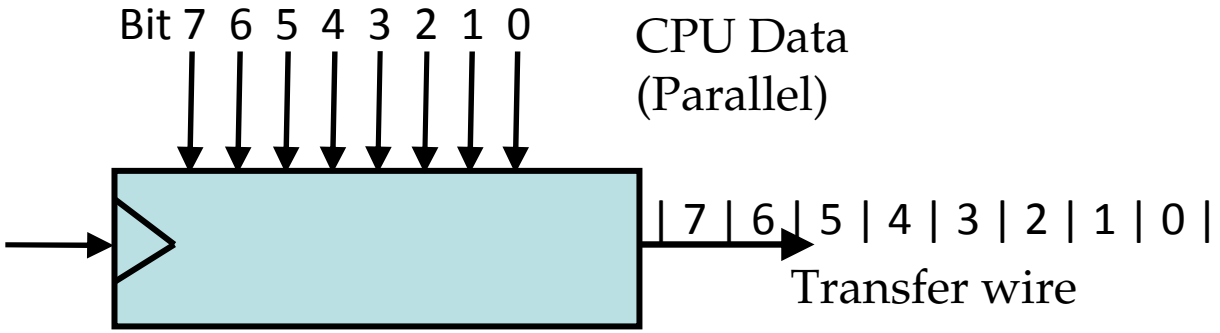
The transfer speed is the BAUD (= bits/seg).

Serial Comms, Fundamentals

Key element

Function to perform: PARALLEL to SERIAL converter

Key component: Shift Register



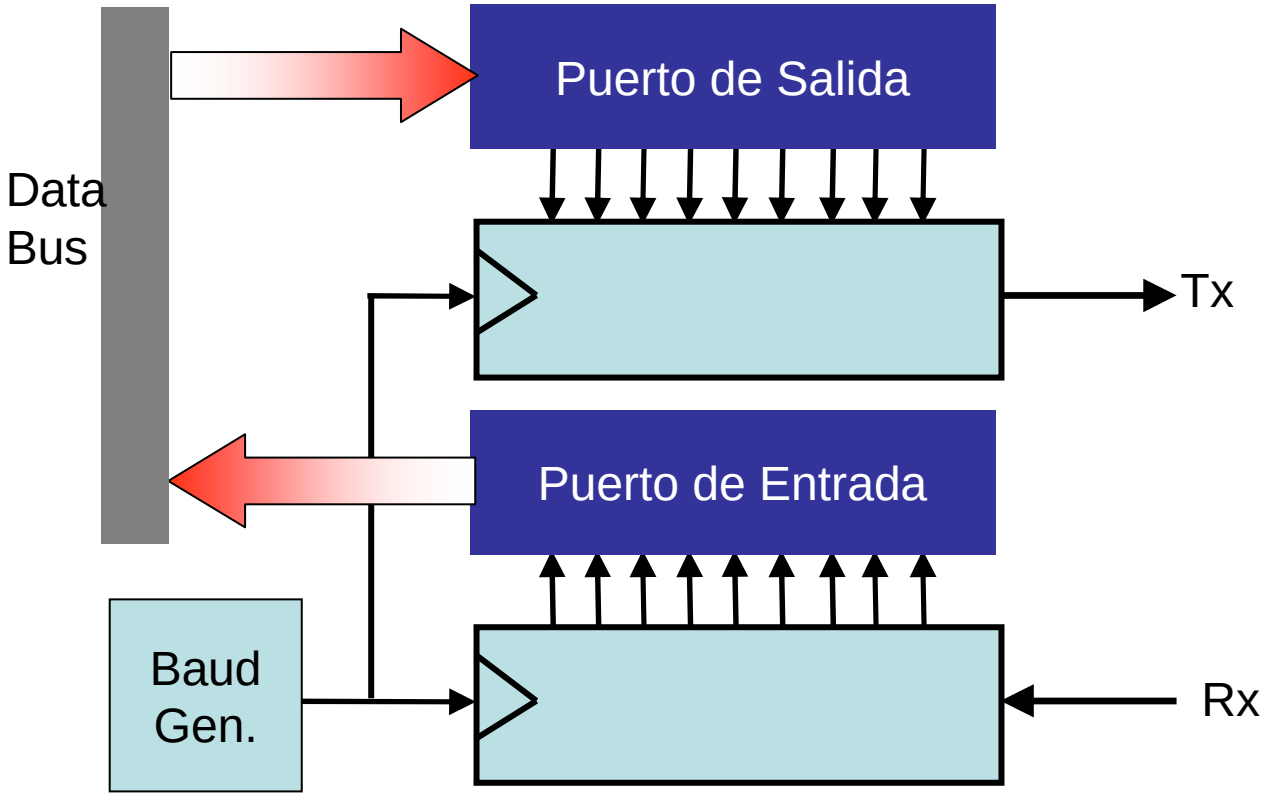
Output Port (Transmitter)
unidirectional !!!

The **information unit** is the *character*, no the byte.

Serial Comms, Fundamentals

Serial Comm Peripheral

UART, Universal Asynch Rx Tx

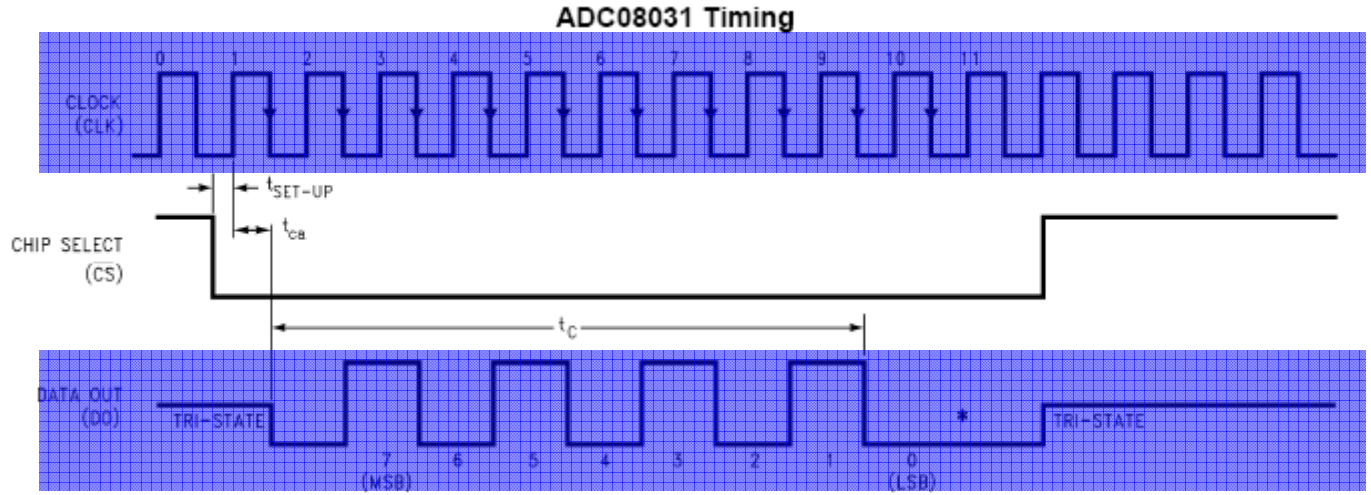


Serial Comms, Fundamentals

Serial Comm Types

Asynchronous

Synchronous



Serial Comms, USART

(USART)Universal Synchronous Asynchronous Receiver Transmitter

Modes:

- **Synch: Employs an independent clock line**
- **Asynch: Clock is within the data**

Microchip PIC USART characteristics:

- **Transmits & receives serial data (8 or 9 bits)**
- **Error detection**
- **Interrupt sources**
- **Input & Output buffers**

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

Serial Comms, USART

Register Name	Description
TXREG	Transmit Data Register
RCREG	Receive Data Register

Register Name	Description
TXSTA	Transmit Status and Control
RCSTA	Receive Status and Control

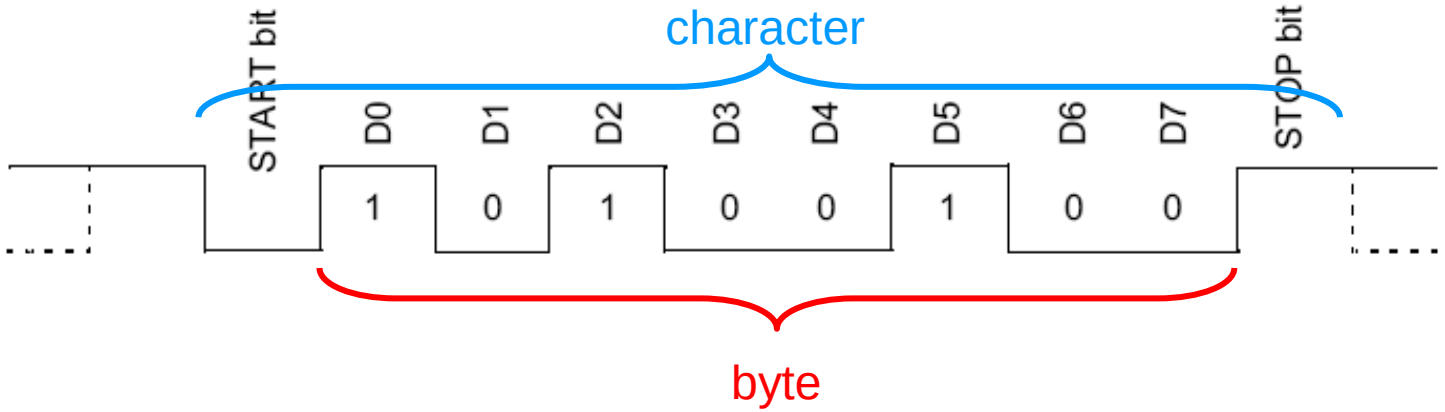
Register Name	Description
SPBRG	Baud Rate Generator

Register Name	Description
INTCON	Interrupt Control Register
RCON	RESET Control Register
PIE1, PIE3	Peripheral Interrupt Enable Registers
PIR1, PIR3	Peripheral Interrupt Flag Registers
IPR1, IPR3	Peripheral Interrupt Priority Registers

Serial Comms, Asynchronous Comms

Synchronization is achieved by:

- Fixed transfer speed at fixed rates
- Start / Stop bits



Characteristics:

- Idle state of the line in HIGH level
- Start bit: Negate idle state level
- Transmission starts by the LSB
- Stop bit: last bit, same state as Idle

Serial Comms, Asynchronous Comms

Configurable parameters:

- Transfer Data Rate
- Data (8 or 9 bits) Ninth bit parity use
- Stop bit duration: **1 Tb**, 1.5 Tb, **2 Tb**

Even
Odd
Mark
Space

Data Config Options on the PIC:

8 bits Stop Bits: 1
8 bits Stop Bits: 2
9 bits Stop Bits: 1

Parity is left to the programmer

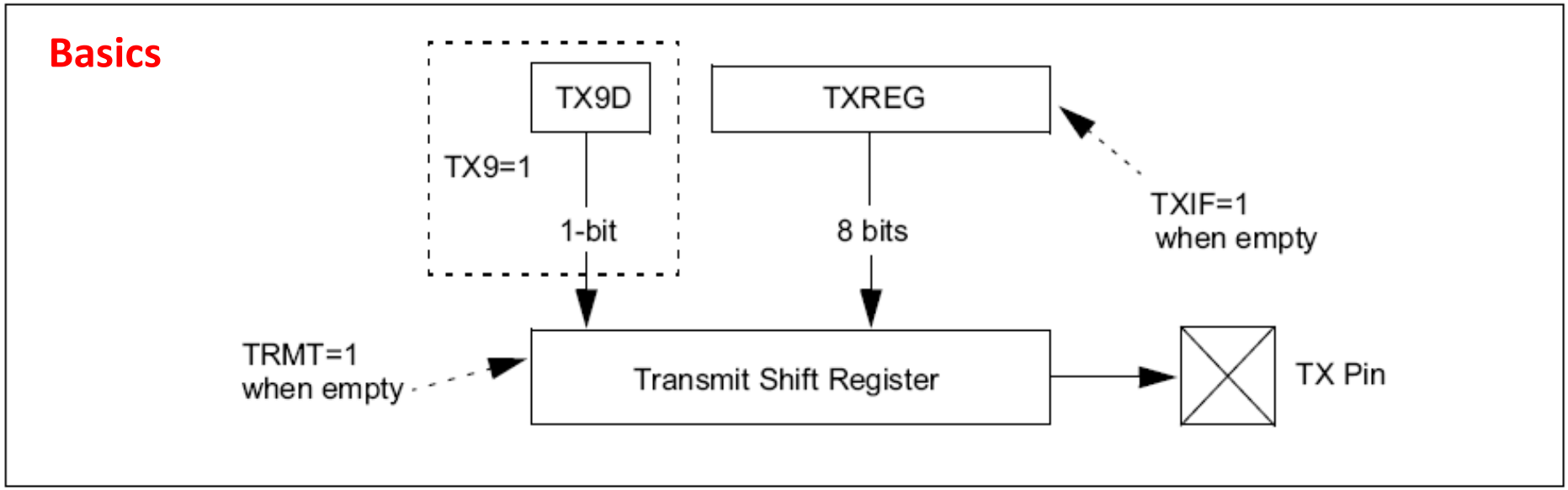
Speed Config Options:

- Register SPBRG (Serial Peripheral Baud Rate Generator)
- Bit BRGH: High speed bit
- Bit BRG16: 16bit operation for SPBRG

Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

Serial Comms, Asynchronous Transmission

Basics



Important issues

- In 9 bit transmission, TX9D must be written previously toTXREG
- TXREG can be written while peripheral is transmitting (2 level FIFO)
- There is a delay from writting to TXREG and clearing TXIF

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

Serial Comms, Asynchronous Transmission

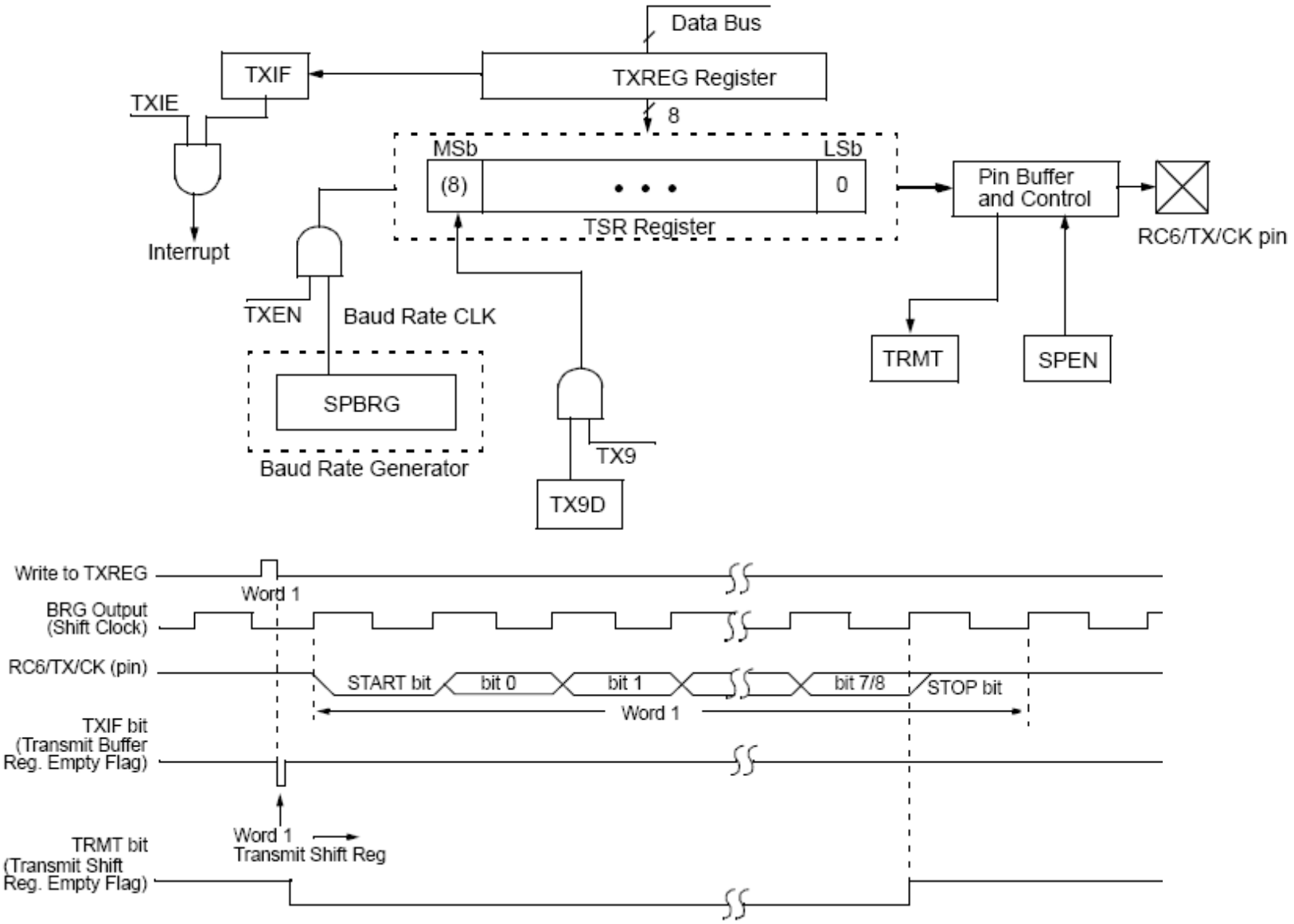


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

Serial Comms, Asynchronous Transmission Config

REGISTER 18-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled
Note: SREN/CREN overrides TXEN in Sync mode.

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

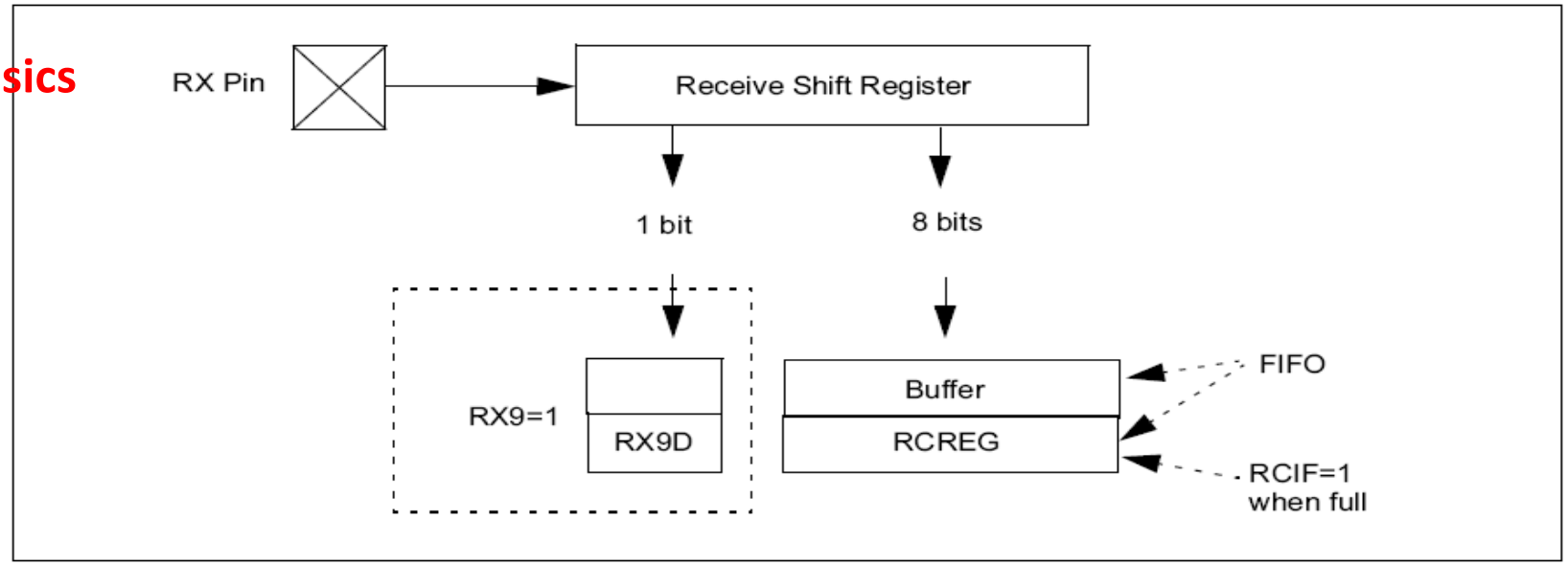
bit 0 **TX9D:** 9th bit of Transmit Data
Can be address/data bit or a parity bit.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

Serial Comms, Asynchronous Reception

Basics



Important issues

- Reception starts upon detection of a START bit
- Transmission integrity is checked testing STOP bit level
- Received data in Shift register is stored in FIFO (One single address, RCREG)
- If thee characters are received in a row, FIFO overflows ➔ Overrun error
- RCIF is set HIGH until FIFO is empty

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
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Serial Comms, Asynchronous Reception

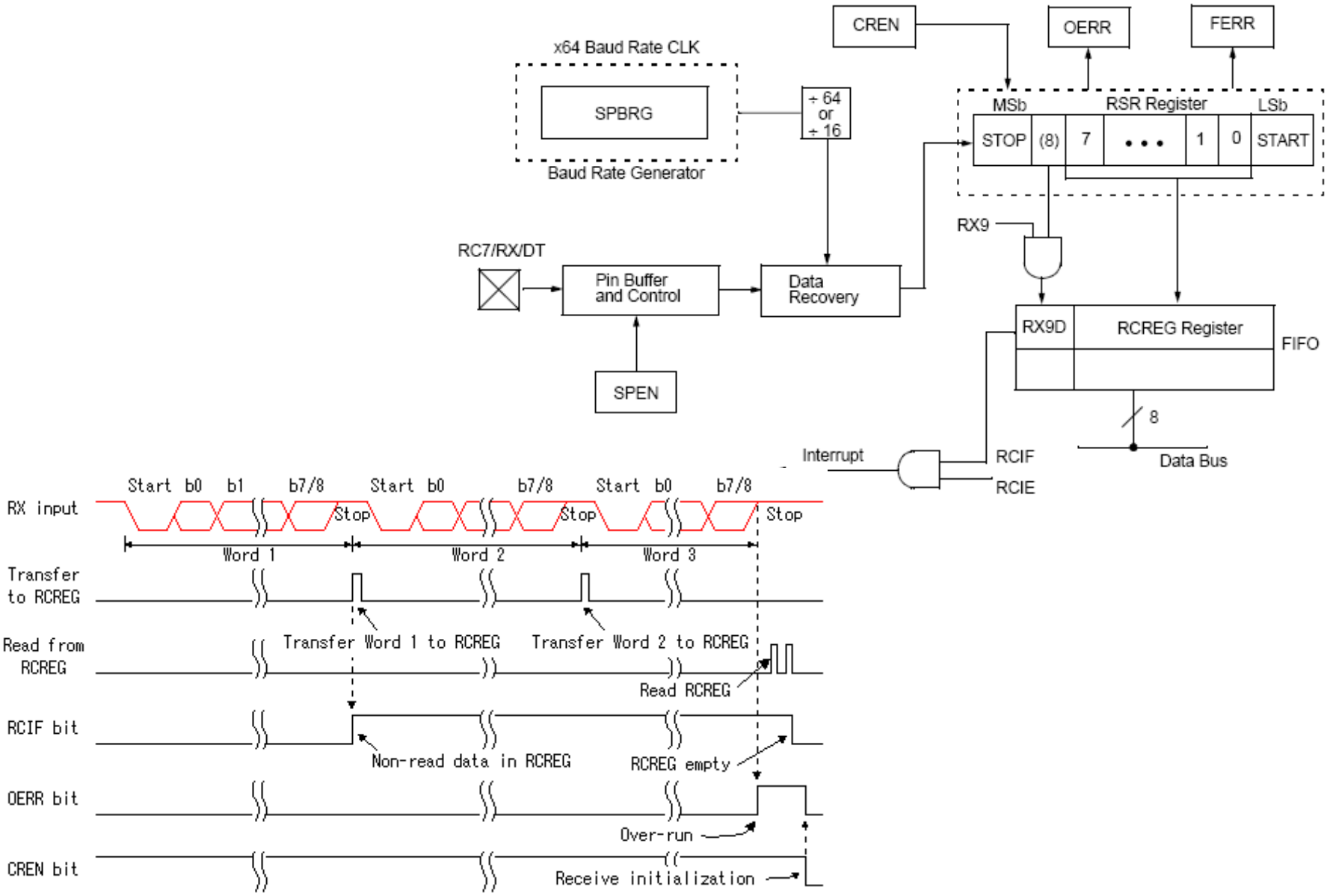


Figura del “PIC18F2525/2620/4525/4620 Data Sheet”
Con permiso de MICROCHIP

Serial Comms, Asynchronous Reception Config

REGISTER 18-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

bit 7 **SPEN**: Serial Port Enable bit
1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled (held in Reset)

bit 6 **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN**: Single Receive Enable bit
Asynchronous mode:
Don't care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don't care.

bit 4 **CREN**: Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN**: Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode 9-bit (RX9 = 0):
Don't care.

bit 2 **FERR**: Framing Error bit
1 = Framing error (can be updated by reading RCREG register and receiving next valid byte)
0 = No framing error

bit 1 **OERR**: Overrun Error bit
1 = Overrun error (can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D**: 9th bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figura del "PIC18F2525/2620/4525/4620 Data Sheet"
Con permiso de MICROCHIP

Serial Comms, Asynchronous Transmission Config

TABLE 18-1: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	Fosc/[64 (n + 1)]
0	0	1	8-bit/Asynchronous	Fosc/[16 (n + 1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	Fosc/[4 (n + 1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGH:SPBRG register pair

Example: With a 16 MHz oscillator, generate 9600 bauds

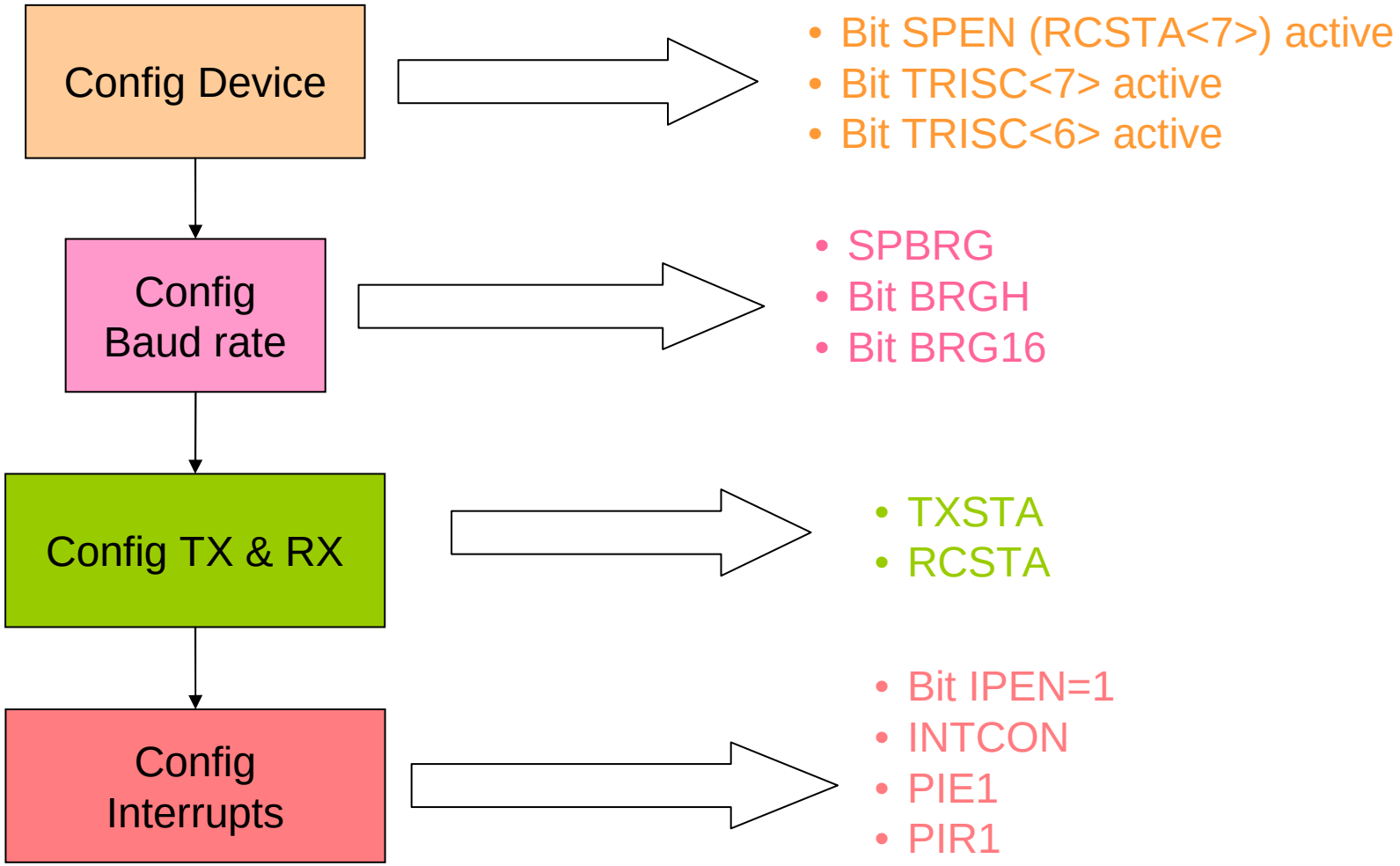
BRG16=0

BRGH = 1
SPBRG = 16000000/(16 x 9600) - 1 = 51.08 → 51 ➔ Baud Rate= 9615.33 baud
BRGH = 0
SPBRG = 16000000/(64 x 9600) - 1 = 12.02 → 12 ➔ Baud Rate= 9615.38 baud

BRG16=1

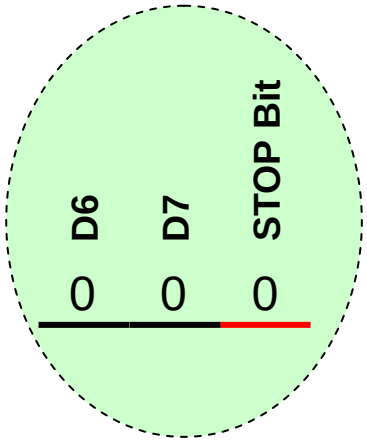
BRGH = 0
SPBRG = 16000000/(16 x 9600) - 1 = 51.08 → 51 ➔ Baud Rate= 9615.33 baud
BRGH = 1
SPBRG = 16000000/(4 x 9600) - 1 = 415.67 → 416 ➔ Baud Rate= 9592.33 baud

Serial Comms, Recommended Initialization

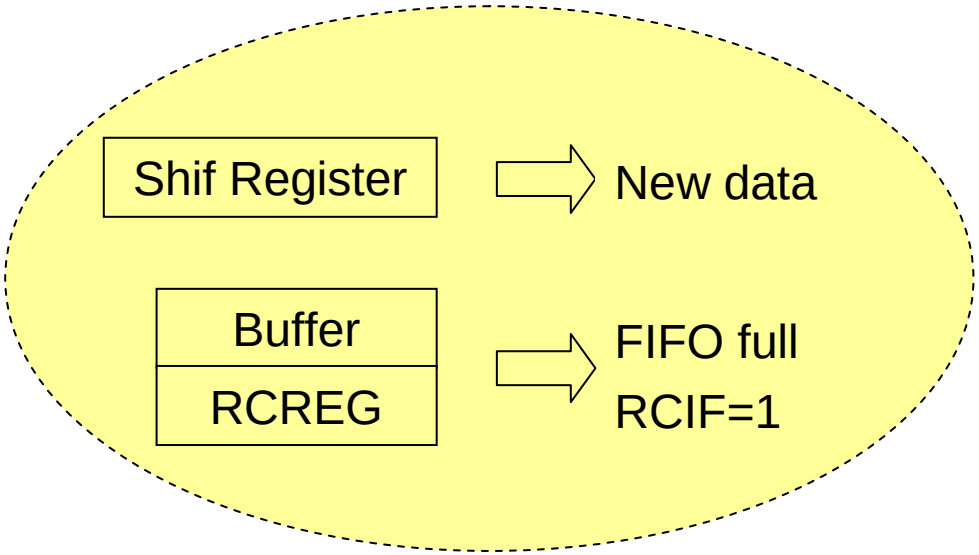


Serial Comms, Detected Errors

Framing Error
FERR=1



Overrun Error
OERR=1



HOMEWORK: Which of the following are error correction or detection schemes? Explain the basic of each one.

- Parity Bit
- CRC
- Checksum

RS232 Fundamentals

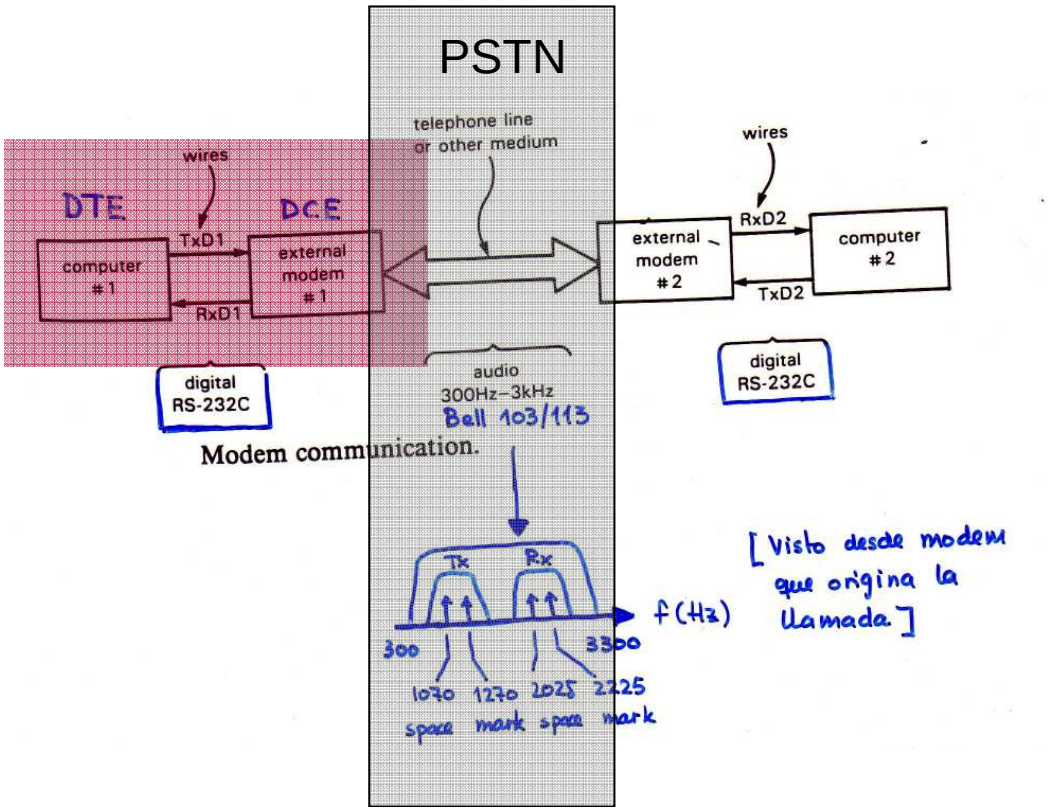
RS232 Standard

Origen del Standard RS232

Originally intended to comunicate a DTE system with a DCE systems.

DTE (Data Terminal Equipment) usually, a computer

DCE (Data Communications Equipment) usually, a modem



RS232 standard

Logical Level: Signals

Nombre	Dirección DTE ↔ DCE	Función	Comentario
TD	⇒	Transmitted data	Par de Datos
RD	⇐	Received Data	
RTS	⇒	Request to Send	Par de Handshake
CTS	⇐	Clear to Send	
DTR	⇒	Data Terminal Ready	Par de Handshake
DSR	⇐	Data Set Ready	
DCD	⇐	Data Carrier Detect	Habilitan DTE
RI	⇐	Ring Indicator	

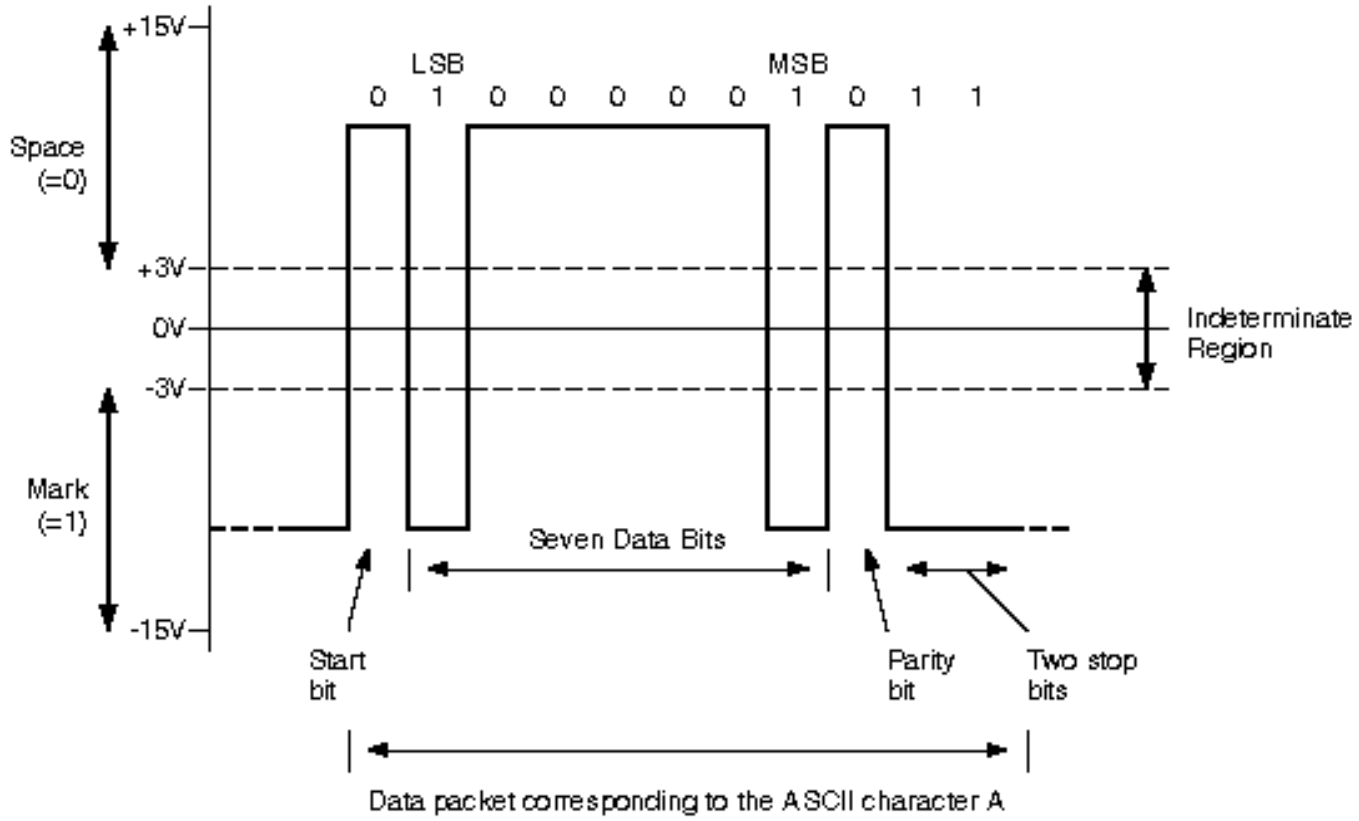
RS232 standard

Electrical Level: Specifications

Parameter		RS232	RS423
Mode of Operation		SINGLE -ENDED	SINGLE -ENDED
Total Number of Drivers and Receivers on One Line		1 DRIVER 1 RECVR	1 DRIVER 10 RECVR
Maximum Cable Length		50 FT.	4000 FT.
Maximum Data Rate		20kb/s	100kb/s
Maximum Driver Output Voltage		+/-25V	+/-6V
Driver Output Signal Level (Loaded Min.)	Loaded	+/-5V to +/-15V	+/-3.6V
Driver Output Signal Level (Unloaded Max)	Unloaded	+/-25V	+/-6V
Driver Load Impedance (Ohms)		3k to 7k	>=450
Max. Driver Current in High Z State	Power On	N/A	N/A
Max. Driver Current in High Z State	Power Off	+/-6mA @ +/-2v	+/-100uA
Slew Rate (Max.)		30V/uS	Adjustable
Receiver Input Voltage Range		+/-15V	+/-12V
Receiver Input Sensitivity		+/-3V	+/-200mV
Receiver Input Resistance (Ohms)		3k to 7k	4k min.

RS232 standard

Electrical Level: RS232 Signals



RS232 standard

Electrical Level: RS232 Drivers

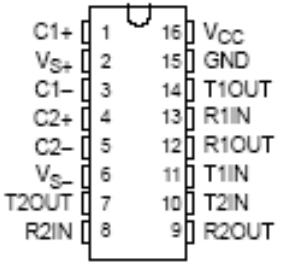
TTL a RS232
RS232 a TTL

MAX232, MAX232I
DUAL EIA-232 DRIVERS/RECEIVERS

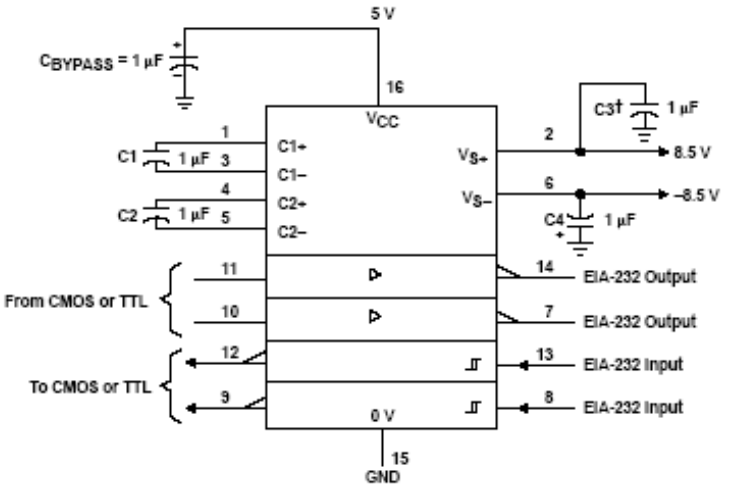
SLLS047I – FEBRUARY 1989 – REVISED OCTOBER 2002

- Meet or Exceed TIA/EIA-232-F and ITU Recommendation V.28
- Operate With Single 5-V Power Supply
- Operate Up to 120 kbit/s
- Two Drivers and Two Receivers
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)
- Applications
  - TIA/EIA-232-F
  - Battery-Powered Systems
  - Terminals
  - Modems
  - Computers

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)

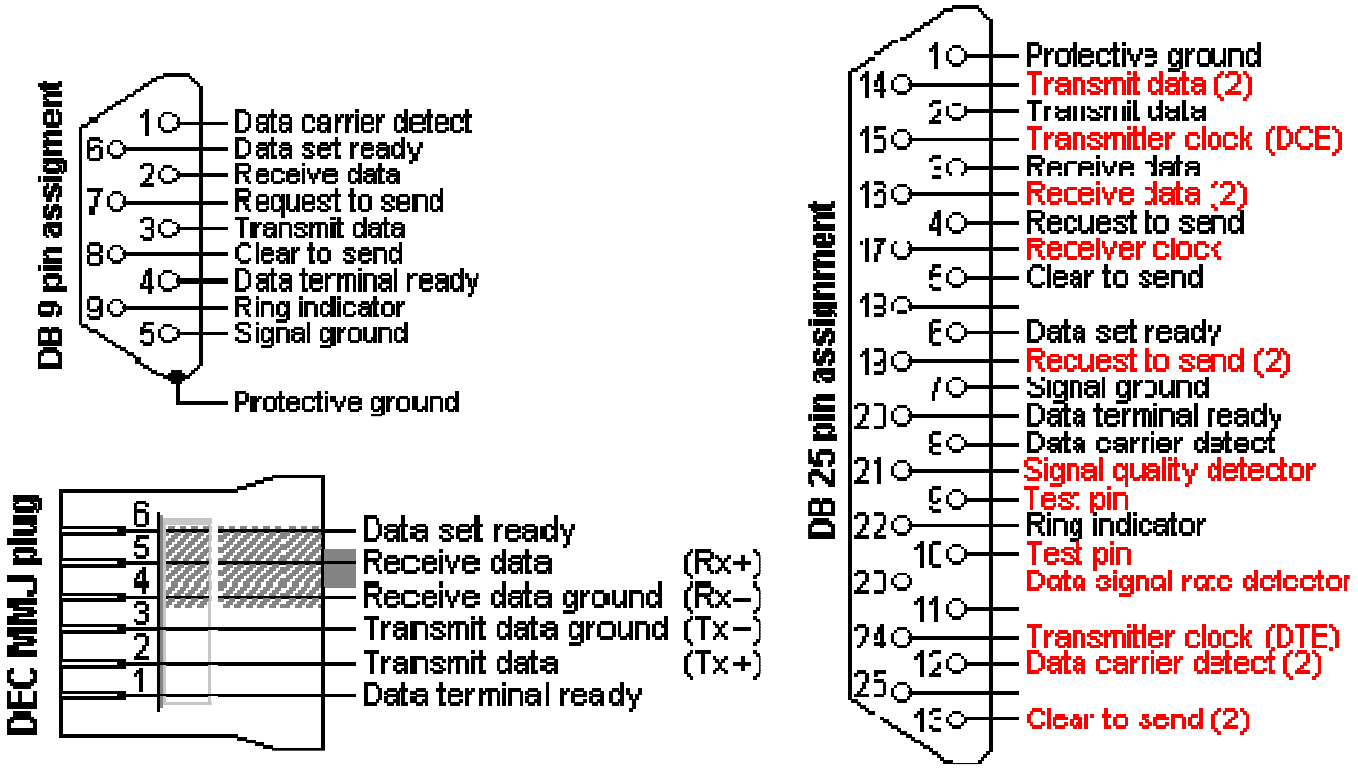


APPLICATION INFORMATION



RS232 standard

Mechanical Level: Connectors



RS232 standard

Null-Modem

To overcome the implementation of the logical protocol lines, and use exclusively the transmission pair, Tx y Rx