Universidad Carlos III de Madrid

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Session 27 – Case Study 2 Audio multiple-stage amplifier

Electronic Components and Circuits

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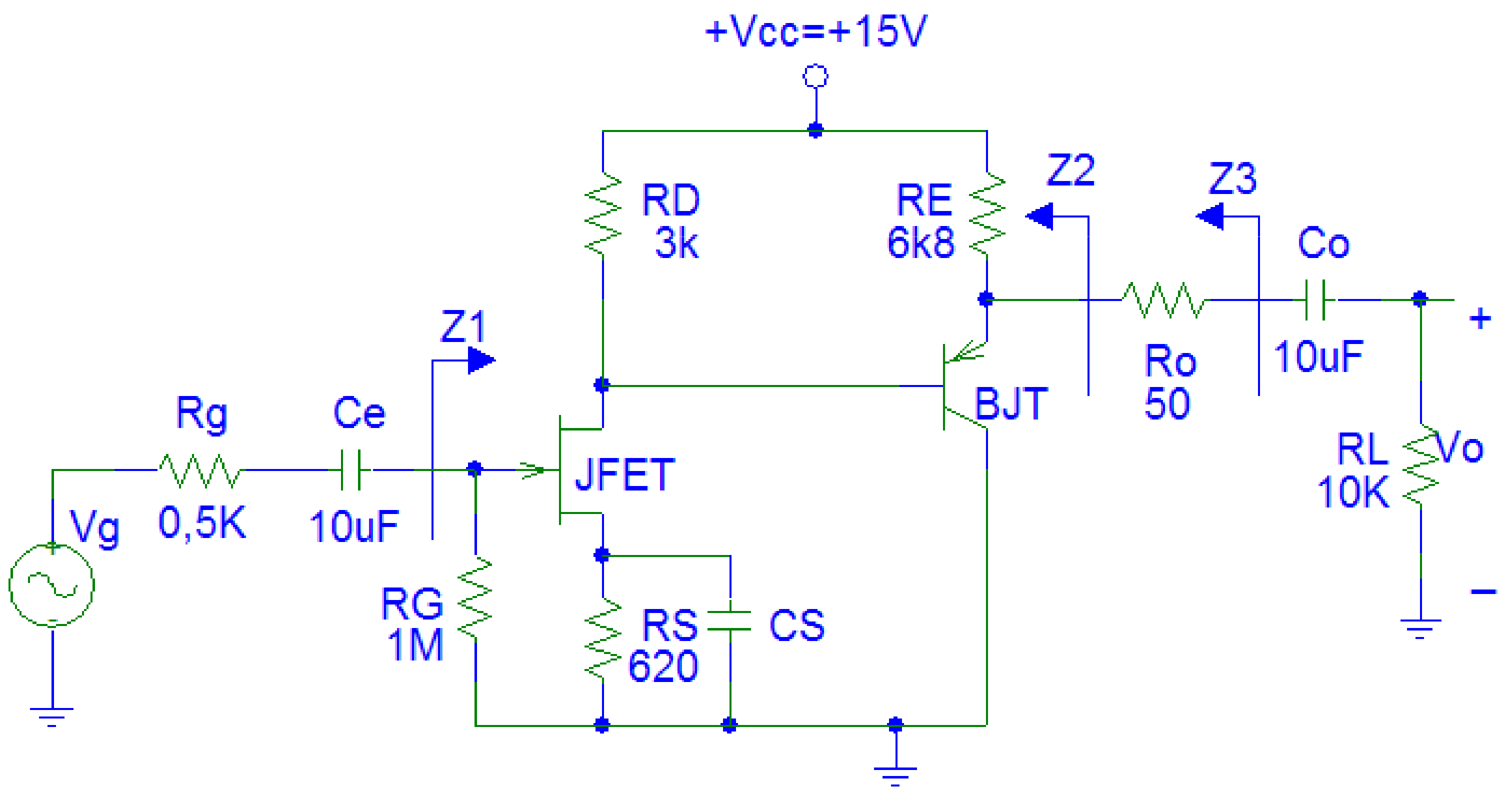
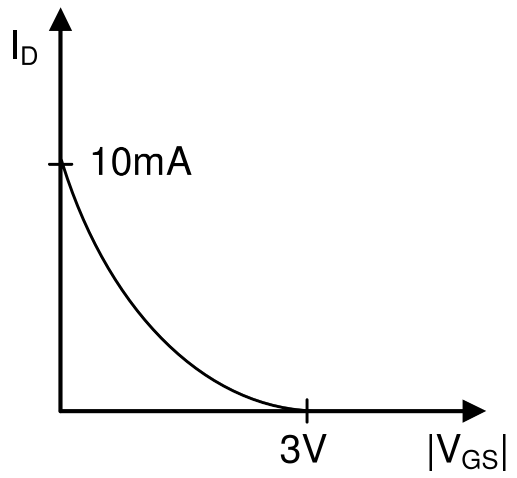
Audio multiple-stage amplifier

OBJECTIVES

- To analyze the bias circuit
- To analyze small-signal equivalent circuits and interpret the characteristics of the amplifier
- To obtain the gain and impedances
- To obtain the cut-off frequencies and the bandwidth
- To understand and anlayze the output stage
- To review the main features of this type of amplifier

Case study 2



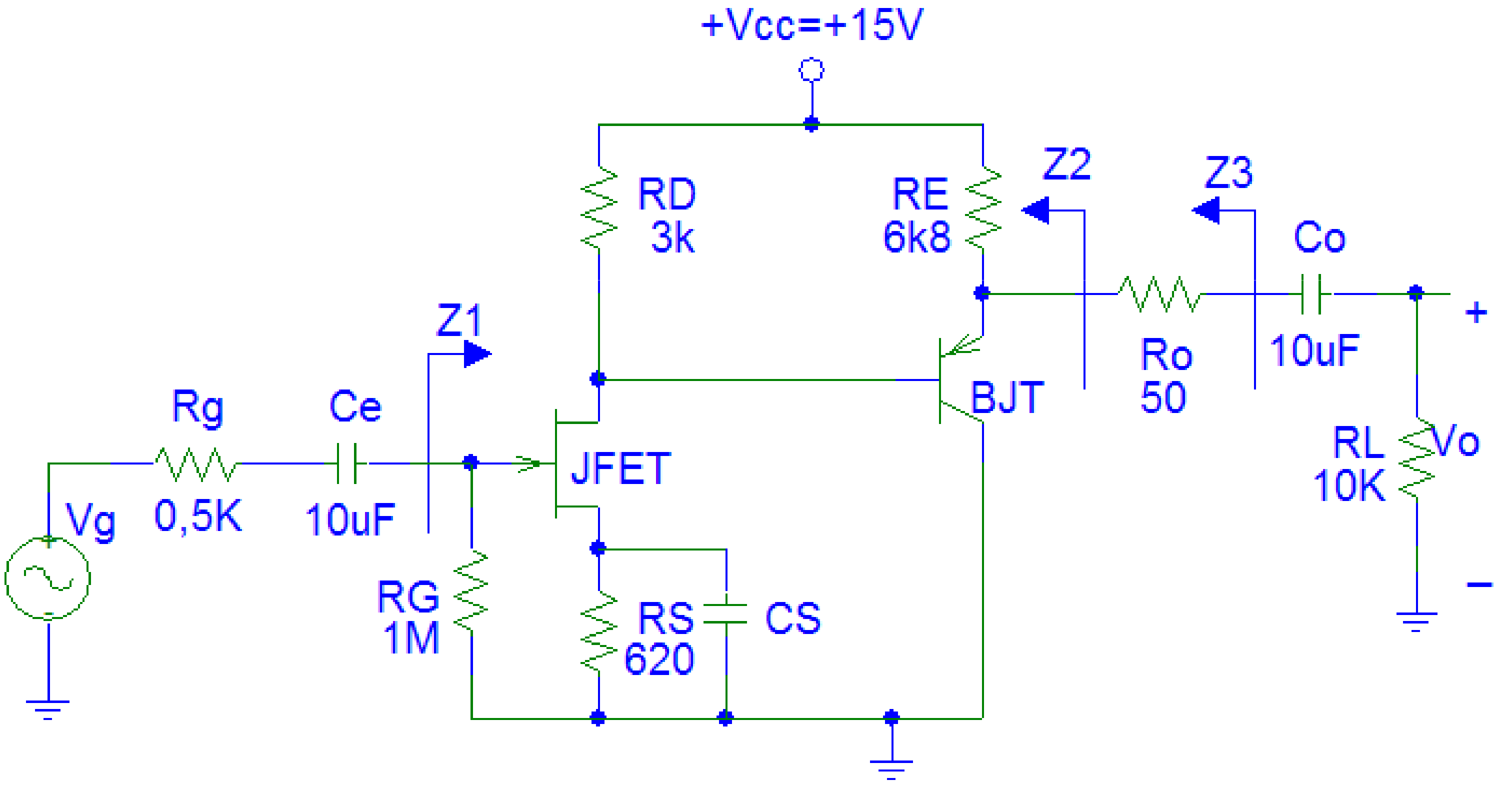


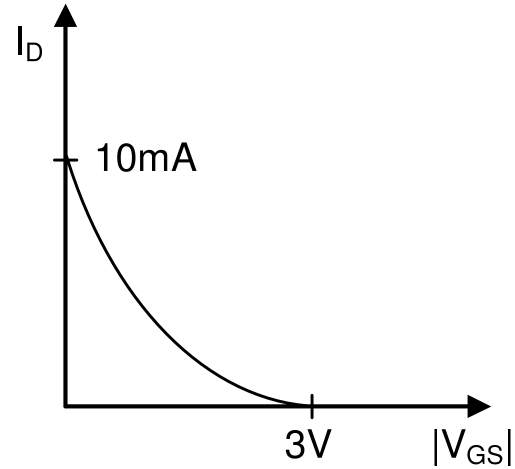
$$I_D = I_{DSS} \cdot (1 - V_{GS}/V_P)^2$$

$V_{CC} = 15$ V

RG = 1MΩ	RS = 620Ω	RD = 3KΩ	RE = 6,8KΩ	Ro = 50Ω
Rg = 500 Ω	RL = 10KΩ	CS → ∞	Ce = 10µF	Co = 10µF
$\lvert V_{BE-ON}\rvert = 0{,}7$ V	$\lvert V_{CEsat}\rvert = 0{,}2$ V	$\beta_F = 100$	$\beta_0 = 100$	$r_o = r_{ds} \to \infty$
$V_T = 25$ mV	Cgd = 1 pF	Cµ = 2pF	Cgs = 0pF	Cπ = 0 pF

Case study 2 - Bias

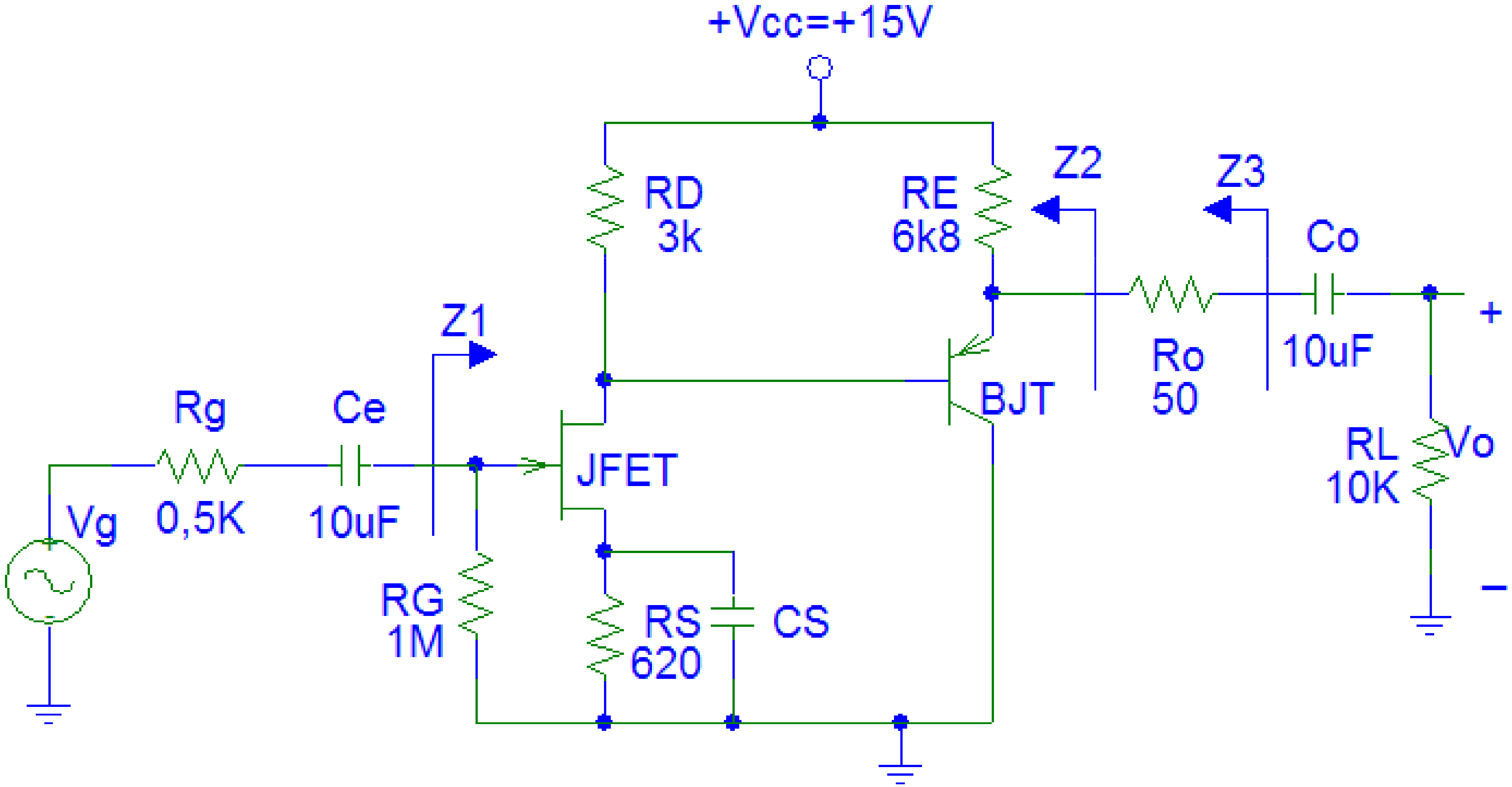




$I_D = I_{DSS} \cdot (1-V_{GS}/V_P)^2$

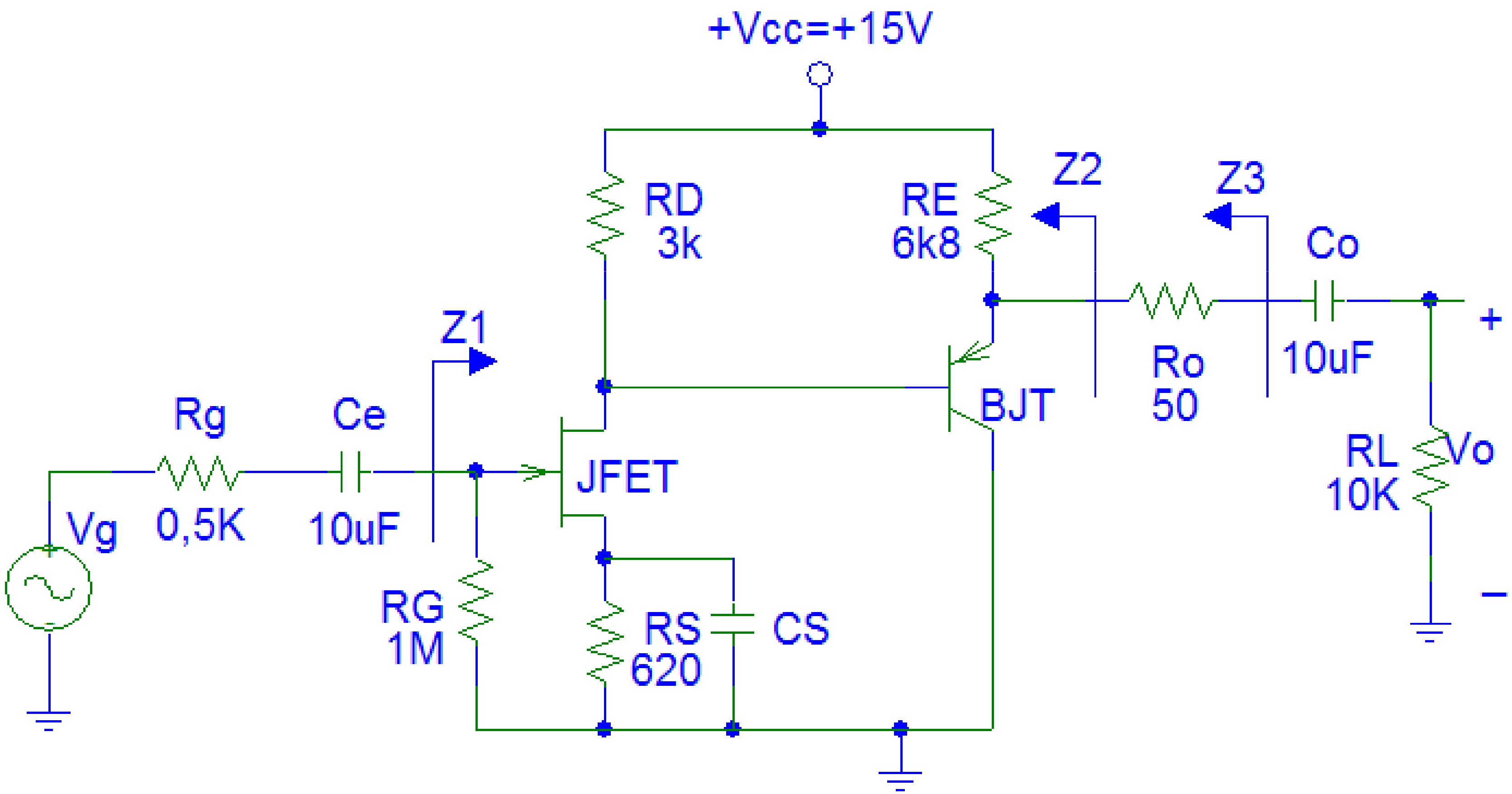
- Get the values of I_{DSS} and Vp of JFET transistor .
- Get the bias point of the transistor JFET (V_{GS}, I_D, V_{DS}).
- Get the bias point of the bipolar transistor (I_C, V_{EC}). Check if the assumption is correct that the base current of BJT is negligible.
- Obtain the DC voltage Vo.

Case study 2 – Small signal



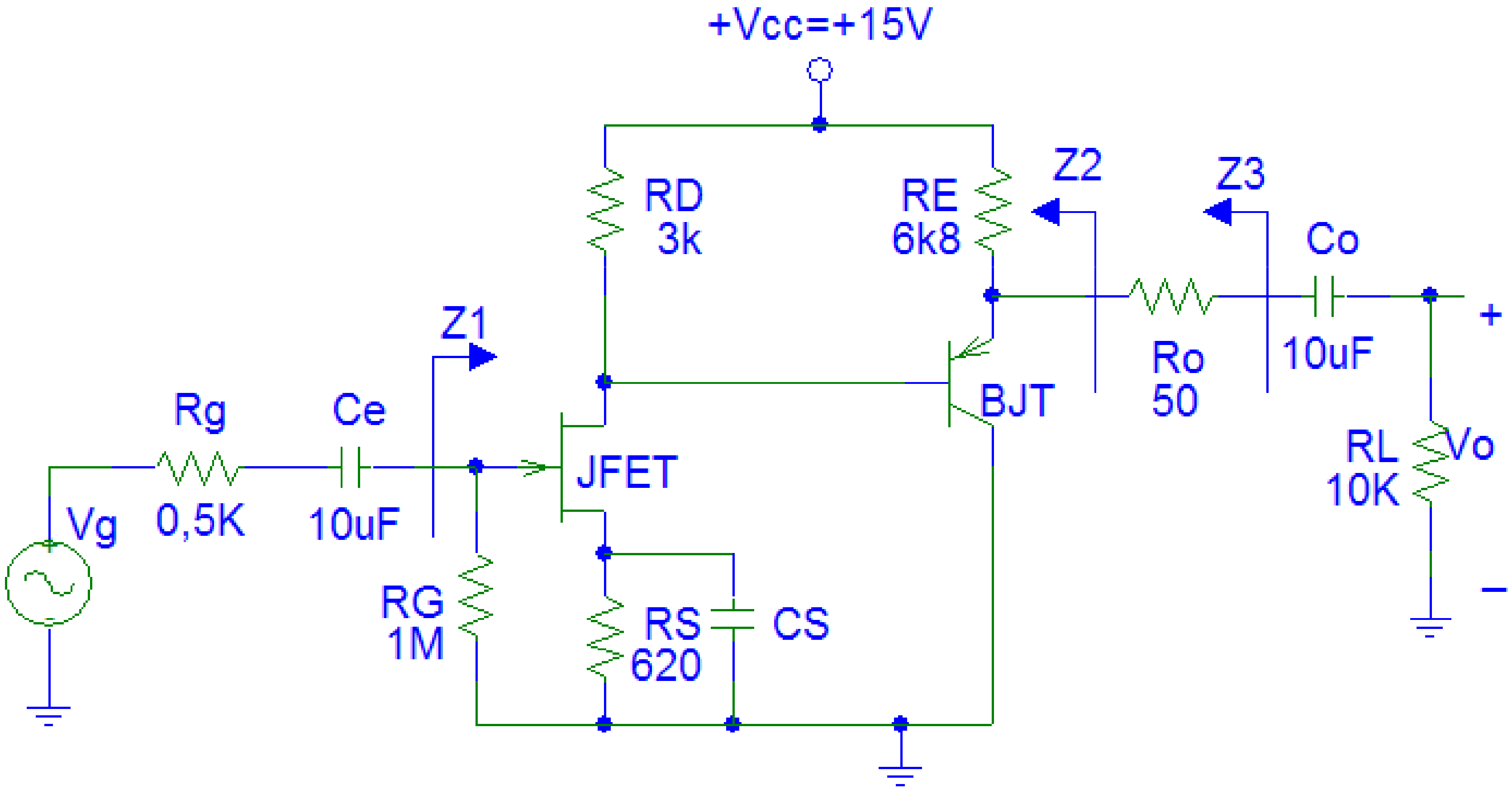
- Draw the equivalent circuit for midrange frequency.
- Obtain the gain Vo/Vg.
- Obtain the impedances Z1, Z2 and Z3.

Case study 2 – Output stage



- Draw the output characteristic curve of BJT and the static load line.
- Draw the dynamic load line.
- Obtain the maximum power supplied to the load RL = 10kΩ.
- Obtain the maximum power supplied to a load RL = 18Ω.
- Redesign the output stage to maximize the power in the load.

Case study 2 – Bandwidth



- Obtain the lower cutoff frequency using the time constants method.
- Draw the equivalent circuit for high frequencies and calculate the upper cutoff frequency.
- Redesign the capacitors to obtain a lower cutoff frequency of 4 Hz.
- Reduce the bandwidth to 20 kHz with an additional Miller capacitor.