Time: 3 hours

PROBLEM

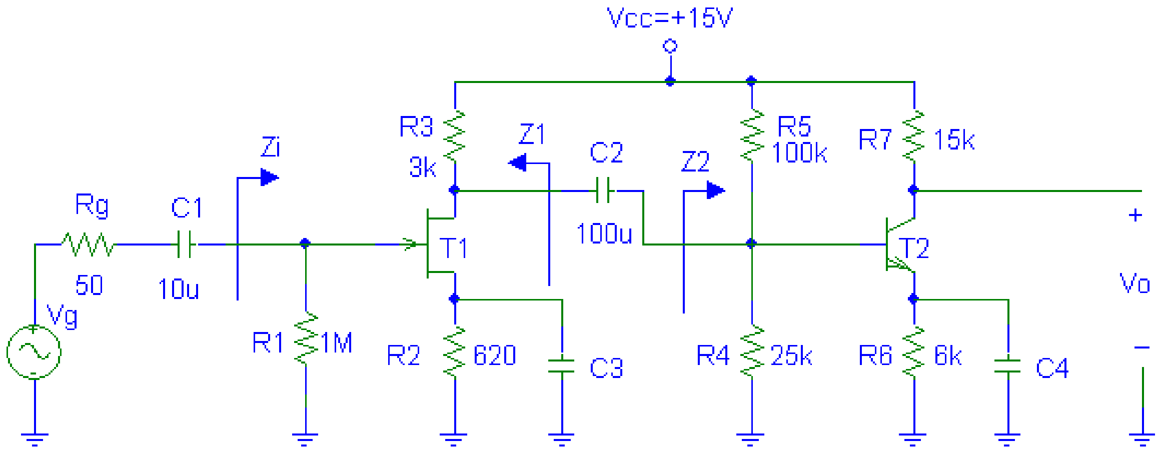


Figure 1

DATA:

Rg = 50 Ω	R1 = 1 MΩ	R2 = 620 Ω	R3 = 3 KΩ
R4 = 25 KΩ	R5 = 100 KΩ	R6 = 6 KΩ	R7 = 15 KΩ
I_{DSS} = 10 mA	V_p = -3 V	$r_{ds1} \to \infty$	$I_D = I_{DSS}\cdot(1-V_{GS}/V_p)^2$
V_{BE-ON} = 0.6 V	V_T = 25 mV	$r_{o2} \to \infty$	$\beta_F = \beta_0 = 200$
C1 = 10 μF	C2 = 100 μF	C3, C4 $\to \infty$	
Cgs_1 = 1 pF	$Cgd_1 \to 0$ pF	$C\pi_2$ = 0.5 pF	$C\mu_2 \to 0$ pF

The circuit of figure 1 is an AC coupled multi-stage amplifier (a field effect transistor and a bipolar transistor).

a) Calculate the bias point of the JFET transistor (V_{GS1}, I_{D1}, V_{DS1}).
b) Calculate the bias point of the BJT transistor (I_{C2}, V_{CE2}). Demonstrate that is true the approximation of base current being negligible.

Note: Hereinafter use the following bias currents: I_{D1} = 2.4 mA e I_{C2} = 0.4 mA.

c) Draw the small-signal equivalent circuit for midrange frequencies. Calculate the impedances Z_1, Z_2 y Z_i. Calculate the gain Vo/Vg.
d) Calculate the high cut-off frequency by using the time constants method.
e) Calculate the low cut-off frequency with the capacitors C1 and C2. Use the time constants method.
f) Plot the asymptotic Bode plot (amplitude and phase) for the complete range of frequencies.

QUESTION 1

In the circuit of figure 2 the transistors Q1 and Q2 are conected as a pseudo-Darlington multi-stage that delivers power to the load RL (equivalent to an emitter follower). Vg is a sinusoidal signal source with DC null.

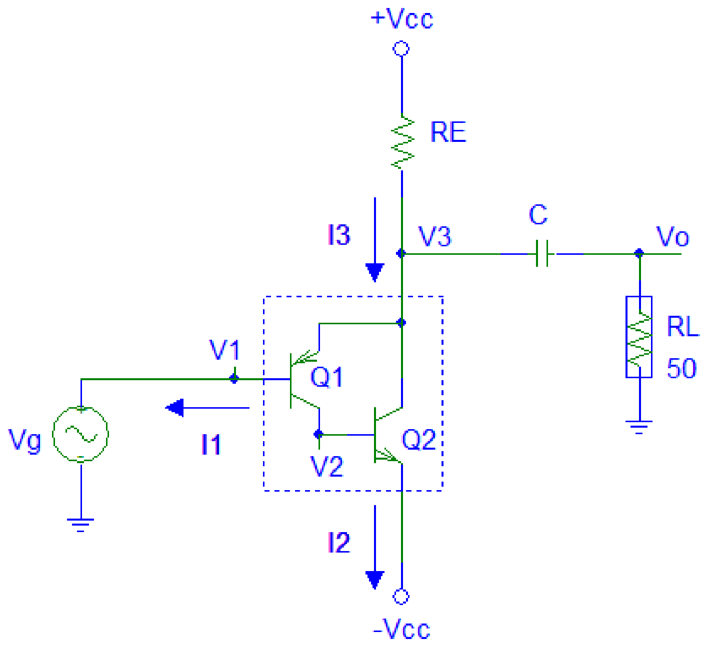


Figure 2

DATA:	$\pm Vcc = \pm 10$ V	RL = 50 Ω	V_T = 25 mV	$C \rightarrow \infty$
Transistor Q1:	$V_{EB\text{-}ON}$ = 0.6 V	$V_{EC\text{-}SAT}$ = 0.2 V	$\beta_{F1} = \beta_{01} = 200$	$r_o \rightarrow \infty$
Transistor Q2:	$V_{BE\text{-}ON}$ = 0.7 V	$V_{CE\text{-}SAT}$ = 0.3 V	$\beta_{F2} = \beta_{02} = 100$	$r_o \rightarrow \infty$

a) Calculate the DC voltages V1, V2, V3 y Vo.
b) Calculate the value of RE to obtain a DC current I3 = 200 mA.
c) Obtain the ratio between I1 and I2 and calculate the DC values of I1 and I2.
d) Demonstrate that both transistors are in the active operating region.

e) Calculate the small-signal parameters and draw the midrange frequency equivalent circuit.
f) Demonstrate that the voltage gain Vo/Vg is equal to 1 V/V approximately.

QUESTION 2

The circuit of figure 3.1 is a two-stage amplifier based on operational amplifiers (ideal OA). It is used for converting current to voltage and only the AC component is amplified and delivered to the load RL. Ig is a generalized current source.

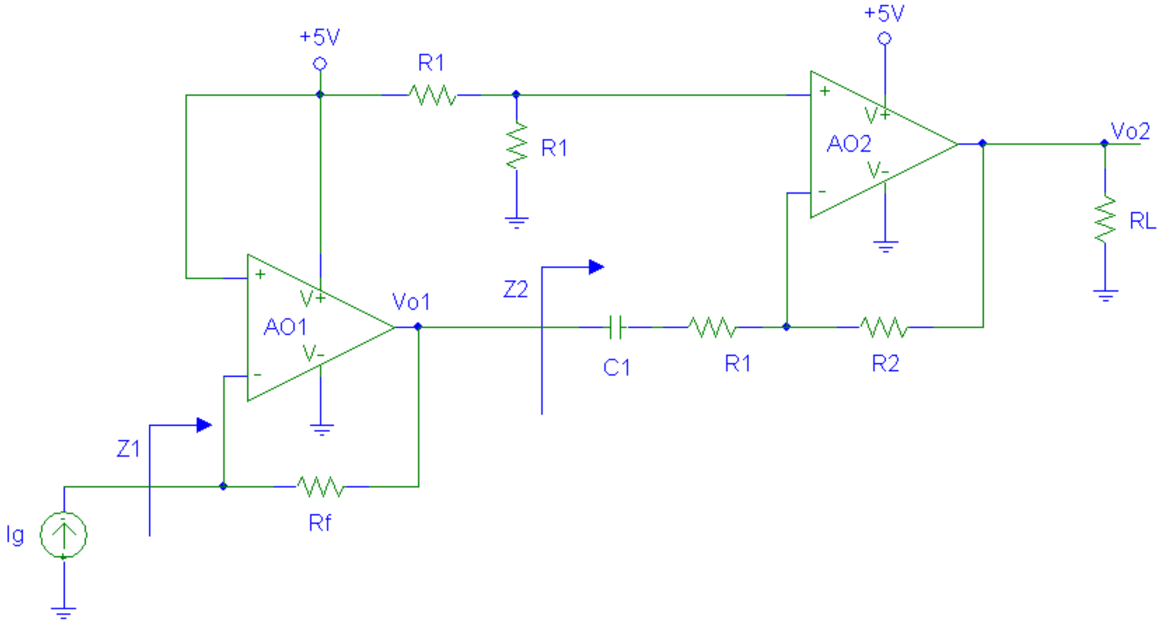


Figure 3.1

DATA: Rf = 50KΩ R1 = 10KΩ R2 = 47KΩ RL = 500Ω C1 = 100nF

Suppose initially Ig = 0µA.

a) Calculate the DC voltages Vo1 y Vo2.

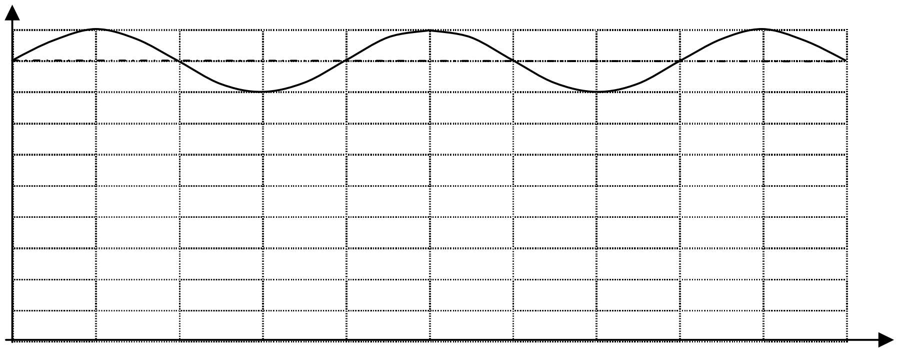
Hereinafter suppose that Ig is a sinusoidal signal of 150 kHz (AC current).

b) Calculate the gain of the first amplifier Vo1/Ig and the input impedance Z1.
c) Calculate the gain of the second amplifier Vo2/Vo1 and the input impedance Z2.

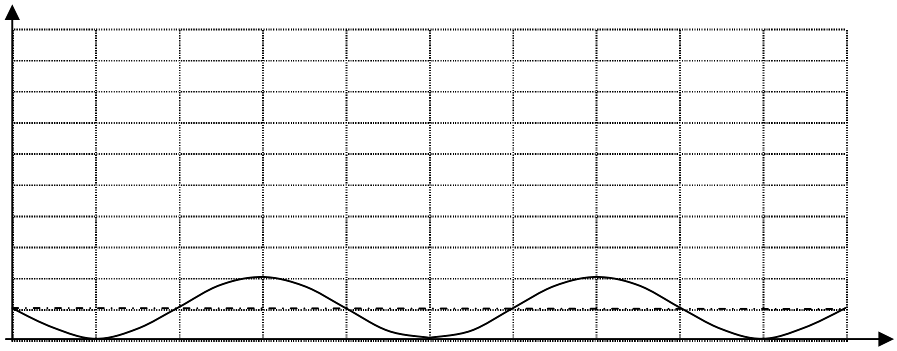
Hereinafter suppose that Ig is a signal composed of 90µA DC current and 10µA peak AC current (sinusoidal, 150 kHz).

d) Mark the signals Ig and Vo1 in figure 3.2 and plot the voltage Vo2.

Ig:



Vo1:



Vo2:

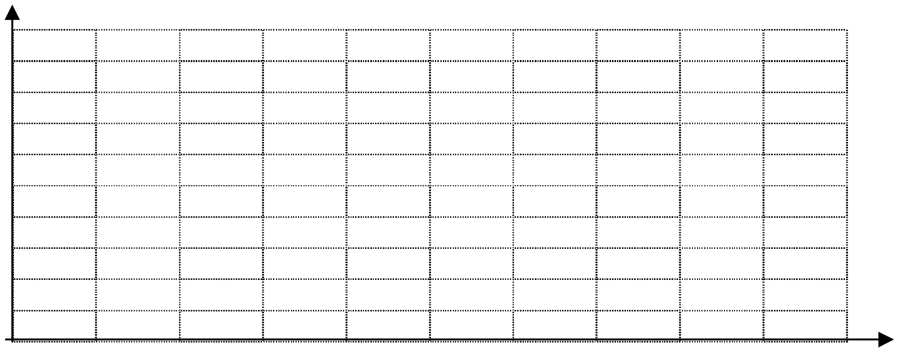


Figure 3.2

QUESTION 3

The circuit of figure 4 is a current source to the light emitting diode (LED).

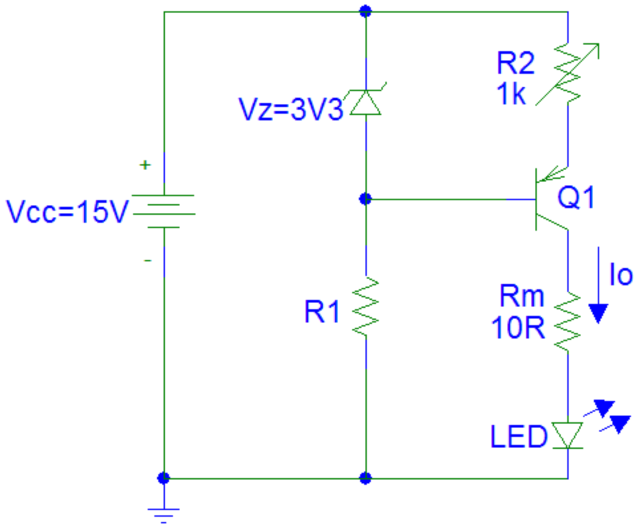


Figure 4

DATA:			
	R1 = ?	R2 = 1KΩ	Rm = 10Ω
	V_Z = 3.3V	I_{Zmin} = 10 mA	$V_{LED\text{-}ON}$ = 1.6V
	$V_{EB\text{-}ON}$ = 0.7V	V_{ECsat} = 0.2 V	β = 150 (hFE)
	$P_{TRTmáx}$ = 500mW	$I_{Cmáx}$ =100mA	$P_{LEDmáx}$ = 100mW

a) Obtain the value of R1 that polarizes the zenner diode with a current of 20 mA.

b) Obtain the value of the current Io for the maximum value of R2 (1KΩ). Demonstrate that the base current is negligible.

c) Plot the current Io as a function of V_{CE} (output characteristic of transistor Q1) and the load line for the maximum value of R2.

d) Calculate the máximum value of Io that can be withstood by the transistor (P_{TRTmax} and I_{Cmax}) and by the LED (P_{LEDmax}).

e) Calculate R2 in this case and demonstrate that the transistor is in the active operating region.

QUESTION 4

Figure 5 shows a two-transistors DC coupled stage biased with a symmetric power supply.

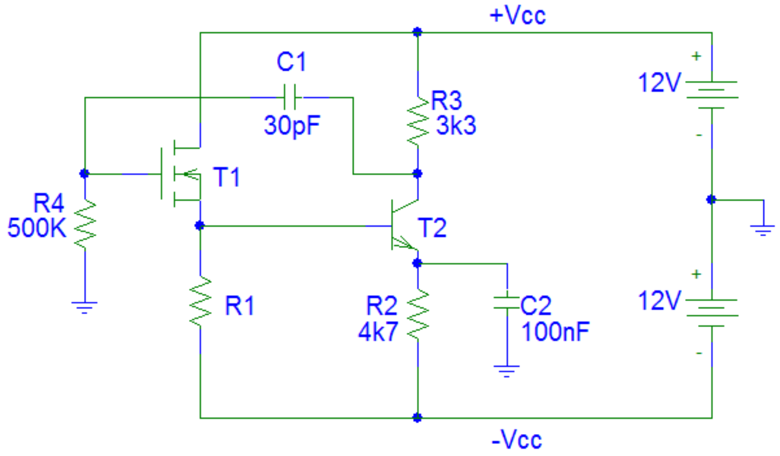


Figure 5

DATA: Bipolar Transistor	$V_{BE\text{-}ON} = 0.6$ V	$V_{CEsat} = 0.2$ V	$\beta = 200$
FET Transistor	$\lvert V_t \rvert = 1$ V	$K = 1$ mA/V^2	$I_D = K\cdot(V_{GS}-V_t)^2$

a) Draw the equivalent circuit for obtaining the bias point.

b) Calculate the value of R1 to obtain a drain current value ID = 1mA (base current is negligible). Demonstrate that the transistor T1 is in the saturation operating region.

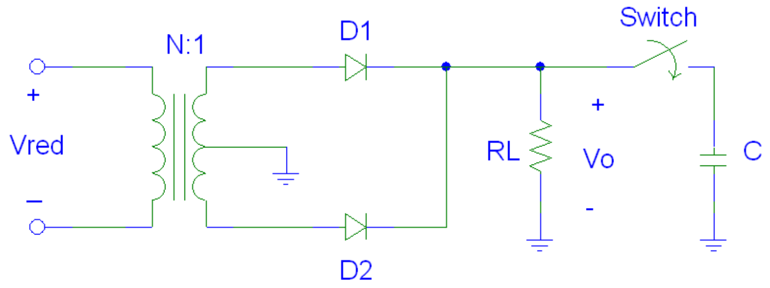
c) Calculate the bias point of transistor T2 (I_C and V_{CE}).

d) Calculate the gate DC voltage V_G and the collector DC voltage V_C.

e) Draw the midrange frequency small-signal equivalent circuit and indicate how must be connected a voltage source (Vs) and the load (RL) to have an amplifier with high voltage gain and high input impedance. Calculate the output impedance in this case.

QUESTION 5

The circuit of figure 6.1 is a diodes application. Vred is the supply voltage of a home plug. The transformation ratio between the primary and the secondary is 26:1.



DATA:

Vred = 220 Vrms; 50 Hz
Ideal diodes ($V_{D\text{-}ON}$ = 0V)
RL= 300 Ω

Figure 6.1

Consider the switch open initially (C offline).

a) Indicate giving reasons what type of circuit is and propose an application.

b) Plot in figure 6.2 the following voltage signals: anode voltage of each diode Va1 and Va2 and the output voltage Vo. Give the most significant voltage and time values. Mark in Vo in which half-wave is ON each diode.

c) Indicate the value of the peak inverse voltage (PIV) in each diode.

d) Obtain the mean value of the current in each diode.

Hereinafter consider the switch closed (C connected to the circuit).

e) Plot in figure 6.3 the ripple voltage of value 1V peak-peak observed in an oscilloscope in AC mode.

f) Calculate the capacitor C to obtain a ripple voltage up to 1V peak-peak

g) Calculate the increase of the DC voltage Vo that is obtained by connecting the capacitor C.

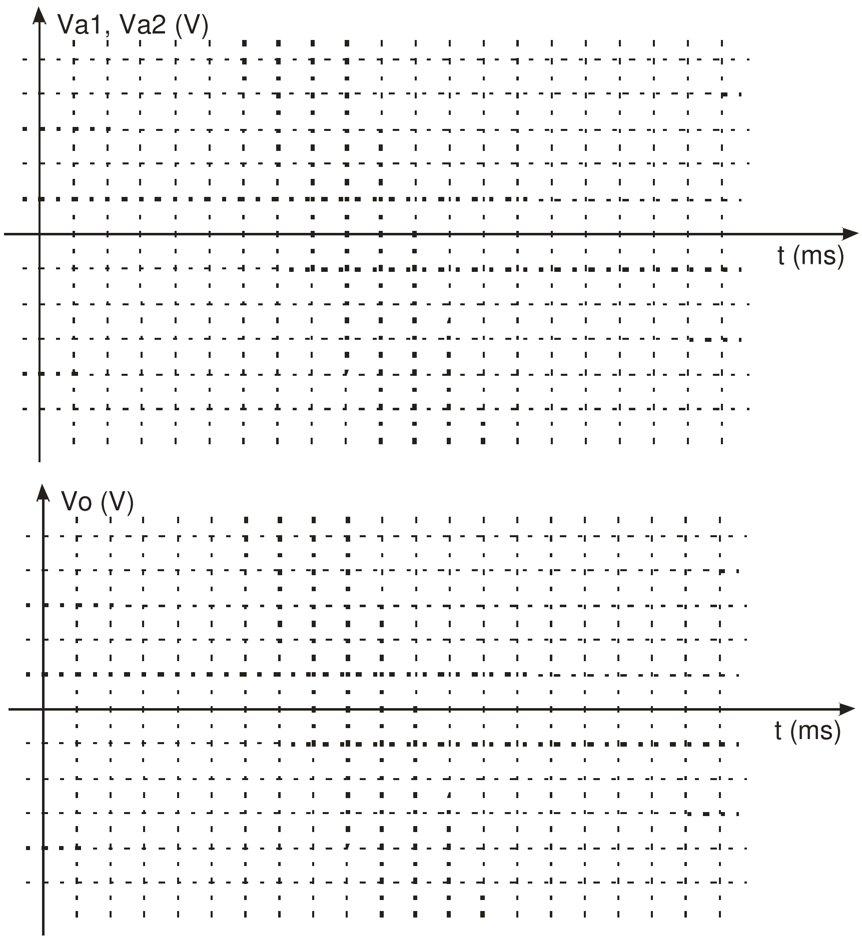


Figure 6.2

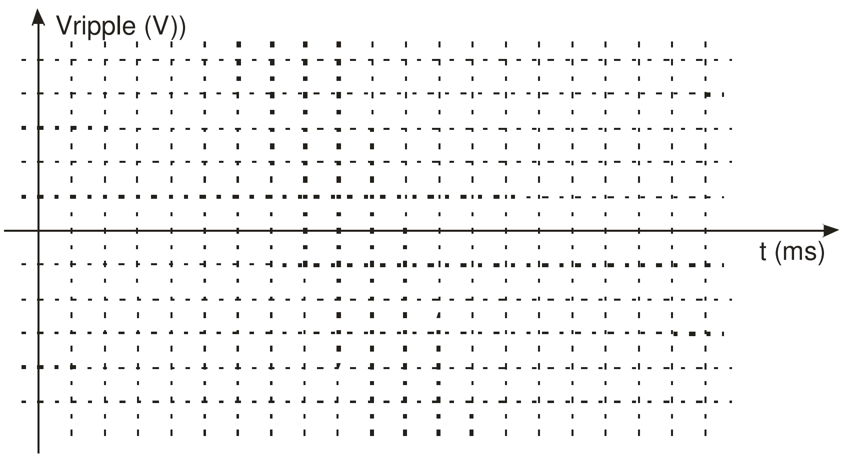


Figure 6.3