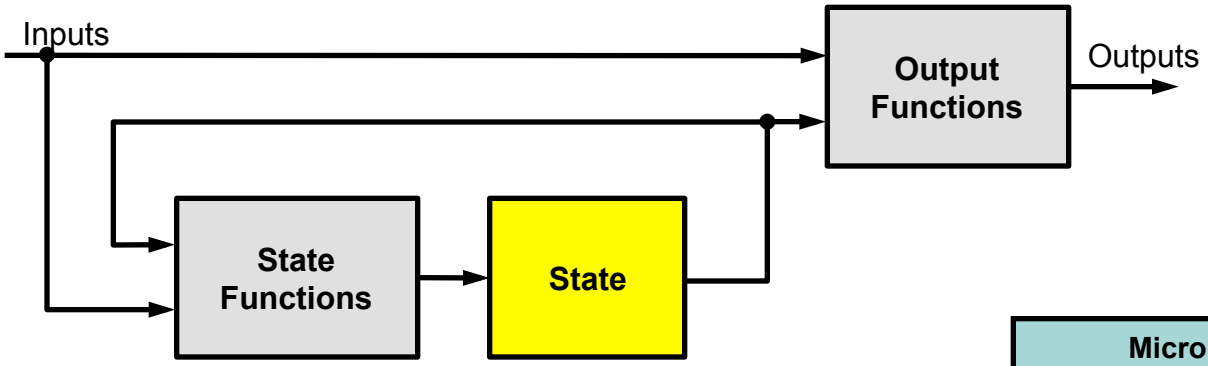
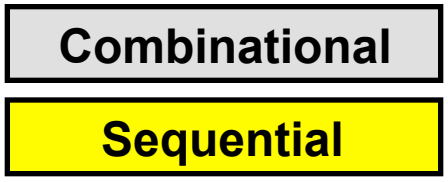
Flip-flops

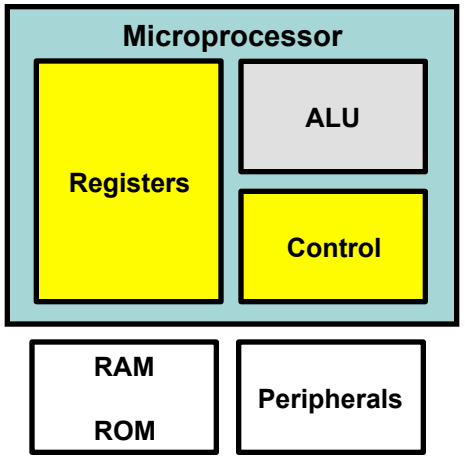
© Luis Entrena, Celia López,
Mario García, Enrique San Millán

Universidad Carlos III de Madrid

Digital circuits and microprocessors







Outline

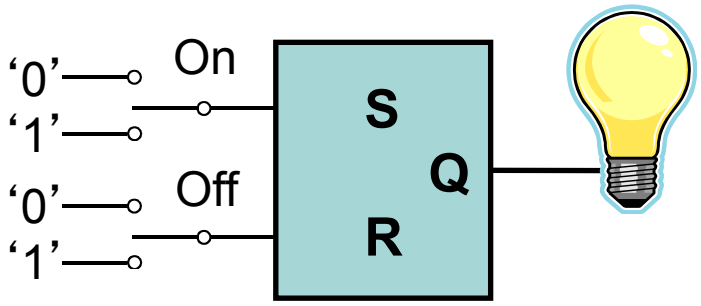
- Introduction
  - The flip-flop as the basic memory element
  - Flip-flop classification
- Asynchronous flip-flops
- Synchronous flip-flops
- Synchronous flip-flops with asynchronous inputs
- Flip-flop control logic
- Timing characteristics
- Synchronous circuits
- Circuits with flip-flops: chronograms

1. Introductión: flip-flops

- Definition:
  - Circuit storing an information bit. It has two stable states, logic 0 and logic 1. The state does not change until the control inputs allow it.
- Classification
  - Control logic: inputs determining the new state
    - D, T, SR, JK
  - Syncronism:
    - Asynchronous: can change the state in response to any input, at any time
    - Synchronous: they have a control input that states when the state can change
      - Level-triggered
      - Edge-triggered

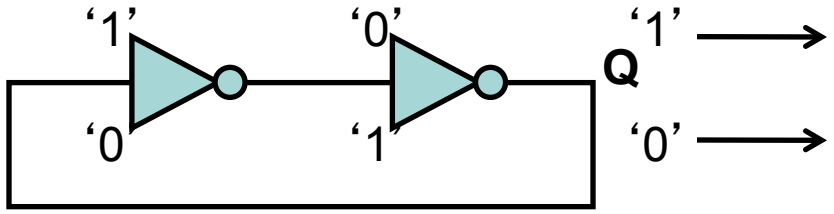
2. Asynchronous flip-flop

- SR asynchronous flip-flop
  - S= ‘1’ => Set
  - R= ‘1’ => Reset
  - S=R= ‘0’ => Keep state
- Characteristics
  - **Memory**: it keeps the state if inputs are not active
  - **Asynchronous**: the state changes inmediately if R or S are activated



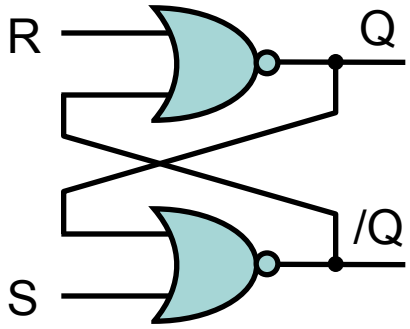
Asynchronous flip-flop

- State keeping circuit



Two stable states

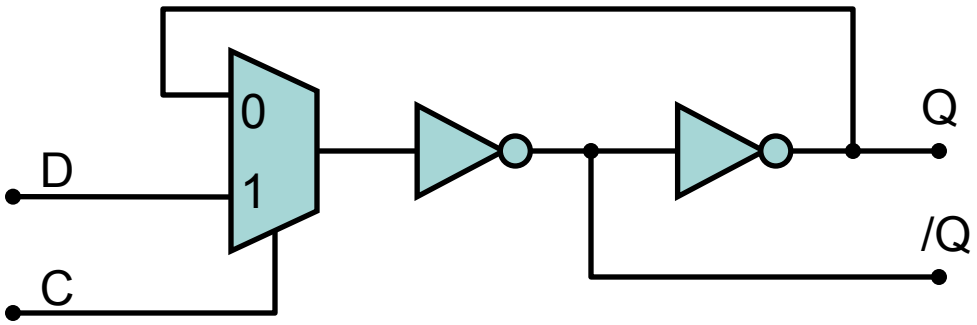
- With control signals

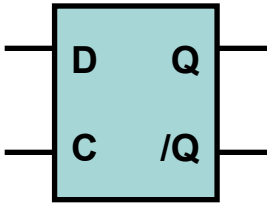


S	R	Q	/Q	
0	0	Q	/Q	→ Keep state
1	0	1	0	→ Set
0	1	0	1	→ Reset
1	1	0	0	→ Forbidden state

3. Level-triggered synchronous flip-flop

- It has a control signal that allows the state to be changed
- Level-triggered synchonous D Flip-flop (D-latch)
  - C= ‘1’ => state changes to D value
  - C= ‘0’ => keep state

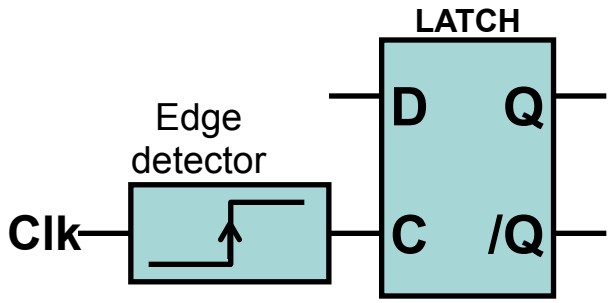


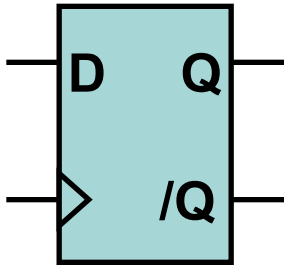


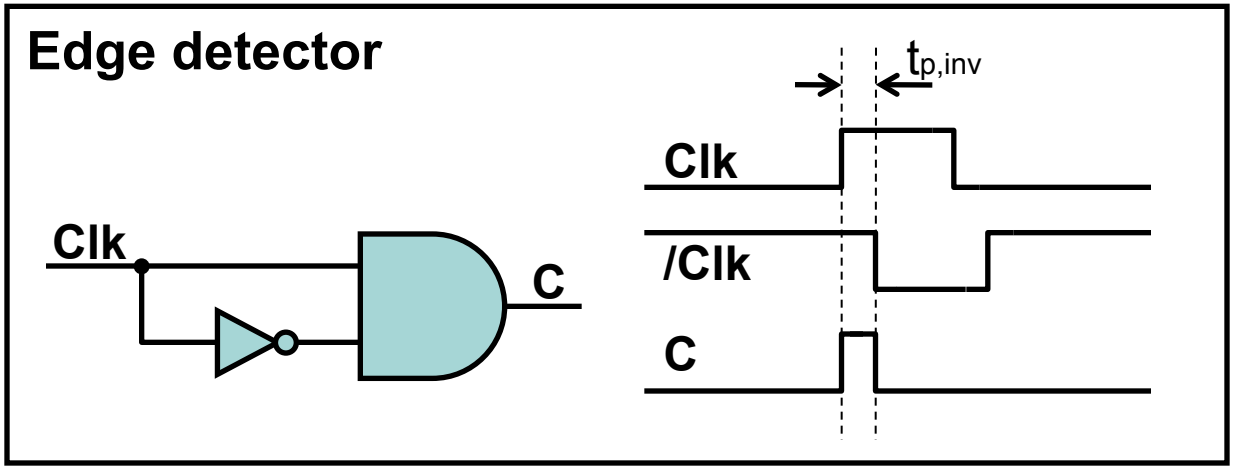
C	D	Q	/Q	
0	X	Q	/Q	→ Keep state
1	0	0	1	→ Assign ‘0’
1	1	1	0	→ Assign ‘1’

Edge-triggered synchronous flip-flop

- Edge-triggered synchonous D flip-flop



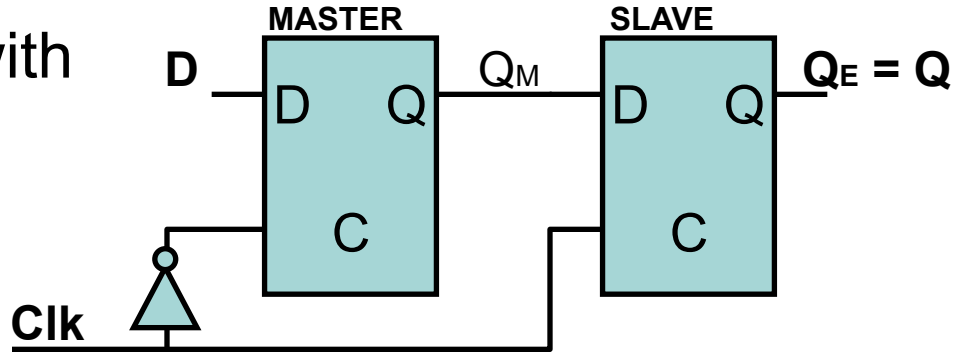


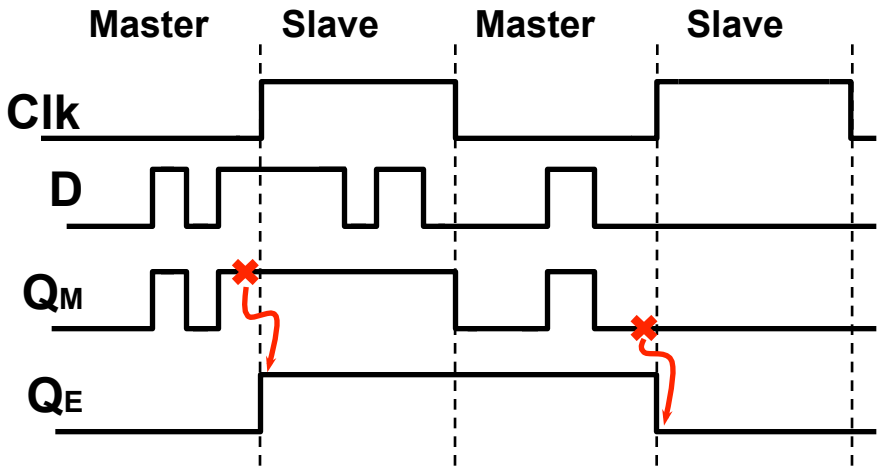


Bad solution due to technology. Inverter delay is not controllable.

Master-Slave synchronous flip-flop

- Two latches active with opposite levels

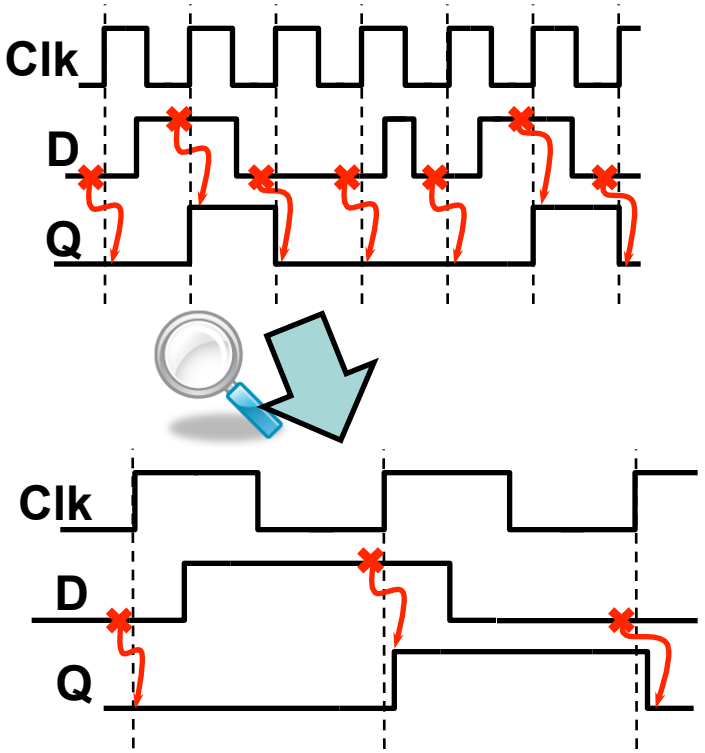




- Q_E changes only in clock rising edges
- Q_E new value is D value just before the clock edge

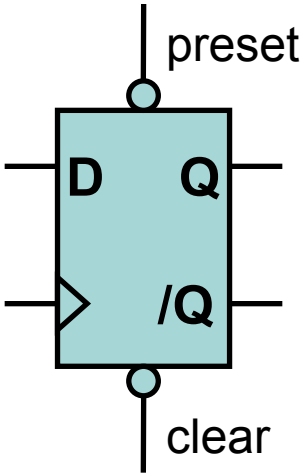
Edge triggered synchonous D flip-flop

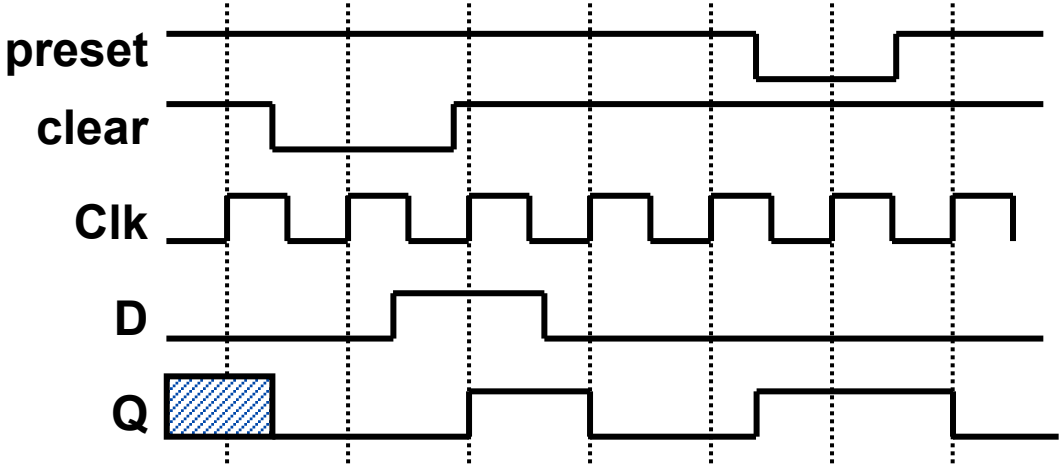
- The one used most
- Only changes in clock edges (normally rising edges)
- The output change takes place just before the edge
- The output new value is taken from D input just before the edge



4. Synchronous flip-flops with asynchronous inputs

- Synchronous flip-flops with asynchronous inputs for initialization
  - Clear: asynchronous initialitation to ‘0’
  - Preset: asynchronous initialitation to ‘1’
  - Usually low-level active





5. Flip-flop control logic

- Flip-flop inputs control the way the state is changed
  - Kinds of flip-flops depending on the inputs:
    - D,T,JK,SR
  - Enable signal:
    - Allows/prevents the state to change
    - In nof enabled, the state is kept
  - Synchronous initialization
    - Set to ‘0’ ir ‘1’ in a synchronous way

Flip-flop control logic

- Working tables
  - Describe functionality

D flip-flop (Data)

D	Q'
0	0
1	1

T flip-flop (Toggle)

T	Q'
0	Q
1	/Q

SR flip-flop (Set-Reset)

S	R	Q'
0	0	Q
0	1	0
1	0	1

JK flip-flop (Jump & Kill)

J	K	Q'
0	0	Q
0	1	0
1	0	1
1	1	/Q

- Transition tables
  - Describes the new state in terms of the present state and input values

D flip-flop

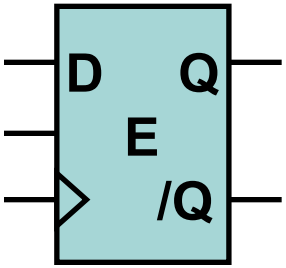
D	Q	Q'
0	0	0
0	1	0
1	0	1
1	1	1

T flip-flop

T	Q	Q'
0	0	0
0	1	1
1	0	1
1	1	0

Flip-flop control logic

- Flip-flops with enable

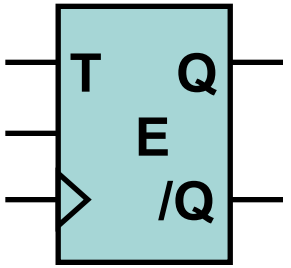


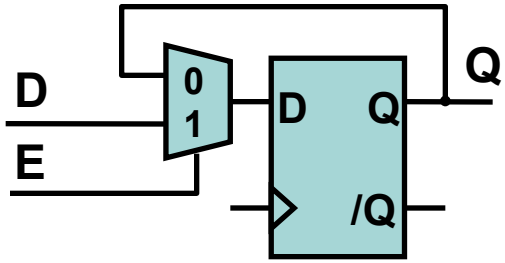
D flip-flop

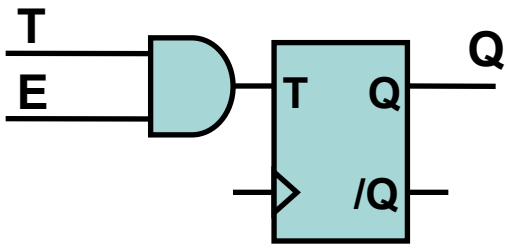
E	D	Q'
0	X	Q
1	0	0
1	1	1

T flip-flop

E	D	Q'
0	X	Q
1	0	Q
1	1	/Q

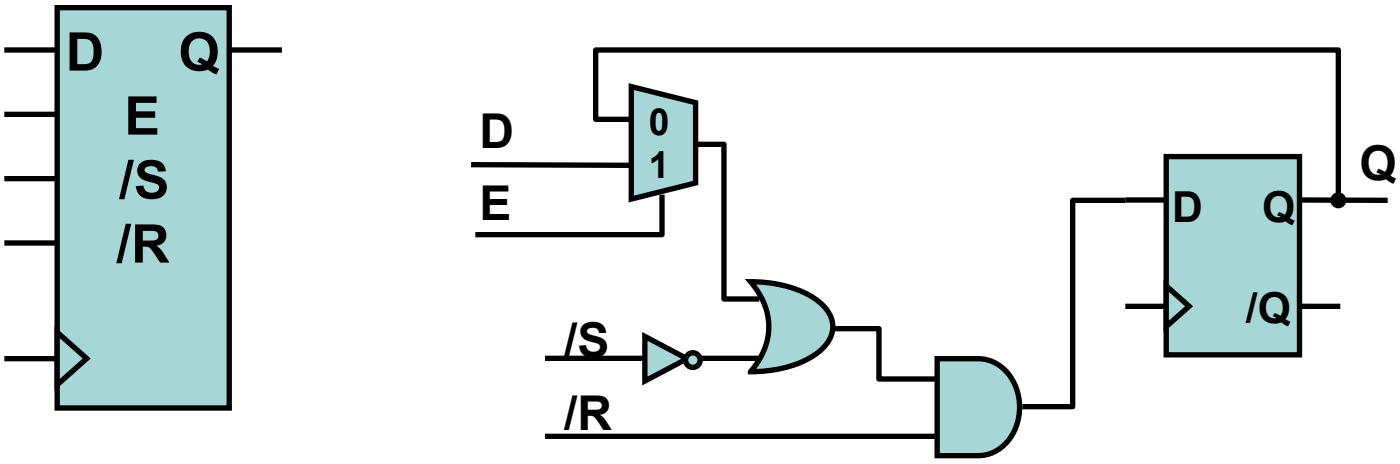






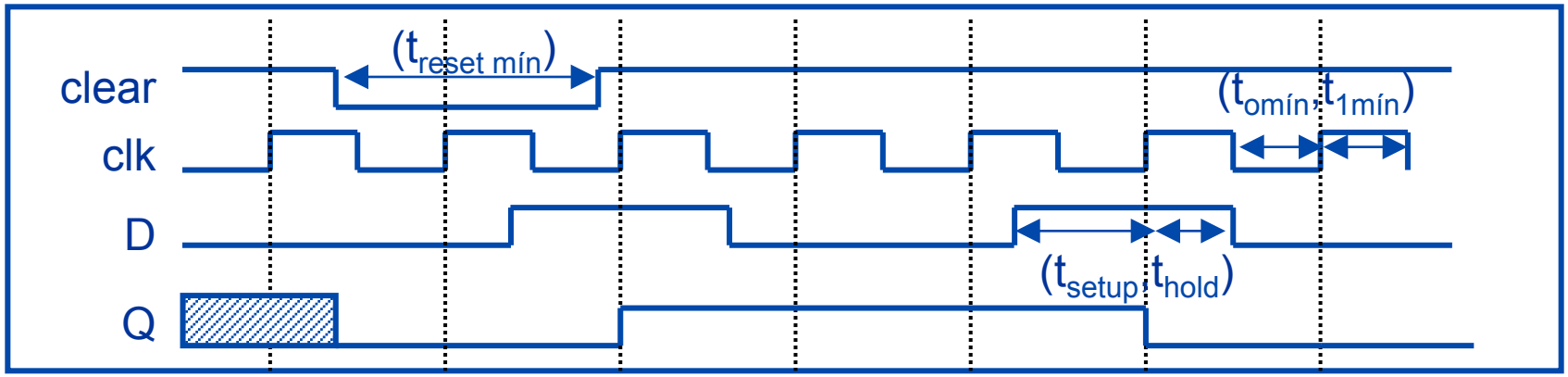
Flip-flop control logic

- Flip-flop with synchronous initialization
  - Set: forces ‘1’
  - Reset: forces ‘0’
- Example: D flip-flop with Enable, Set and Reset
  - Priority: Reset, Set, Enable



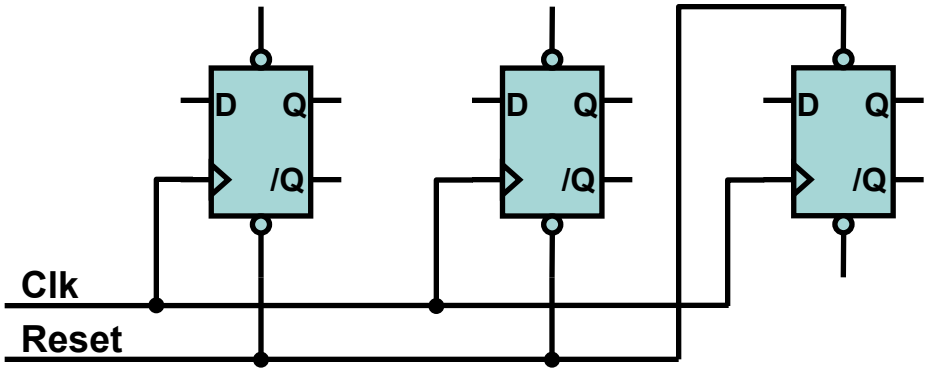
6. Timing characteristics

- Timing flip-flop restrictions
  - Clock level length → (t_{0min},t_{1min})
  - Asynchronous signals length → ($t_{reset\ min}$)
  - Data insertion times→ (t_{setup},t_{hold})



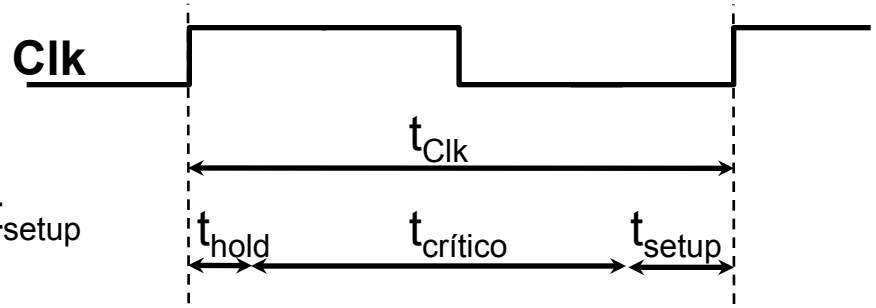
7. Synchronous circuits

- Synchronous circuit
  - Every flip-flop use the same clock
  - Every flip-flop is triggered by the same clock edge (usually the rising edge)
  - There is a common initialization signal called *Reset*



Synchronous circuits: the clock cycle

- Critical path:
  - Path between two flip-flops with the larger delay
  - Slowest path between two flip-flops. It determines the maximum allowable clock frequency for the circuit.



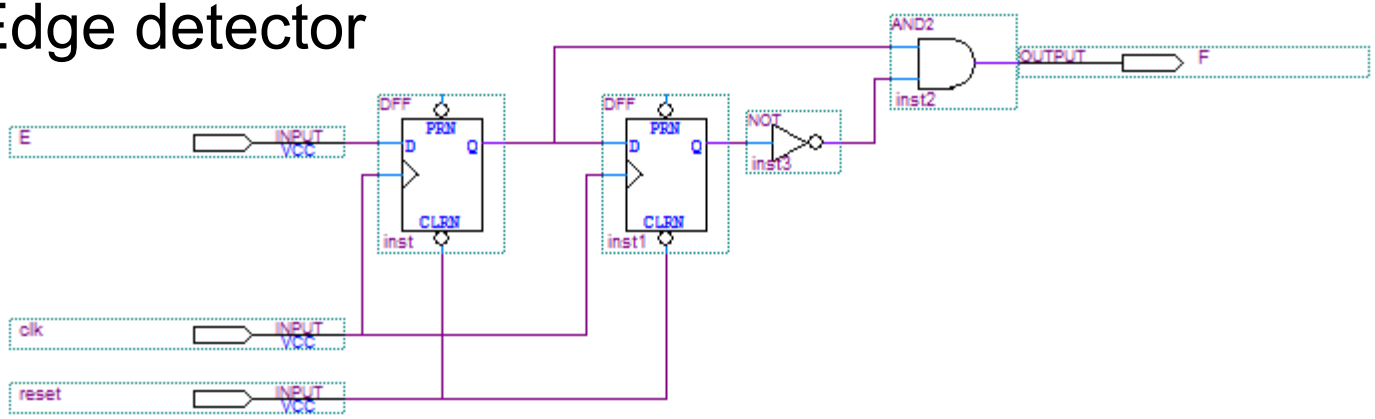
$t_{Clk} > t_{hold} + t_{crítico} + t_{setup}$

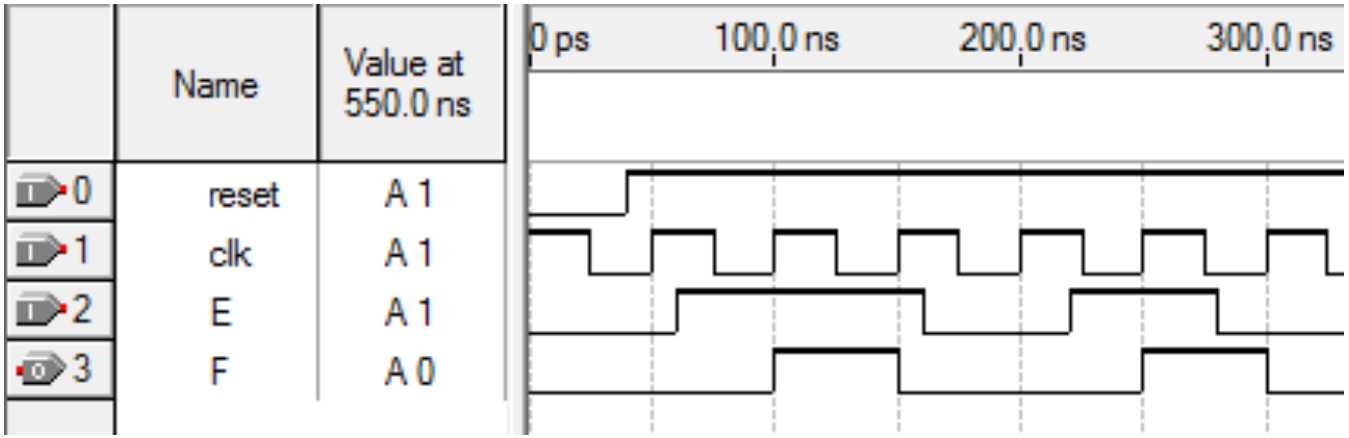
$f_{Clk} = 1 / t_{Clk}$

$t_{Clk} = 1ns \rightarrow f_{Clk} = 1GHz$

7. Chronograms

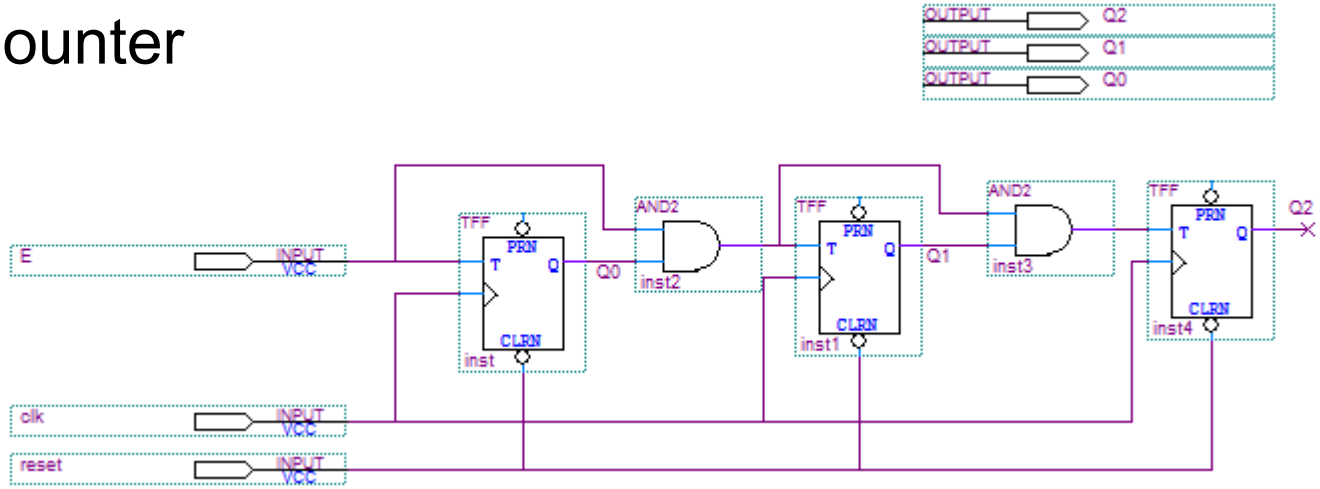
- Edge detector

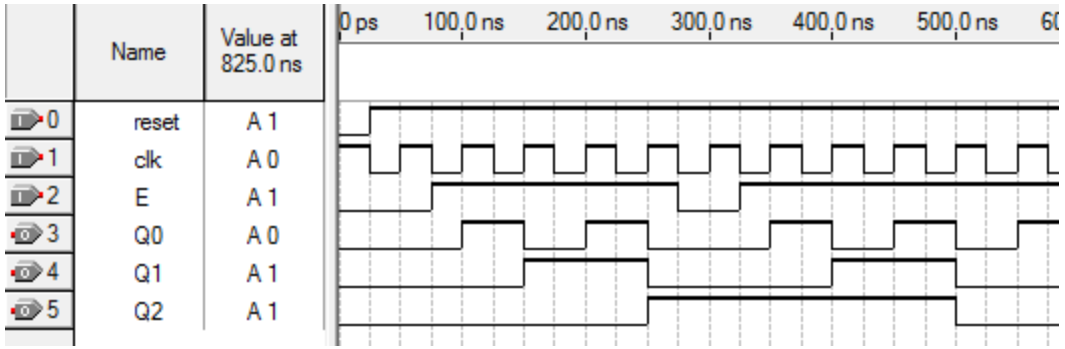




Chronograms

- Counter





Bibliography

- “Circuitos y Sistemas Digitales”. J. E. García Sánchez, D. G. Tomás, M. Martínez Iniesta. Ed. Tebar-Flores
- “Electrónica Digital”, L. Cuesta, E. Gil, F. Remiro, McGraw-Hill
- “Fundamentos de Sistemas Digitales “, T.L Floyd, Prentice-Hall