Synchronous Sequential Circuits

© Luis Entrena, Celia López, Mario García,
Enrique San Millán

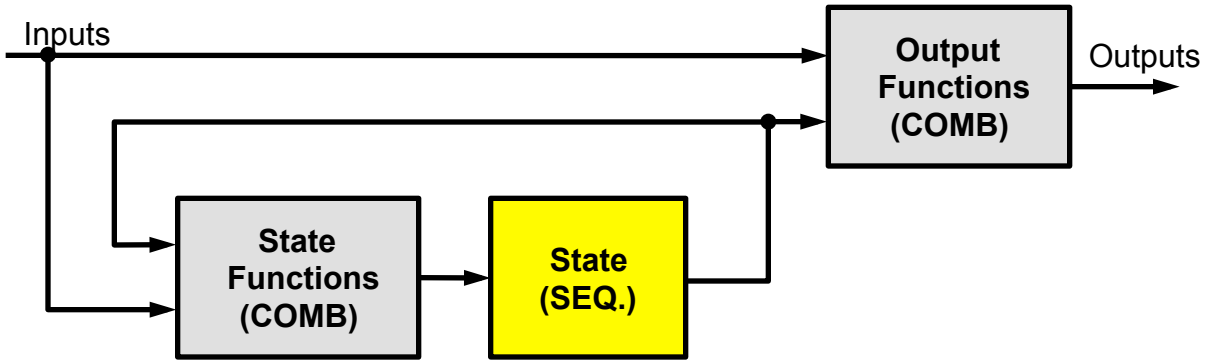
Universidad Carlos III de Madrid

Outline

- Introduction
- Finite State Machines
  - Moore model
  - Mealy model
- Synchronous Sequential Circuits Analysis
- Synchronous Sequential Circuits Synthesis
- Examples

Introduction

- General scheme of a synchronous sequential circuit:



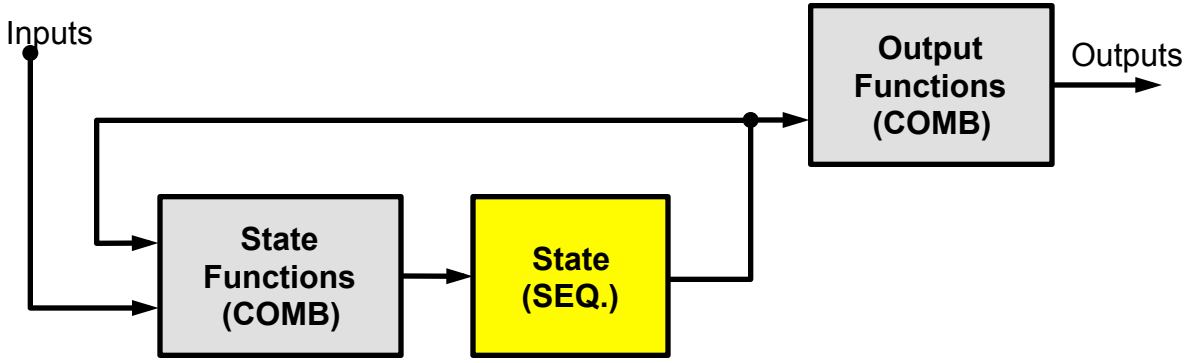
- The block "State" is composed by flip-flops, all of them synchronized with the same clock signal

Finite State Machines

- The behaviour of a synchrouns circuit can be represented with a Finite State Machine (FSM)
- A finite state machine has the following elements:
  - X = Inputs
  - Y = Outputs
  - Z = States (flip-flop values, they change with each clock edge)
  - δ = State functions (combinational functions of the flip-flop inputs)
  - λ = Output functions (combinational)
- A FSM is defined as a sequence of events in discrete times. The States change in each event (the changed value is defined by δ).

Moore Model

- In the Moore model, outputs depend only on the states (not on the inputs)
- Moore finite state machine:
  - $Z = \delta (X, Z)$
  - $Y = \lambda (Z)$
- Structure of a Moore model circuit

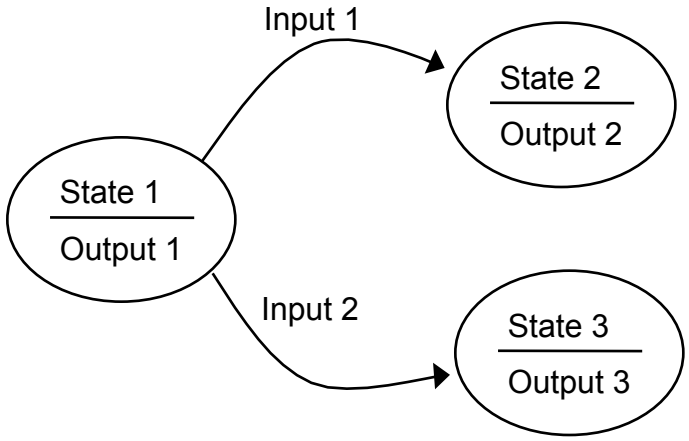


Moore Model

- Clock and reset signals do not appear in finite state machines, the association between them and the finite state machine is:
  - In each clock edge there is a transition or state change
  - Reset is used only to establish the initial state
- In Moore machines the outputs change only if there is a state change
  - Outputs are synchronized with the clock signal

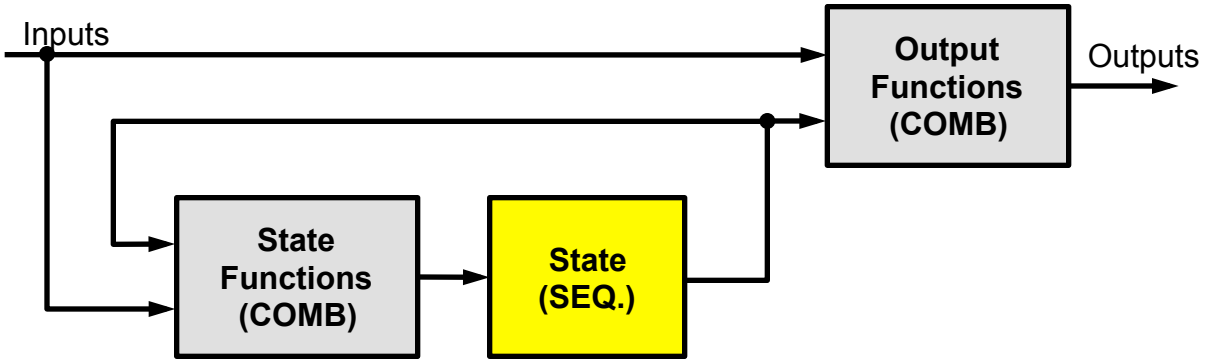
Moore Model

- A FSM can be represented with a State Transition Graph (STG):
  - Each state is represented with a circle
  - Each state transition is represented with an arrow
  - The different input conbinations are represented in the arrows
  - In Moore machines, outputs are represented inside each state
- State Transition Graph (Moore):



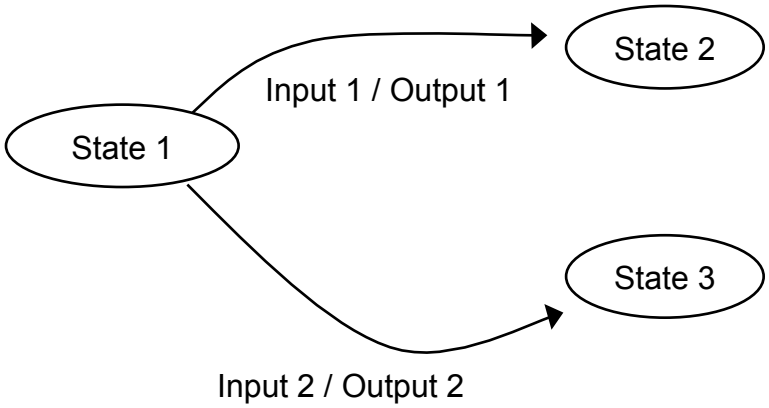
Mealy Model

- In Mealy model the outputs depend both on the inputs and the states (it is the more gerenal case)
- Mealy FSM:
  - $Z = \delta (X, Z)$
  - $Y = \lambda (X, Z)$
- Structure of a Mealy machine associated circuit:



Mealy Model

- **Mealy State Transition Graph**:
  - Each state is represented with a circle
  - Each state transition is represented with an arrow
  - The different input combinations are represented in the arrows
  - En Mealy model, outputs are represented in the arrows (they depend on the state and the inputs)



Mealy Model

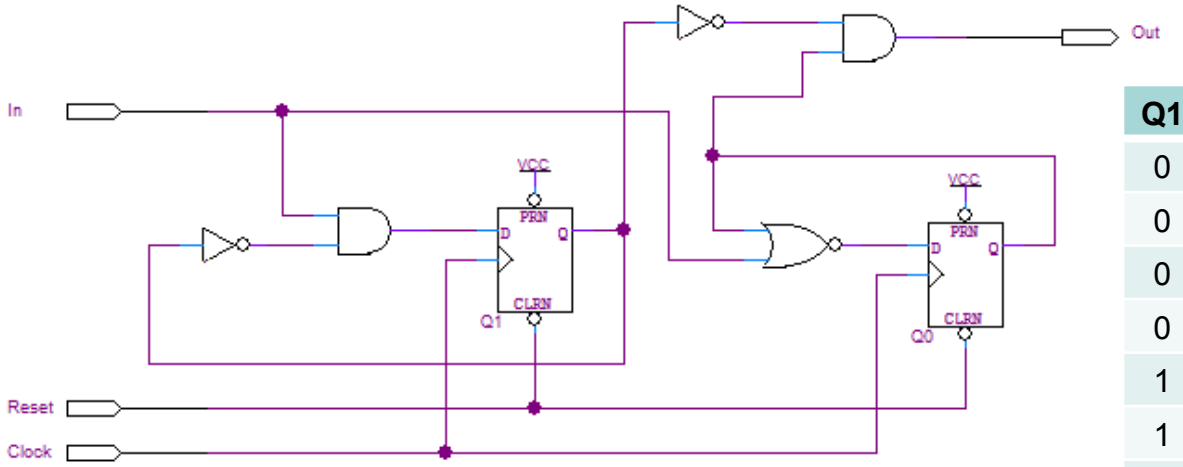
- The same as in Moore machines, clock and reset signals are implicit
- In Mealy machines, outputs may change at any moment (a change in the inputs is sufficient):
  - Outputs are **not** synchronized with the clock signal
  - TIP: Although outputs are not synchronized, the circuit is still synchronous (all the flip-flops are synchronized with the same clock signal)

Analysis and Synthesis of Synchronous Sequential Circuits

- **Analysis**: Starting from a circuit, obtain its functionality
  - **Combinational Circuits:**
    - Obtain truth tables of boolean functions of the outputs
  - **Sequential Circuits**:
    - Obtain STG, or state and output functions (δ y λ)
- **Synthesis**: Starting from a functionality, obtain a circuit implementation
  - **Combinational circuits:**
    - Obtain boolean expressions, implement with logic gates, multiplexers, decoders, etc.
  - **Sequential circuits:**
    - Obtain STG and implement state and output functions (δ y λ) with logic gates, multiplexers, dedoders, etc.

Analysis of Synchronous Sequential Circuits

- Analysis: Calculate δ y λ, obtain the transitions table, and obtain the STG.
- Example:



Transitions table:

Q1	Q0	In	D1	D0	Q1+	Q0+	Out
0	0	0	0	1	0	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

$$\delta \Longrightarrow \begin{cases} D_0 = \overline{Q_0 + In} \\ D_1 = \overline{Q_1} \cdot In \end{cases}$$

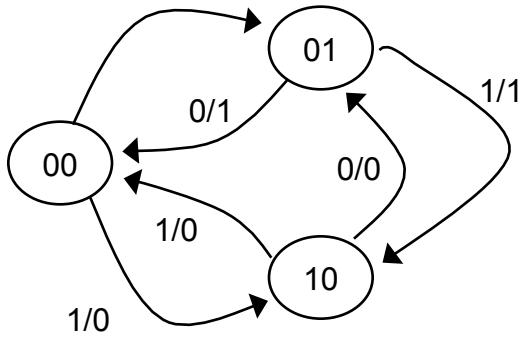
$$\lambda \Longrightarrow \quad Out = \overline{Q_1} \cdot Q_0$$

Analysis of Synchronous Sequential Circuits

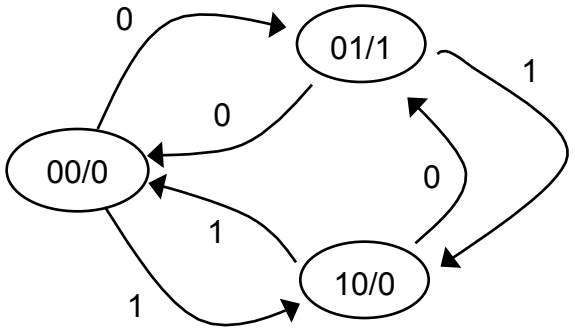
Transitions Table:

Q1	Q0	In	D1	D0	Q1+	Q0+	Out
0	0	0	0	1	0	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	1	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

STG (Mealy):



STG (Moore):



Synthesis of Synchronous Sequential Circuits

- Starting from the functionality of a sequential circuit, the steps to obtain a circuit implementation are:

1. Obtain the STG
2. Encode the states
3. Obtain the outputs and state transitions tables
4. Flip-flops excitation table
5. Obtain the output functions
6. Obtain the state functions
7. Implementation

- The difference between Moore y Mealy is in the output funcions

Flip-flop excitation tables

- These tables describe all the possible input combinations that allow to change from state Q to Q+

R-S latch

Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

J-K flip-flop

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D flip-flop

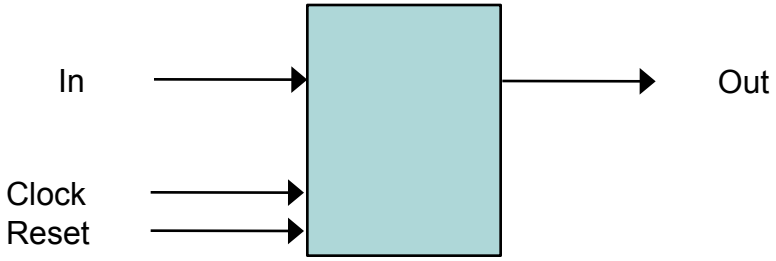
Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

T flip-flop

Q	Q+	T
0	0	0
0	1	1
1	0	1
1	1	0

Synthesis of Synchronous Sequential Circuits

- Problem: Design a synchronous sequential circuit which allows to detect a sequence of three or more 1s in a row through a serial input.
  - The input is read in each clock rising edge.
  - The output is activated if the sequence is detected

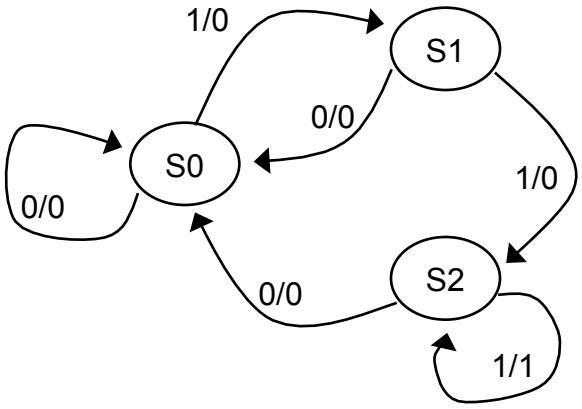


  - Example of inputs and outputs sequence:
    - X : 0 0 1 1 0 1 1 1 1 1 0 0 1 1 1
    - Z : 0 0 0 0 0 0 0 1 1 1 0 0 0 0 1

Synthesis of Synchronous Sequential Circuits

- **Example 1:** Mealy with D flip-flops:

1. State Transition Graph:



2. State Encoding:

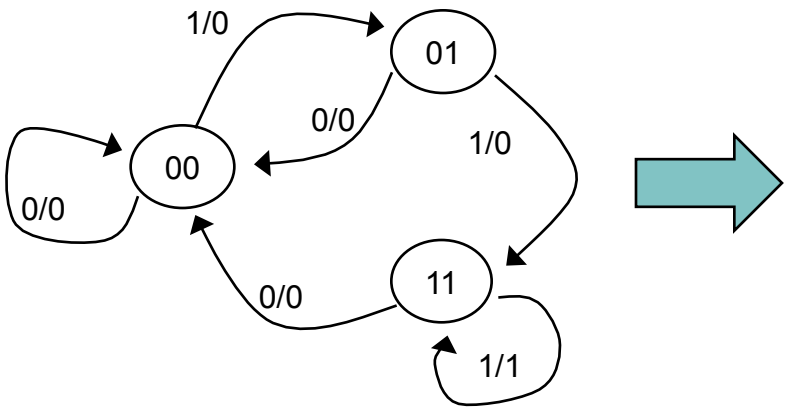
State	Q1	Q0
S0	0	0
S1	0	1
S2	1	1
	1	0

Unreachable state

Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops:

3. Transitions table and outputs table (merged together):



In	Q1	Q0	Q1+	Q0+	Out
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	X	X	X
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	X	X	X
1	1	1	1	1	1

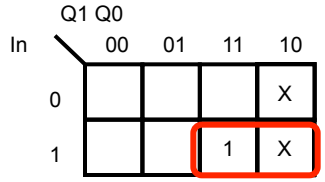
Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops:

4. Excitation table (D flip-flops):

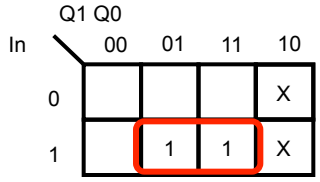
In	Q1	Q0	Q1+	Q0+	Out	D1	D0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	X	X	X	X	X
0	1	1	0	0	0	0	0
1	0	0	0	1	0	0	1
1	0	1	1	1	0	1	1
1	1	0	X	X	X	X	X
1	1	1	1	1	1	1	1

5. Output function:

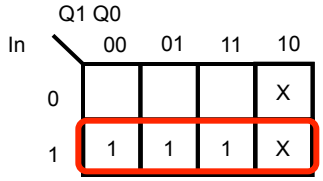


$$Out = Q_1 In$$

6. State functions



$$D_1 = Q_0 In$$

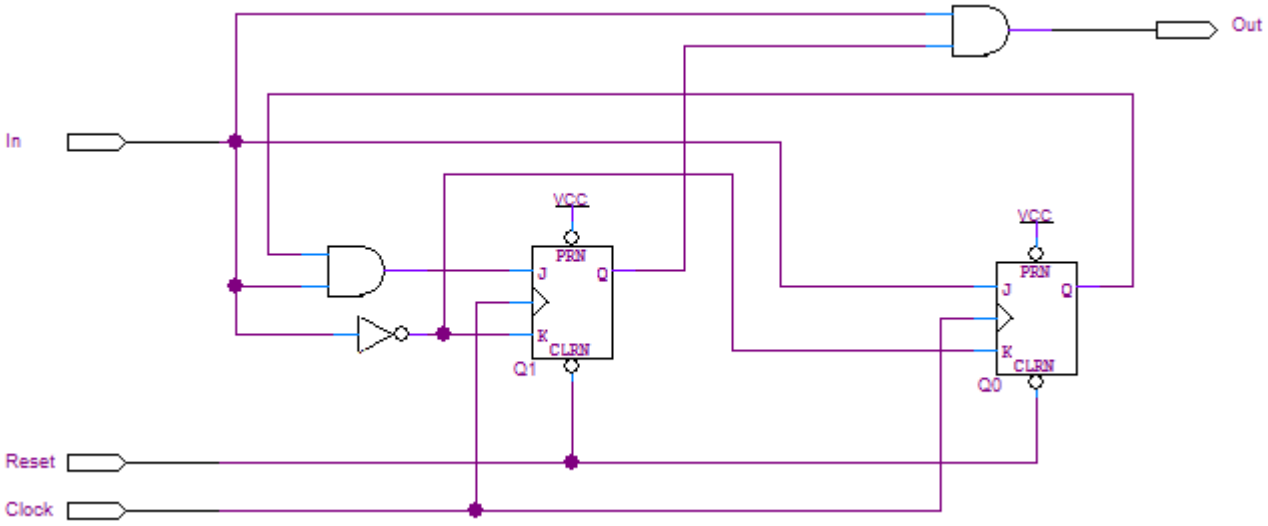


$$D_0 = In$$

Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops:

7. Implementation



$$Out = Q_1 In$$

$$D_1 = Q_0 In$$

$$D_0 = In$$

Synthesis of Synchronous Sequential Circuits

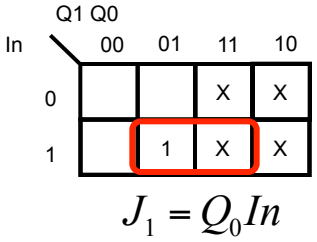
- **Example 2**. Mealy with J-K flip-flops:

4. Excitation table (J-K flip-flops):

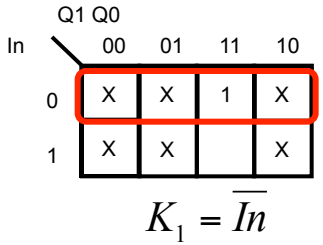
In	Q1	Q0	Q1+	Q0+	Out	J1	K1	J0	K0
0	0	0	0	0	0	0	X	0	X
0	0	1	0	0	0	0	X	X	1
0	1	0	X	X	X	X	X	X	X
0	1	1	0	0	0	X	1	X	1
1	0	0	0	1	0	0	X	1	X
1	0	1	1	1	0	1	X	X	0
1	1	0	X	X	X	X	X	X	X
1	1	1	1	1	1	X	0	X	0

5. Output function: $Out = Q_1 In$

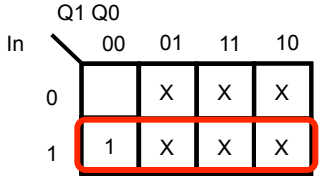
6. State functions:



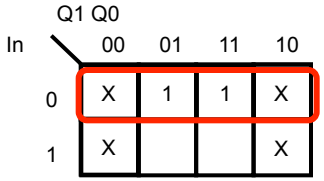
$J_1 = Q_0 In$



$K_1 = \overline{In}$



$J_0 = In$

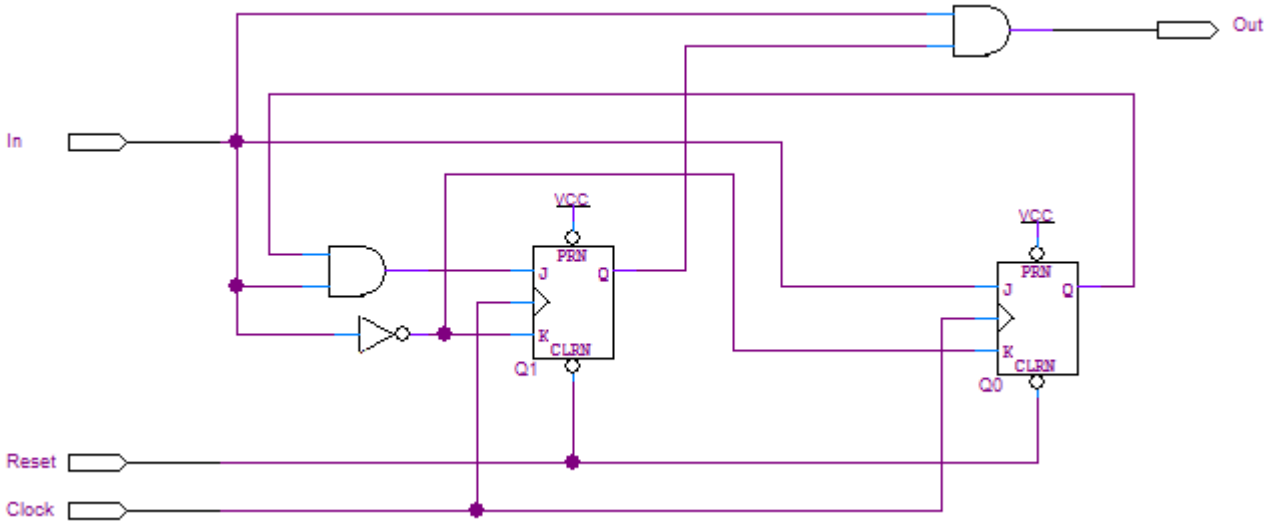


$K_0 = \overline{In}$

Synthesis of Synchronous Sequential Circuits

- Mealy with J-K flip-flops:

7. Implementation



$$Out = Q_1 In$$
$$J_0 = In$$
$$K_0 = \overline{In}$$
$$J_1 = Q_0 In$$
$$K_1 = \overline{In}$$

Synthesis of Synchronous Sequential Circuits

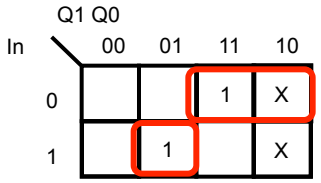
- **Example 3**. Mealy with T flip-flops :

4. Excitation table (T flip-flops):

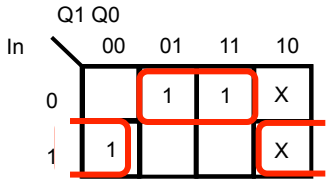
In	Q1	Q0	Q1+	Q0+	Out	T1	T0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1
0	1	0	X	X	X	X	X
0	1	1	0	0	0	1	1
1	0	0	0	1	0	0	1
1	0	1	1	1	0	1	0
1	1	0	X	X	X	X	X
1	1	1	1	1	1	0	0

5. Output function: $Out = Q_1 In$

6. State functions



$$T_1 = Q_1 \overline{In} + \overline{Q_1} Q_0 In$$

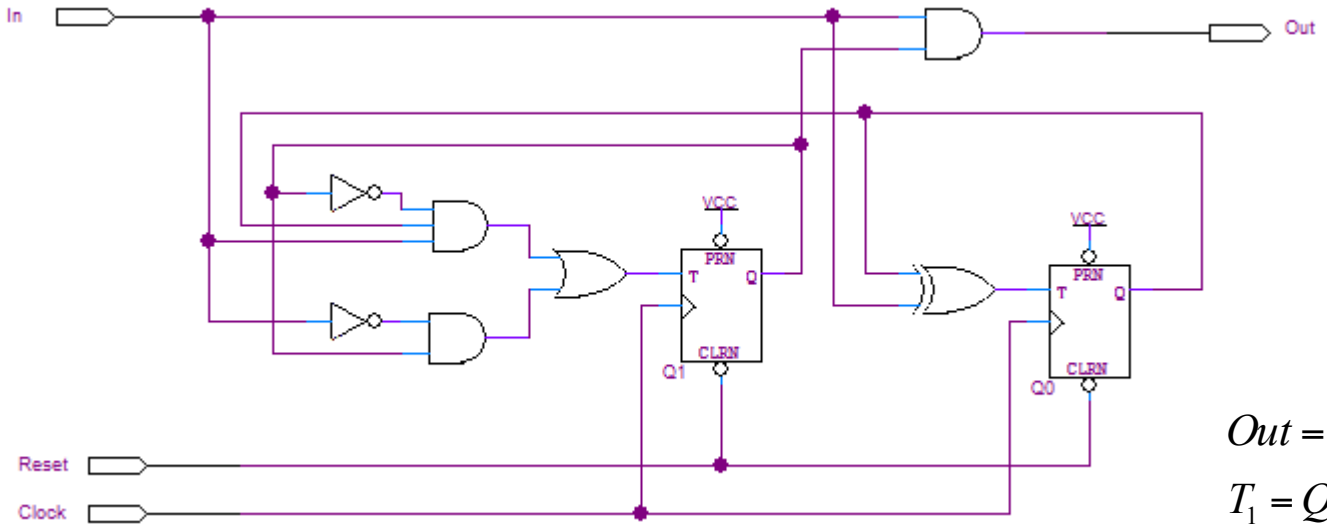


$$T_0 = \overline{In} Q_0 + In \overline{Q_0} = In \oplus Q_0$$

Synthesis of Synchronous Sequential Circuits

- Mealy with T flip-flops:

7. Implementation



$$Out = Q_1 In$$

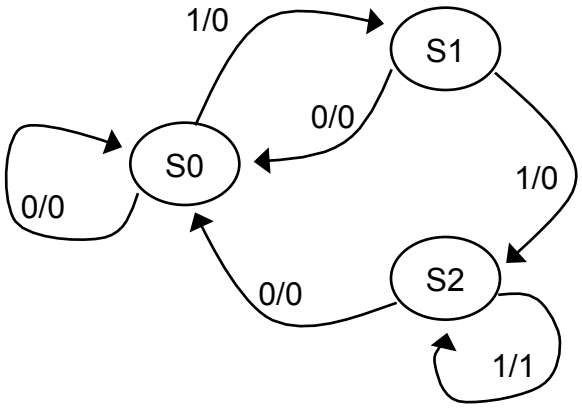
$$T_1 = Q_1 \overline{In} + \overline{Q_1} Q_0 In$$

$$T_0 = \overline{In} Q_0 + In \overline{Q_0} = In \oplus Q_0$$

Synthesis of Synchronous Sequential Circuits

- **Example 4:** Mealy, with a different state encoding:

1. State Transition Graph:



2. State Encoding:

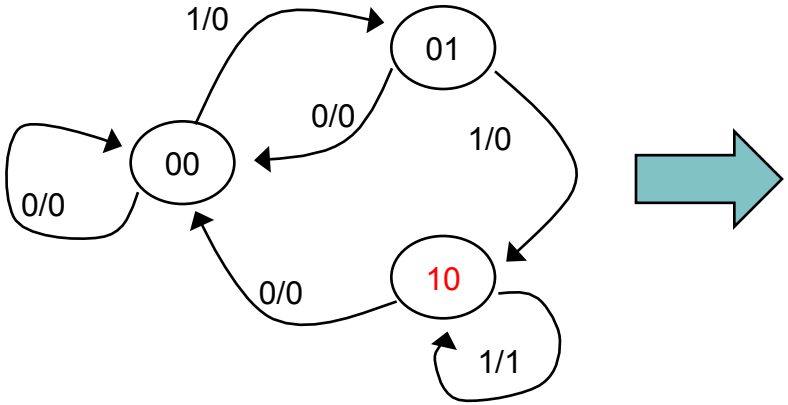
State	Q1	Q0
S0	0	0
S1	0	1
S2	1	0
	1	1

S2 is encoded with a different value

Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops (different encoding):

3. Transitions table and outputs table (merged together):
4. :



In	Q1	Q0	Q1+	Q0+	Out
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	X	X	X
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	X	X	X

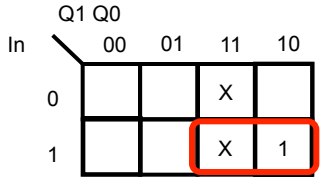
Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops :

4. Excitation table (D flip-flops):

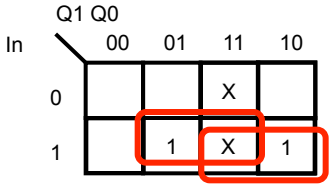
In	Q1	Q0	Q1+	Q0+	Out	D1	D0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	1	X	X	X	X	X
1	0	0	0	1	0	0	1
1	0	1	1	0	0	1	0
1	1	0	1	0	1	1	0
1	1	1	X	X	X	X	X

5. Output function:

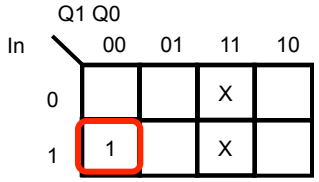


$$Out = Q_1 In$$

6. State functions



$$D_1 = Q_0 In + Q_1 In = In(Q_0 + Q_1)$$

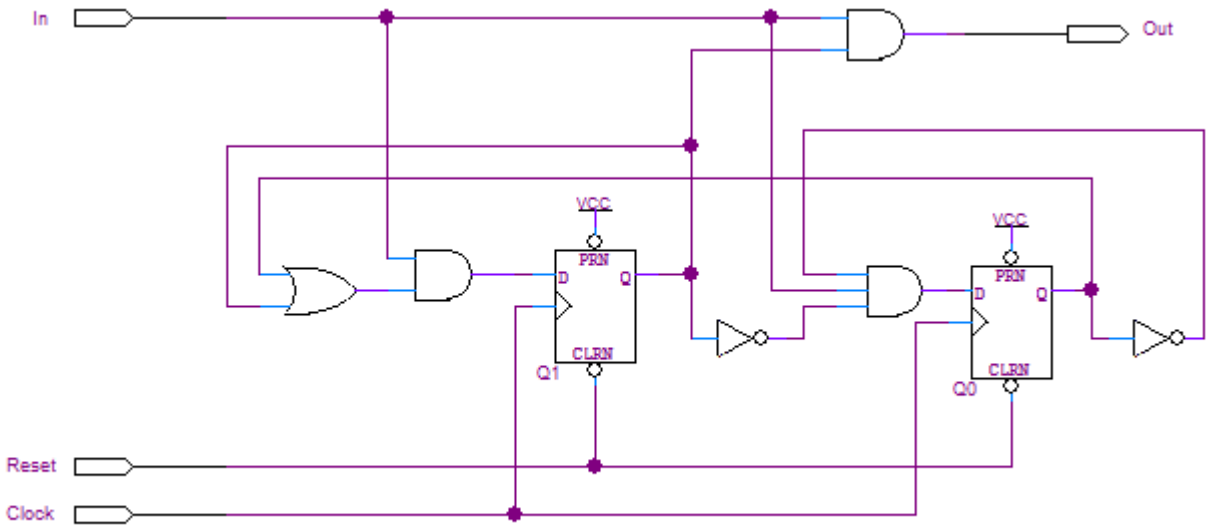


$$D_0 = \overline{Q_1}\,\overline{Q_0}\,In$$

Synthesis of Synchronous Sequential Circuits

- Mealy with D flip-flops (different encoding):

7. Implementación



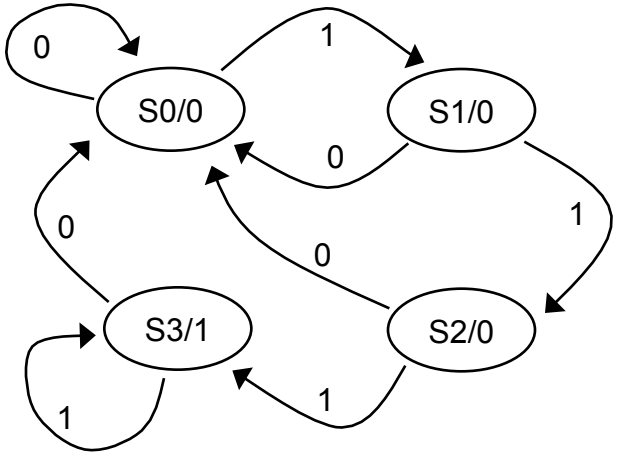
With this different encoding, more logic gates are requiered

$$Out = Q_1 In$$
$$D_1 = In(Q_0 + Q_1)$$
$$D_0 = \overline{Q_1}\,\overline{Q_0}\,In$$

Synthesis of Synchronous Sequential Circuits

- **Example 5:** Moore with D flip-flops:

1. State transition graph:



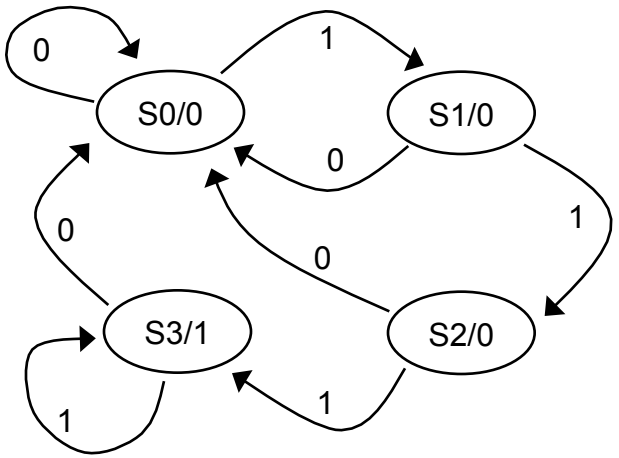
2. State encoding:

State	Q1	Q0
S0	0	0
S1	0	1
S2	1	1
S3	1	0

Synthesis of Synchronous Sequential Circuits

- Moore with D flip-flops:

  3. Transitions table and outputs table:



In	Q1	Q0	Q1+	Q0+
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	0

Q1	Q0	Out
0	0	0
0	1	0
1	0	0
1	1	1

Synthesis of Synchronous Sequential Circuits

- Moore with D flip-flops:

4. Excitation table (D flip-flops):

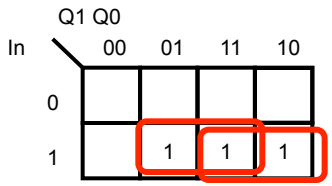
In	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	1
1	0	1	1	1	1	1
1	1	0	1	0	1	0
1	1	1	1	0	1	0

5. Output function:

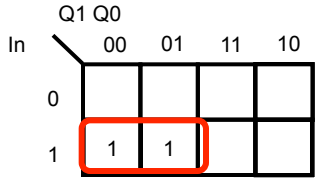
Q1	Q0	Out
0	0	0
0	1	0
1	0	0
1	1	1

$$Out = Q_1 Q_0$$

6. State functions



$$D_1 = Q_0 In + Q_1 In =$$
$$= (Q_0 + Q_1) In$$

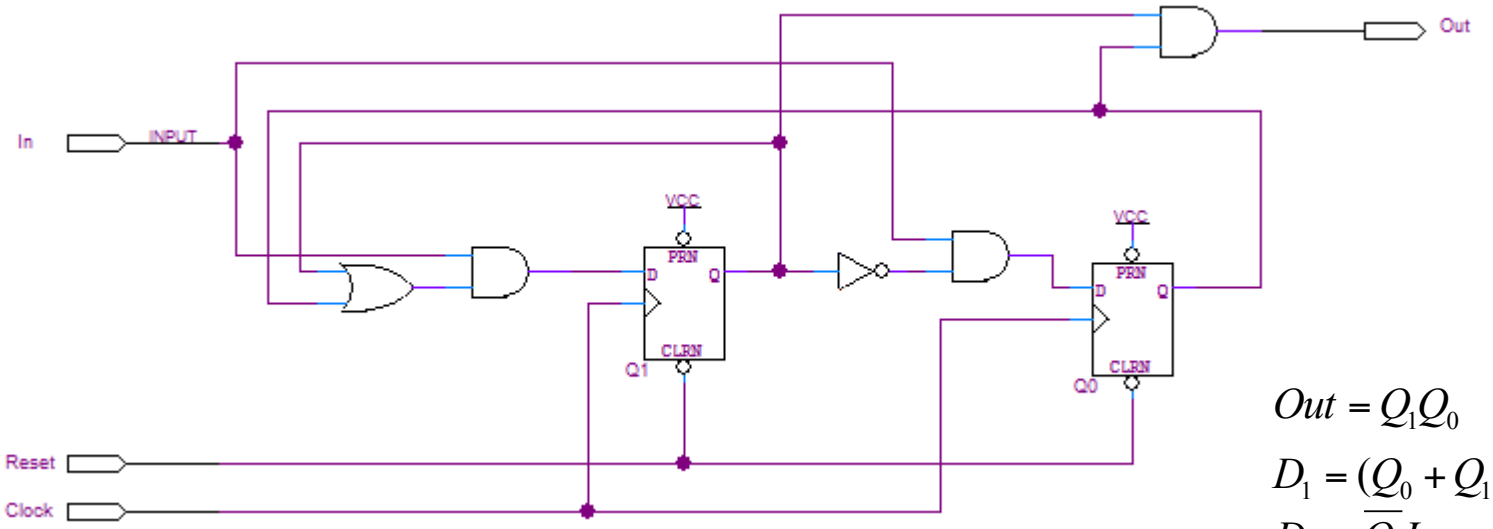


$$D_0 = \overline{Q_1} In$$

Synthesis of Synchronous Sequential Circuits

- Moore with D flip-flops:

7. Implementation



$$Out = Q_1 Q_0$$

$$D_1 = (Q_0 + Q_1)In$$

$$D_0 = \overline{Q_1} In$$