1. Implement, with the minimum possible number of transistors, a 2-input multiplexer using:

   a) CMOS technology
   b) Transmission gates

   Hint: Multiplexer equation: $Y = \overline{S}A + SB$
   Data inputs: A, B, Selection input: S. Output: Y.

2. We wanto to design a **128M x 32 bits** RAM memory. We have the following available chips:

   4 chips of 32 M x 8 bits.
   2 chips of 32 M x 16 bits.
   4 chips of 16 M x 32 bits.

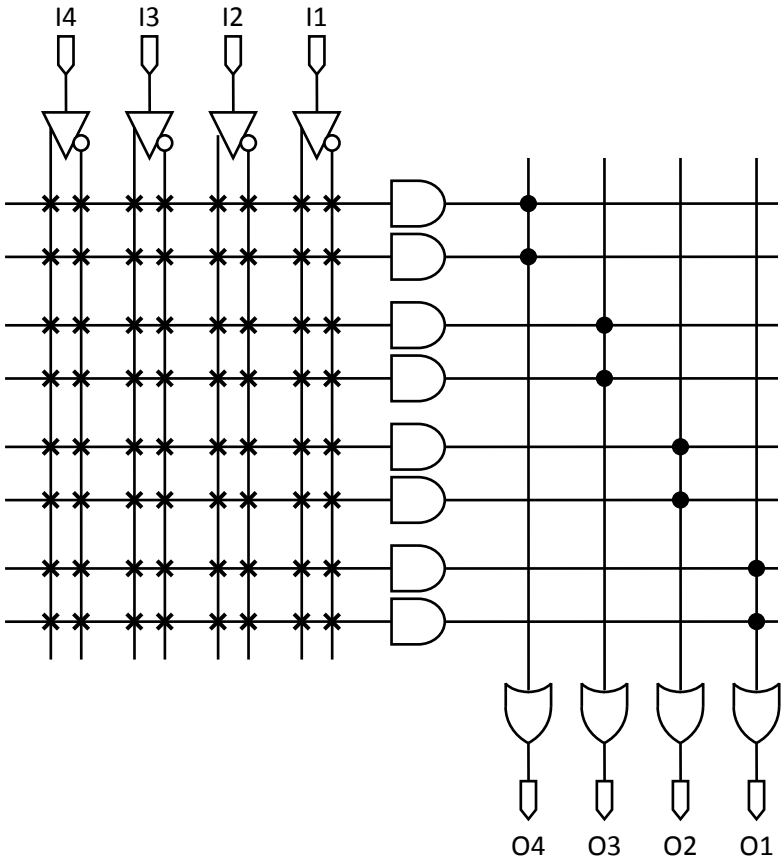
   Each chip has a **CS'** pin (active-low Chip Select), an **R/W'** pin (read/write) and an **OE'** pin (Output Enable).

   a) Draw the memory map with the necessary blocks, showing the first and last addresses of each block (binary and hexadecimal). Specify the type of chip used in each block.
   b) Design the circuit, showing:
      1. Chip used for each case (32M x 8, 32M x 16 ó 16M x 32).
      2. First and last lines of addresses and data for each chip.
      3. Address and data buses, indicating the first and last lines.
      4. Decoding logic to activate the CS' of each circuit.

3. A system memory is going to be implemented with the following requirements:
   - 16 bits word length.
   - 16K PROM in the lower part of the memory.
   - 16K SRAM immediately after the 16K PROM
   - 32K EEPROM in the upper part.

   The following memory modules are available: 16K×8 PROM, 16K×16 SRAM and 32K×16 EEPROM. All the control inputs of the memory modules are active-high.

   Find:
   a) The number of address lines of the system.
   b) The number of memory modules of each type that are needed.
   c) Draw the memory map and point out the addresses (in hexadecimal) for the first and last positions in each of the memory modules.
   d) Design the decoding circuitry of the memory using the programmable device shown in Figure P3.2 with the minimum number of necessary logic gates. Use the following sheet for the implementation of the decoding circuitry and hand it with the rest of the problem solution. Circle in the Figure the connections to be programmed in the programmable device.

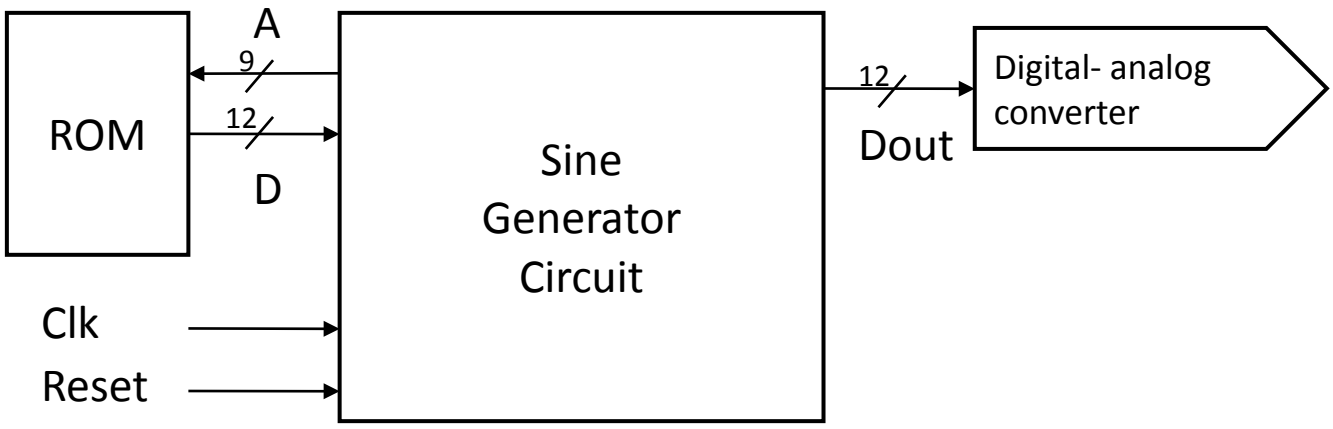


4. A sinusoidal periodic signal is going to be generated with a digital circuit and a digital-analog converter, as shown in the figure. The circuit will use an external 512x12 ROM memory which stores a table of values of the first quadrant of the sine function (between 0 and $\pi/2$), in particular:

$$2^{10} * \text{Sine}\,(\pi/2 * A/256), \qquad A \in [0, 256],$$

where A is the address of the ROM memory. Please note that the highest possible value is 210 = 010000000000, which is reached for A=256.

The circuit must read iteratively from the memory and generate periodically the DOUT output for the four quadrants of the sine.



The inputs and outputs of the circuit are:

CLK: Clock signal

Reset: Asynchronous initialization signal

A: 9-bit memory address

D: Data provided by the memory (12 bits)

DOUT: Output data to the converter in 2s-complement (12 bits)

Find:

a) Draw a block diagram for the circuit pointing out clearly:

   a. The components that have been used. Any of the digital components studied during the course can be used. **It is not necessary to implement these components with logic gates.**
   b. The signals that have been used. Point out the purpose of each of them.
   c. In case of using a state machine, draw its diagram.

b) If CLK has a frequency f, ¿Which is the frequency of the generated sinusoidal signal? Figure out how the design should be modified so that the frequency of the generated signal could be programmable and externally configurable.