

Memories

© Luis Entrena, Celia López, Mario García,
Enrique San Millán

Universidad Carlos III de Madrid

Outline

- Introduction. Memory types
- Characteristics of memories
- Internal organization of a memory
- Random Access Memories (RAM)
- Read Only Memories (ROM)
- Extension of memory size
- Memory access chronograms
- Other applications of memories

Memories

- Devices for masive storage of information
- They are a fundamental component of digital systems
- There are many types of memories. They can be classified according to several parameters:
 - Physical property exploited to store information
 - Access features, permanence of information, etc.

Types of memories

- Magnetic memories:
 - Magnetization patterns on surface covered by a magnetic material
 - Examples: hard disk, floppy disk, magnetic tape, etc.
- Optical memories:
 - Information is recorded by a laser that generates tiny holes on a surface. Reading is performed by illuminating with a laser and measuring the reflective properties of the surface
 - Examples: CD, DVD
- Semiconductor memories
 - Electronic circuits
 - *We will focus on these types of memories*

Semiconductor memories

- RAM memory (Random Access Memory)
 - Memories for reading and writing
 - Example: computer main memory
- ROM memory (Read Only Memory)
 - Read only memory
 - Contents fixed during manufacturing or programmable
 - Example: Flash memory

Characteristics of memories

- Capacity: amount of stored information
 - Data width: number of bits that can be accessed at the same time
 - Typically powers of 2: 1, 2, 4, 8, 16, 32
 - 1 Byte = 1B = 8 bits
 - Number of positions: Typically powers of 2
 - $2^{10} = 1.024 = 1K$ (Kilo)
 - $2^{20} = 1.048.576 = 1M$ (Mega)
 - $2^{30} = 1.073.741.824 = 1G$ (Giga)
 - $2^{40} = 1.099.511.627.776 = 1T$ (Tera)
 - Capacity = <Number of positions>x<data width>
 - Example: 16Mx8

Characteristics of memories

- Access time:
 - Time required to access one memory datum
 - May be different for reading and writing
- Access mode:
 - Sequential or serial: it can be accessed only in a particular order. Access time varies depending on the position to be accessed
 - Example: magnetic tape
 - Random: it can be accessed in any order. Access time is the same for all positions.
 - Example: computer main memory

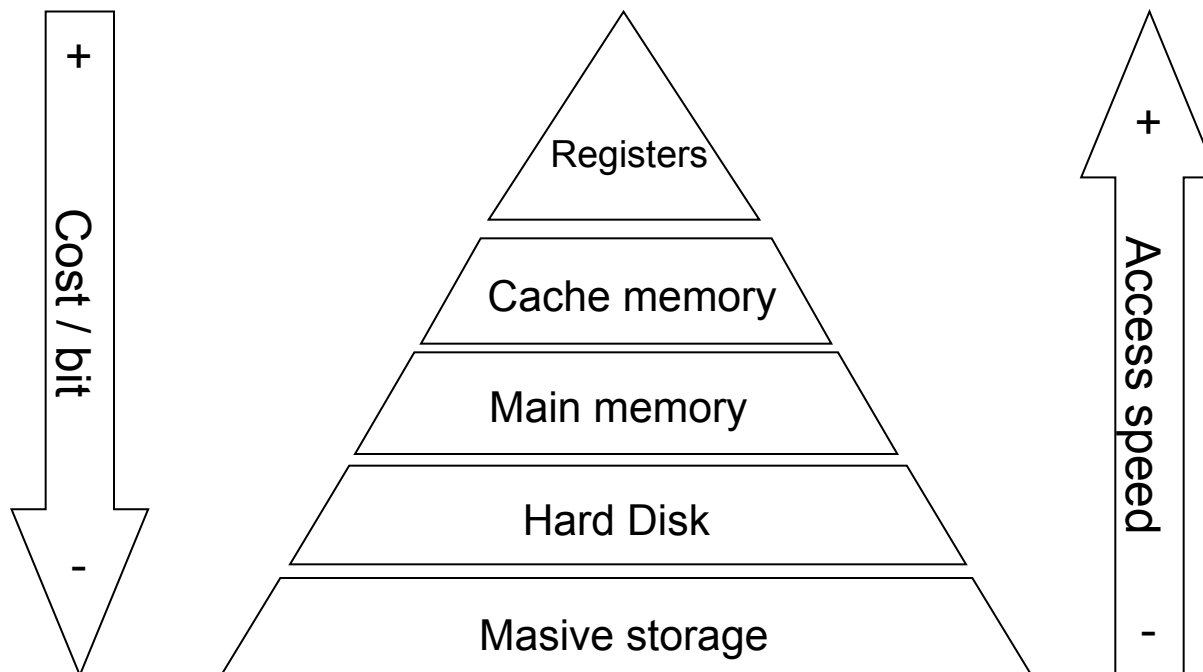
Characteristics of memories

- Permanence or data stability:
 - Non volatile memory: keeps the stored information even if it is not constantly supplied with electric power
 - Example: Flash memory
 - Volatile memory: requires constant power to maintain the stored information. Information is lost if it is disconnected from the power supply
 - Example: static RAM (cache memory)
 - Dynamic memory: Information is lost after some time, even when constantly connected to the power supply
 - Need periodic refresh of stored information
 - Example: dynamic RAM (computer main memory)

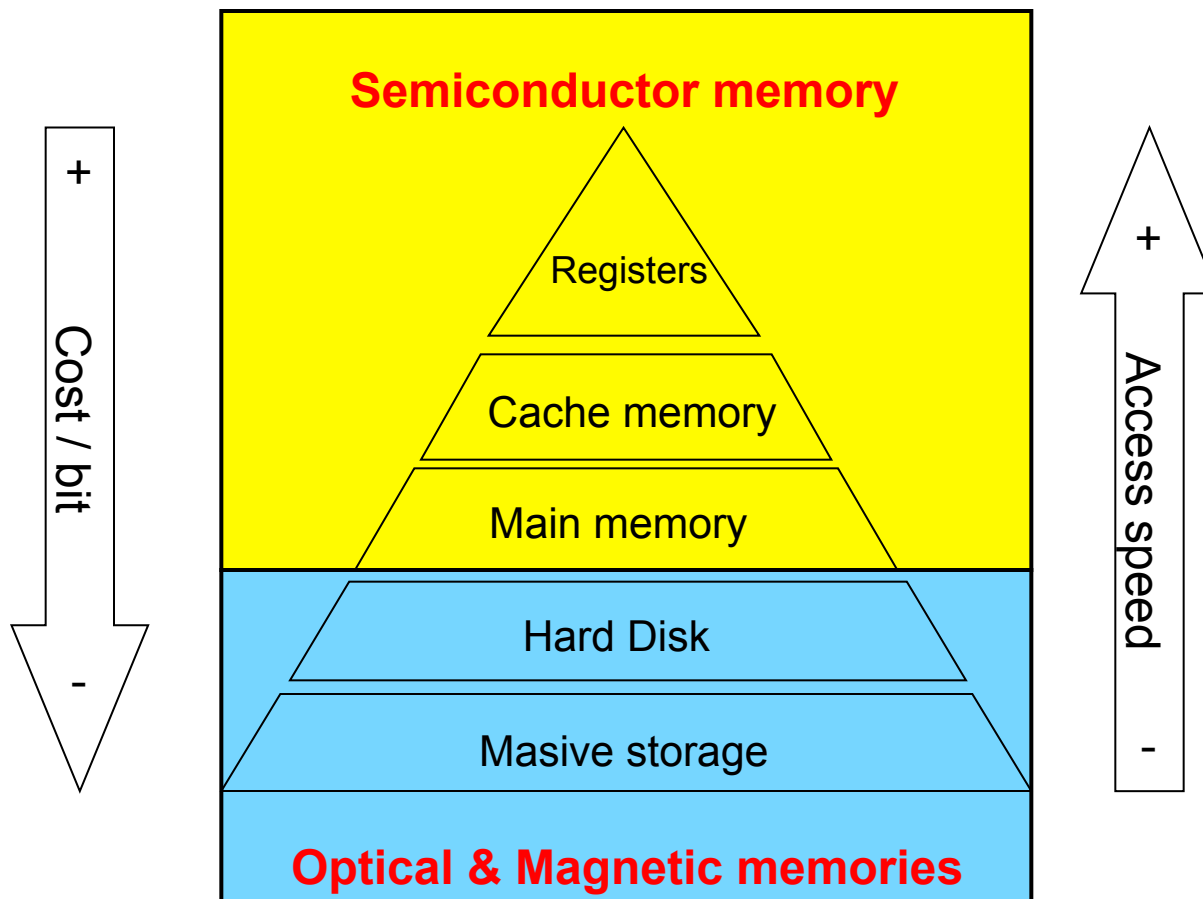
Characteristics of memories

- Other characteristics that can determine the selection of a memory for a particular application:
 - Cost/bit
 - Power consumption
- No single type of memory is the best with respect to all characteristics!
 - The most suitable memory type, or a hierarchical combination of memories, should be used for each application

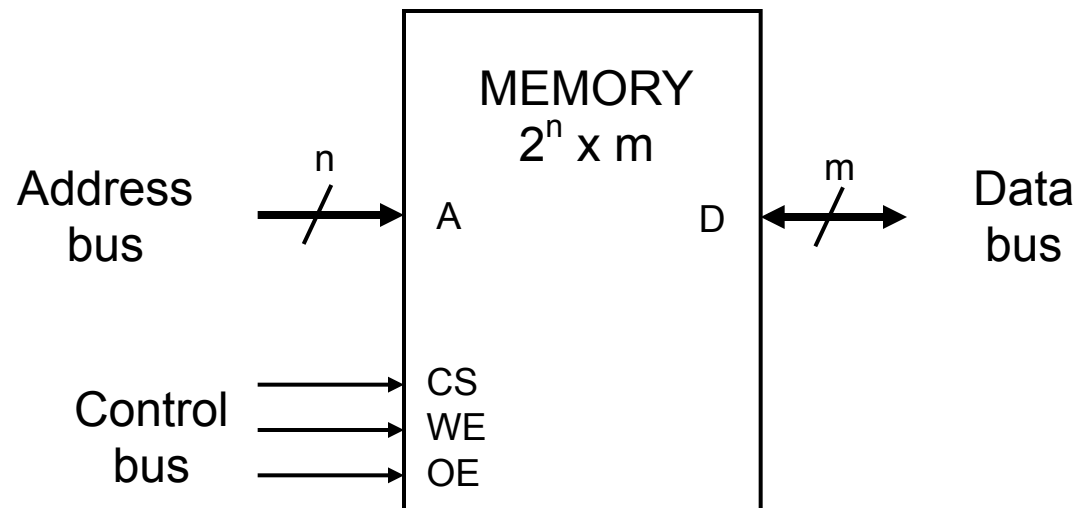
Memory hierarchy



Memory hierarchy



Memory organization: interface



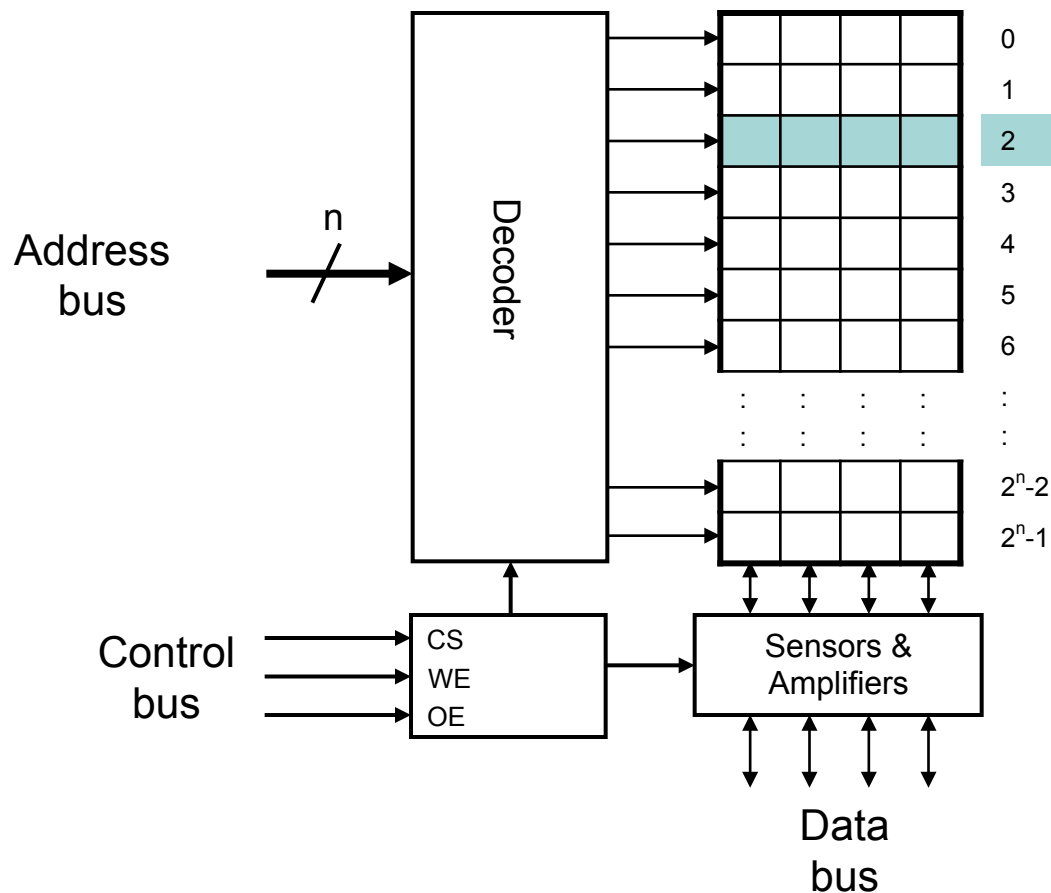
Memory organization: interface

- Address bus (A): Sets the position to access
 - n bits wide for a memory with 2^n positions
 - Example: 20 bits for 1M, 30 bits for 1G
- Data bus (D): Provides the datum
 - Data bus width (m) is equal to data size
 - Input data for writing
 - Output data for reading
 - Can be a single bidirectional bus, or two buses, one input bus and one output bus

Memory organization: interface

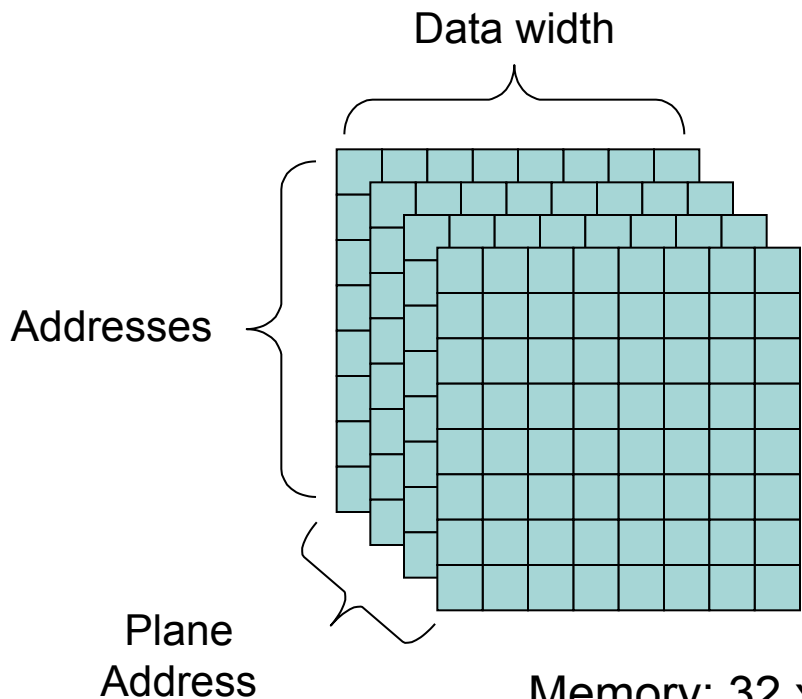
- Control bus: signals that control memory operation. Some typical signals:
 - CS (Chip Select) or CE (Chip Enable): when deasserted, data bus is typically in tristate mode
 - R/W (Read/Write) or WE (Write Enable): selects the memory operation (read or write)
 - OE (Output Enable): Enables data output. When deasserted, data bus is typically in tristate mode
 - RAS (Row Address Strobe) and CAS (Column Address Strobe) in memories with 3D organization
 - Other signals: CLK in synchronous memories, BE (Byte Enable) to select particular bytes in a memory word, etc.

Memory organization: internal structure

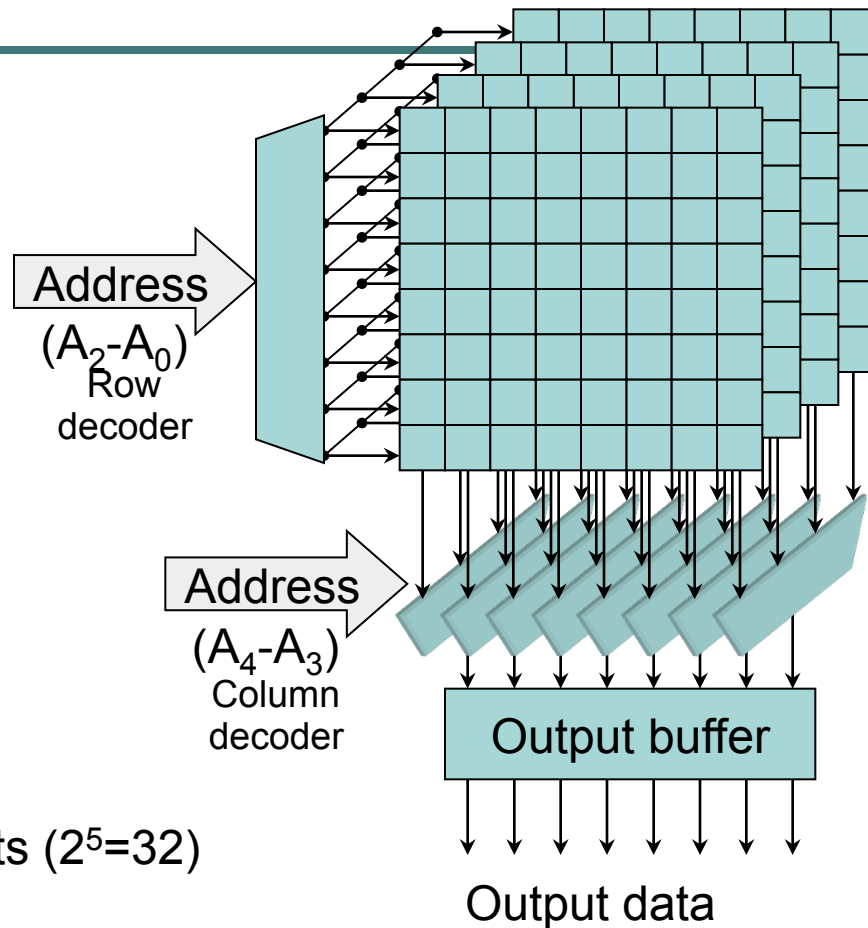


3D Organization

Data access



Memory: 32 x 8
 Address bus: 5 bits ($2^5=32$)
 Data bus: 8 bits
 Size: $32 \cdot 8 = 256$ bits



RAM memory

- Read & Write memory
- Two main types:
 - Static RAM (SRAM): every bit is stored in a bistable
 - Dynamic RAM (DRAM): every bit is stored in a capacitor
- Currently, the most widely used type of DRAM is DDR (Double Data Rate) SDRAM
 - 3D organization
 - Clocked memory (Synchronous DRAM)
 - Data access in both clock edges (Double Data Rate)
 - 64 bits wide data
 - Versions evolving on time: DDR, DDR2, DDR3, DDR4

RAM memory

- Advantages and disadvantages:

	SRAM	DRAM
Capacity (number of bits)		✓
Speed	✓	
Cost/bit		✓
Power consumption		✓
Volatile	YES	YES
Refresh	NO	YES
Application example	Cache	Main memory

ROM memory

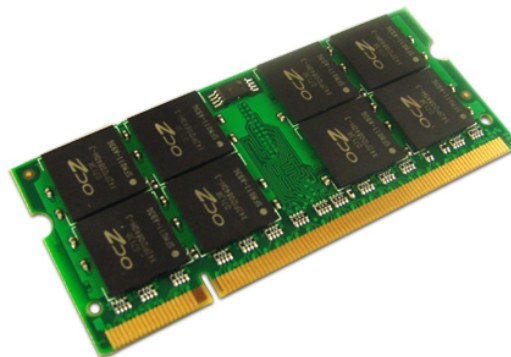
- Read Only Memory
- Non volatile
- Types
 - Mask programmable: contents fixed by manufacturing
 - One-Time Programmable: contents fixed by the user
 - Erasable or Reprogrammable: can be erased to store new contents
- The concepts of “writing” and “programming” should be distinguished, although the frontier is becoming blurred:
 - Writing is an operation similar to reading
 - Programming uses physical means different from reading, it is generally slower and it must be applied on a block basis or even for the entire chip

Types of ROM memory

Type	Meaning	Read	Programmable	Erasable (Reprogrammable)
ROM	Read Only Memory	Random	No (mask prog.)	No
PROM	Programmable ROM	Random	One-Time Prog. (OTP)	No
EPROM	Erasable Programmable ROM	Random	Electrically	UV light
EEPROM	Electrically Erasable Programmable ROM	Random	Electrically	Electrically
NOR Flash	Cells in parallel	Random	Electrically	Electrically
NAND Flash	Cells in series	Serial	Electrically	Electrically

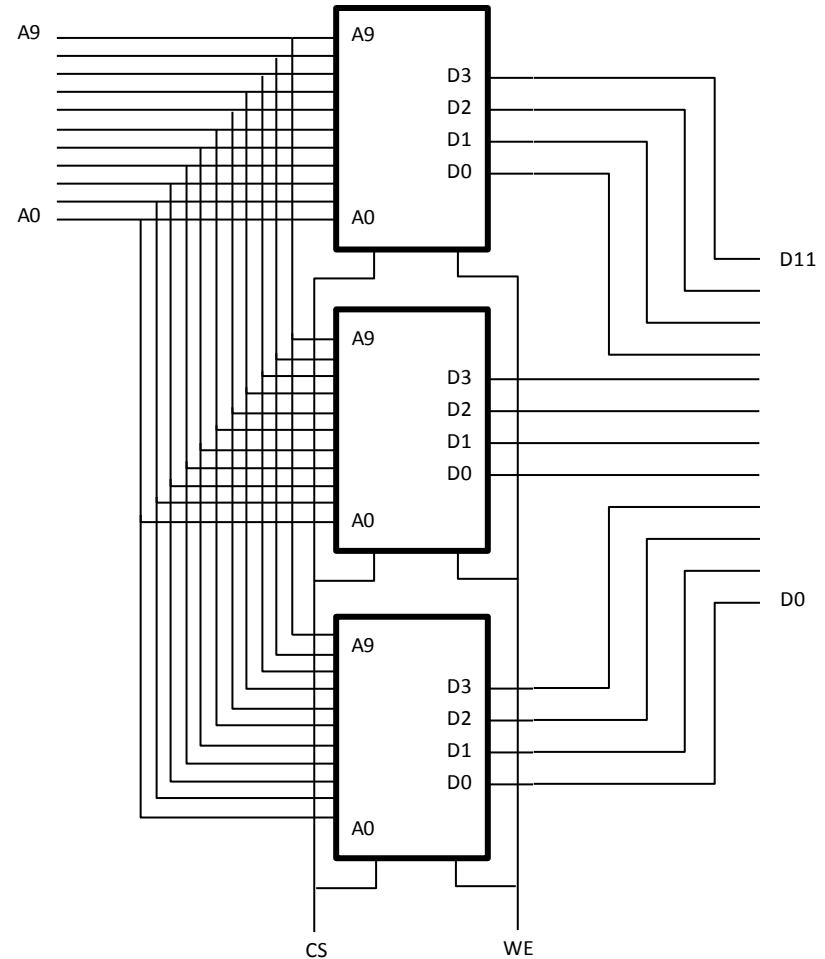
Memory expansion

- ¿How can we build large memories from available memory chips?
 - Data bus expansion
 - Address bus expansion
 - Data and address bus expansion
- Memory expansion is common practice (example: DIMM modules)



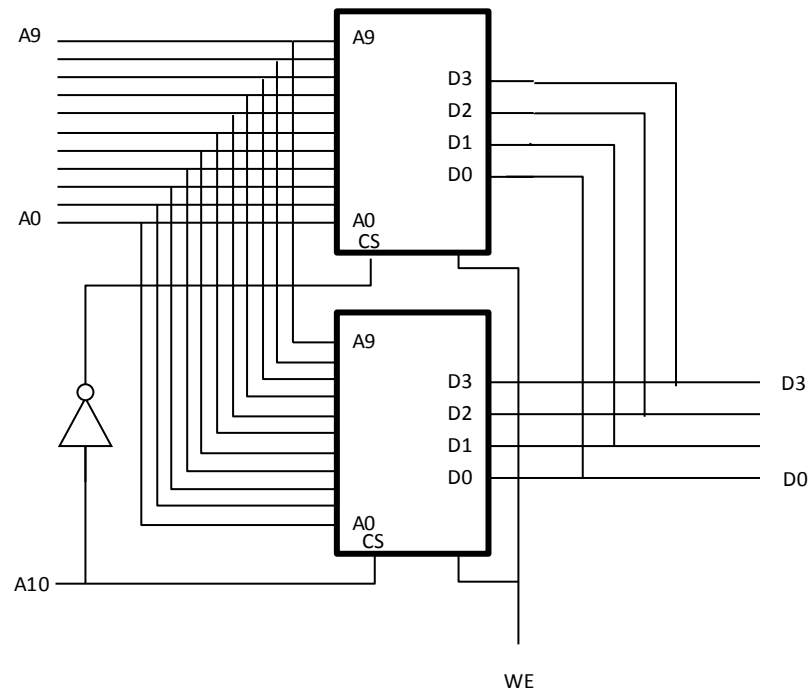
Data bus expansion

- Common address and control buses
- Data bus is formed by the union of chip data buses:
 - Every chip provides a portion of the data bus



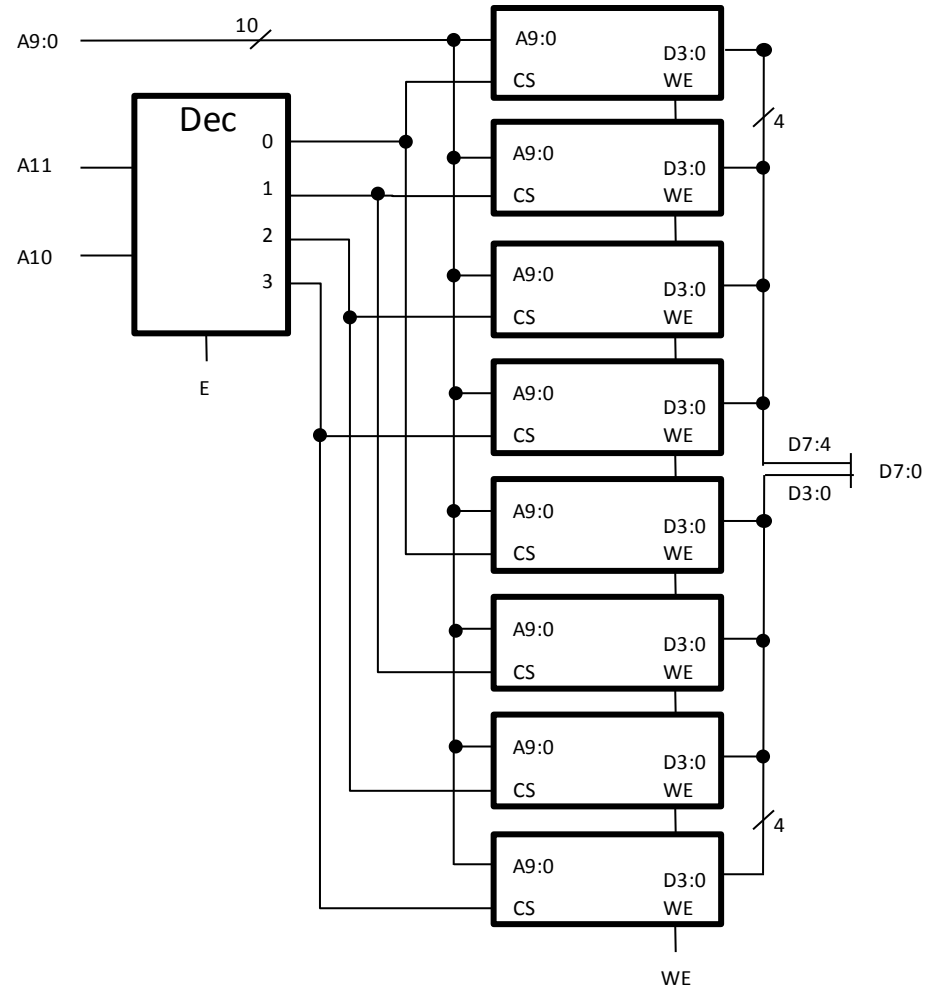
Address bus expansion

- Common data and control buses
- Address bus:
 - Every chip provides a portion of the address space
 - MSB address bits are decoded to select a chip
 - LSB address bits are common to all chips: they provide the address for each chip



Data bus and address bus expansion

- Combination of data and address bus expansion



Memory map

- Address range of each memory chip

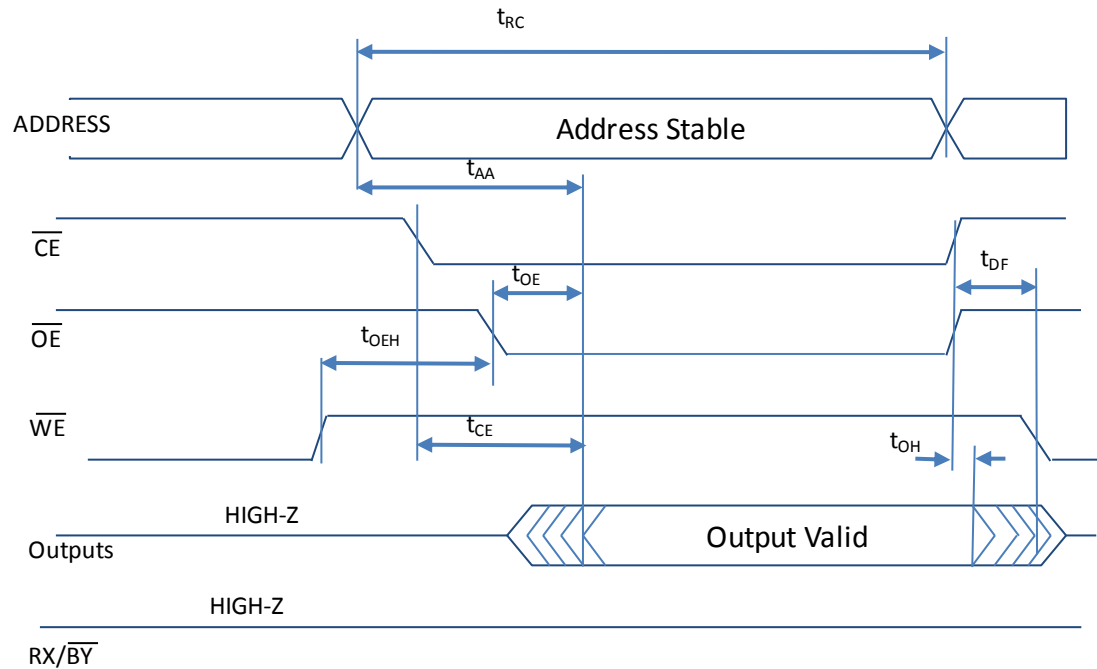
	Address	Address (bin)		
	(hex)	A16	A16	A14...A0
ROM (64K)	00000h	0	0	0...0
	0FFFFh	0	1	1...1
RAM (32K)	10000h	1	0	0...0
	17FFFh	1	0	0...0
RAM (32K)	18000h	1	1	0...0
	1FFFFh	1	1	1...1

$$64K = 2^6 \cdot 2^{10} = 1 \cdot 2^{16} = 10000h$$

$$32K = 2^5 \cdot 2^{10} = 2^3 \cdot 2^{12} = 08000h$$

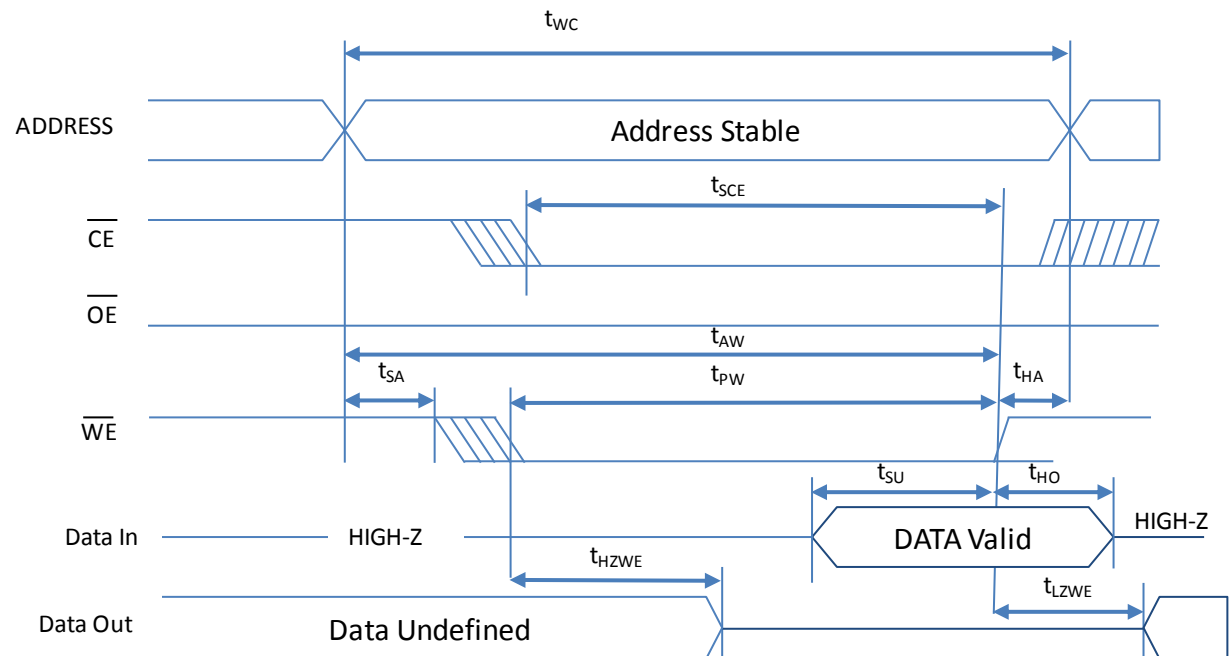
Chronogram: read cycle

- t_{RC} : Min. Read Cycle time
- t_{AA} : Read access time



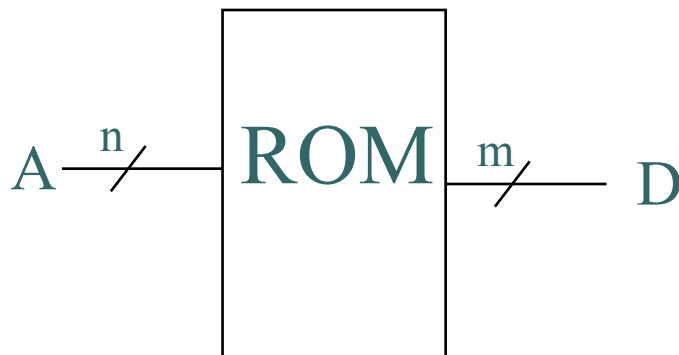
Chronogram: write cycle

- t_{WC} : Min. Write Cycle time
- t_{pW} : Min. Write Pulse time
- t_{SU} : Setup time
- t_{HO} : Hold time



Other applications of memories

- Memories can be used to implement logic functions
- Implementation of a function is achieved by storing its truth table
- A memory used to store a truth table is called a Look-Up Table (LUT)
- The memory size required to implement a logic function increases exponentially with the number of input variables.

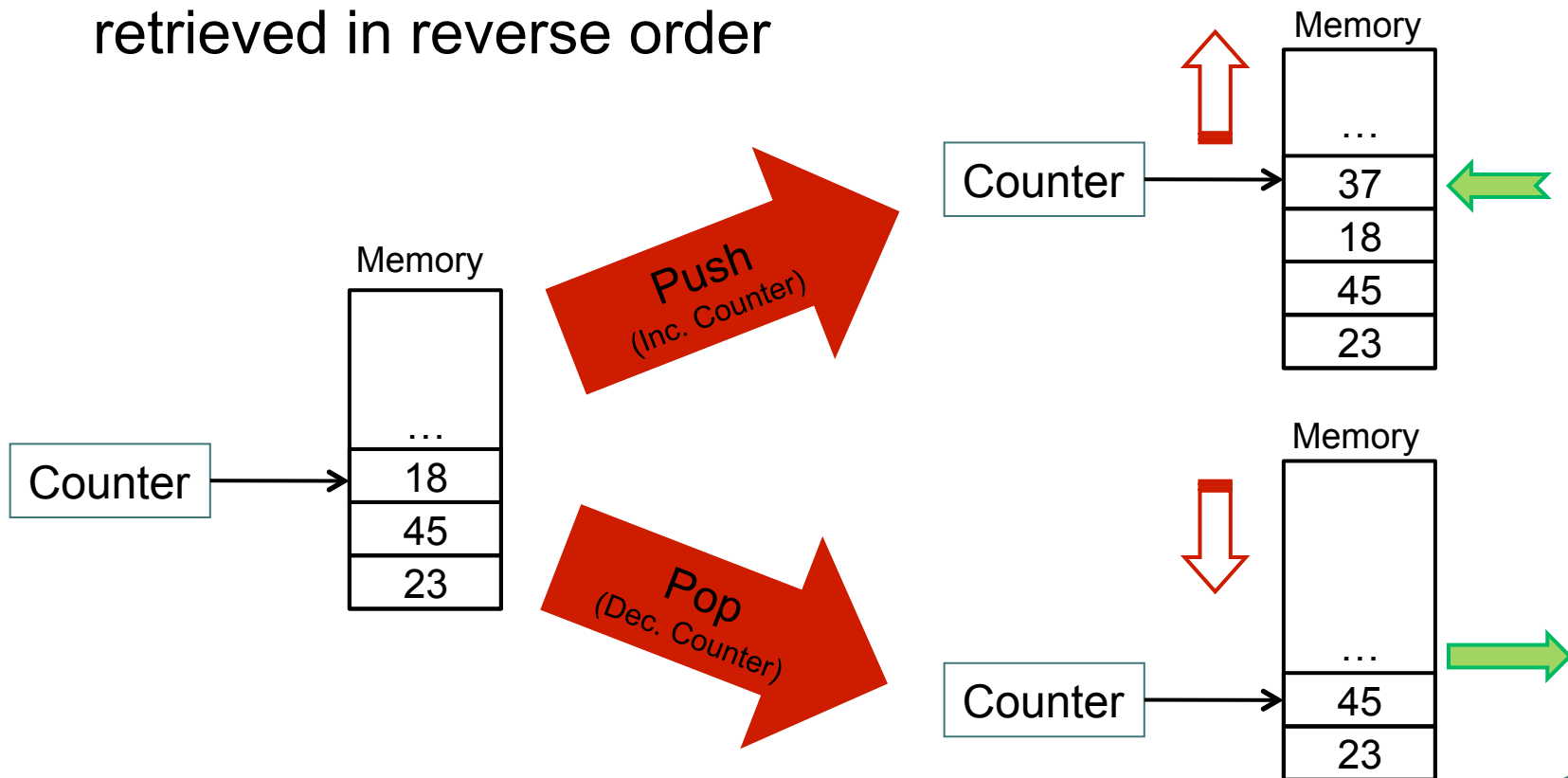


m functions of n variables

$$(D_{m-1}, \dots, D_0) = f(A_{n-1}, \dots, A_0)$$

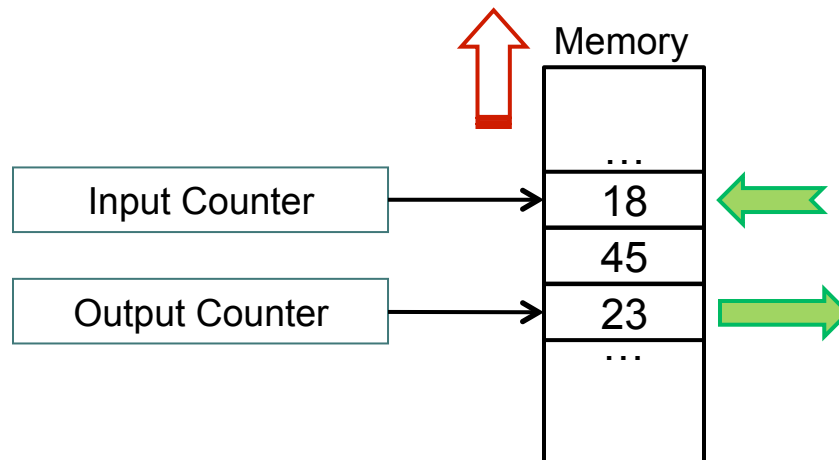
LIFO Memory

- LIFO (Last In First Out): Data are stored and then retrieved in reverse order



FIFO memory

- FIFO (First In First Out): Data input and output in the same order, but at different time
- Application: Temporal storage to accommodate different data rates



References

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