Programmable Logic Devices

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Outline

- Tecnologies for implementing programmable circuits
- Simple Programmable Logic Devices
- Complex Programmable Logic Devices:
  - CPLD
  - FPGA

Digital Circuit Implementation

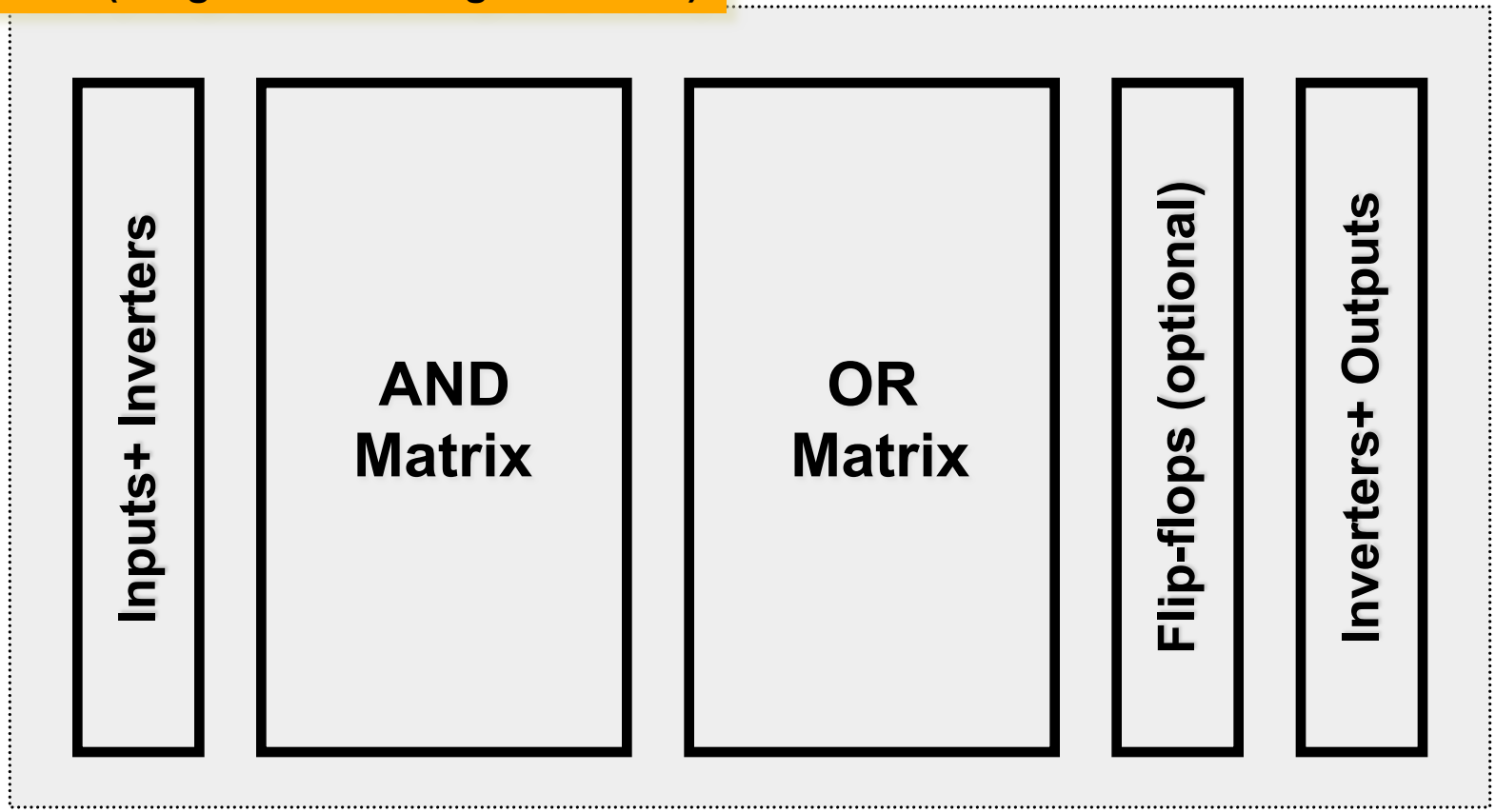
- Dicrete logic
- Application Specific Integrated Circuits (ASIC)
- Programmable Logic Devices (PLD)
  - Simple
    - PROM: Programmable Read Only Memory
    - PLA: Programmable Logic Array
    - PAL: Programmable Array Logic
    - GAL: Generic Array Logic
  - Complex
    - CPLD: Complex Programmable Logic Device
    - FPGA: Field Programmable Gate Array

Tecnologies

- Floating gate MOS transistor (EPROM-FLASH)
  - When transistor gate is overvoltaged, the switch is permanently open or closed, behaving as programmable connection
- Static RAM (SRAM)
  - Memory can be used as combinational logic.
  - LUTs (Look-Up Tables): 4, 5, 6 inputs.
- Antifuse
  - When fused, an antifuse produces a short-circuit.
  - Fuses offer lower resistance than diodes used in classic PLDs, and thus better performance

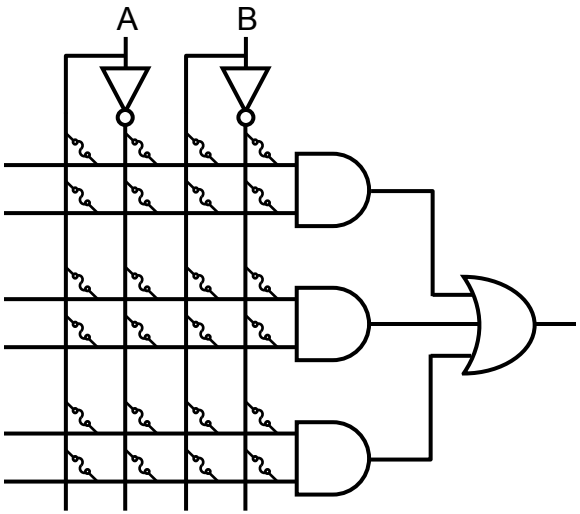
Simple Programmable Circuits

PLDs (Programmable Logic Devices)

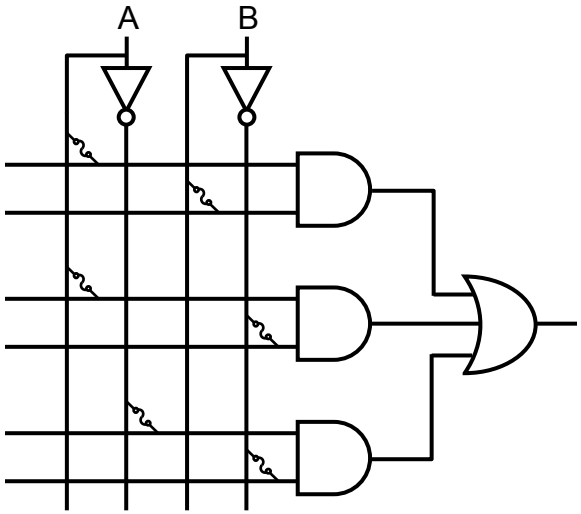


Programmable matrixes

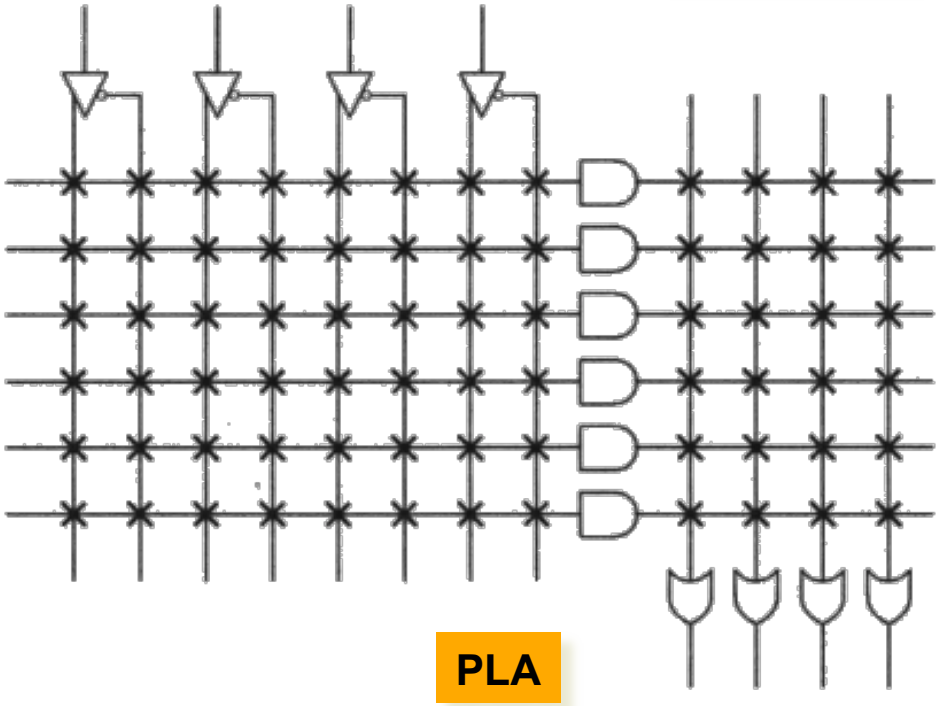
AND matrix with fixed OR



Function X=A*B+A*NOT(B)+NOT(A)*NOT(B)



Programmable matrixes

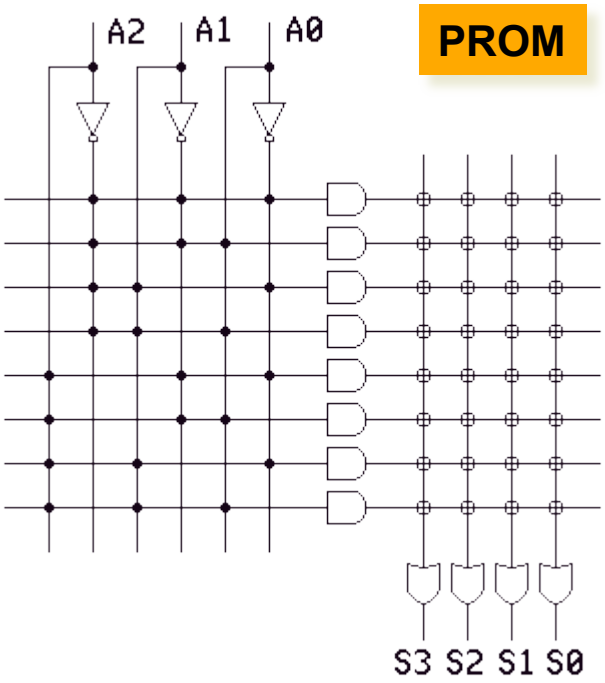


Types of PLD

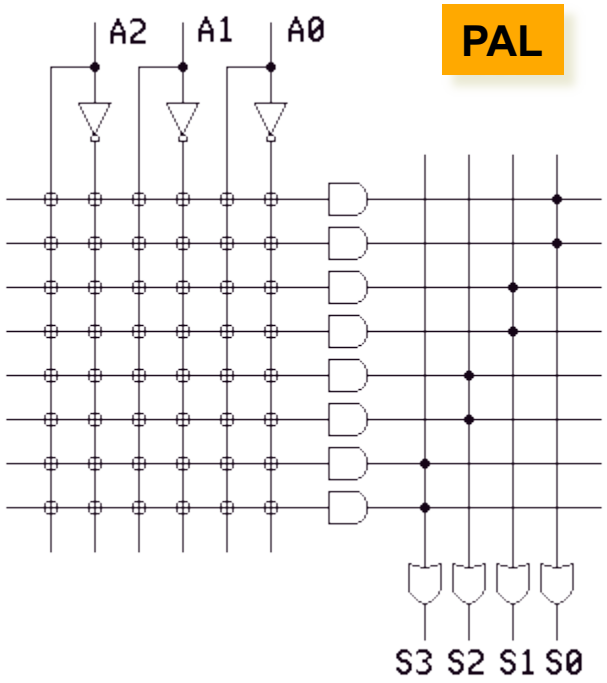
	Matriz AND	Matriz OR
PROM	Fixed	Programmable
PLA	Programmable	Programable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

- Simplified notation for connections

Kinds of PLDs



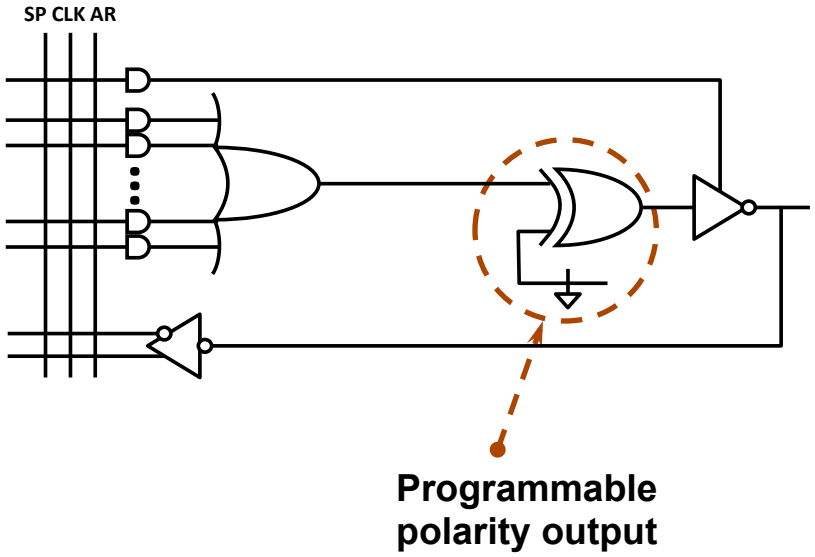
- Fixed AND matrix (address decoder)
- Programmable OR matrix (data)



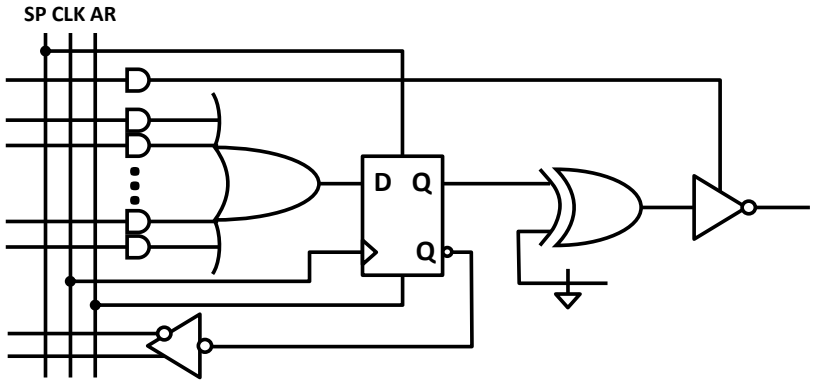
- Programmable AND matrix
- Fixed OR matrix

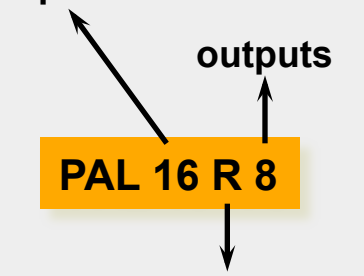
Output blocks

Combinational input-output



Registered output





Name convention

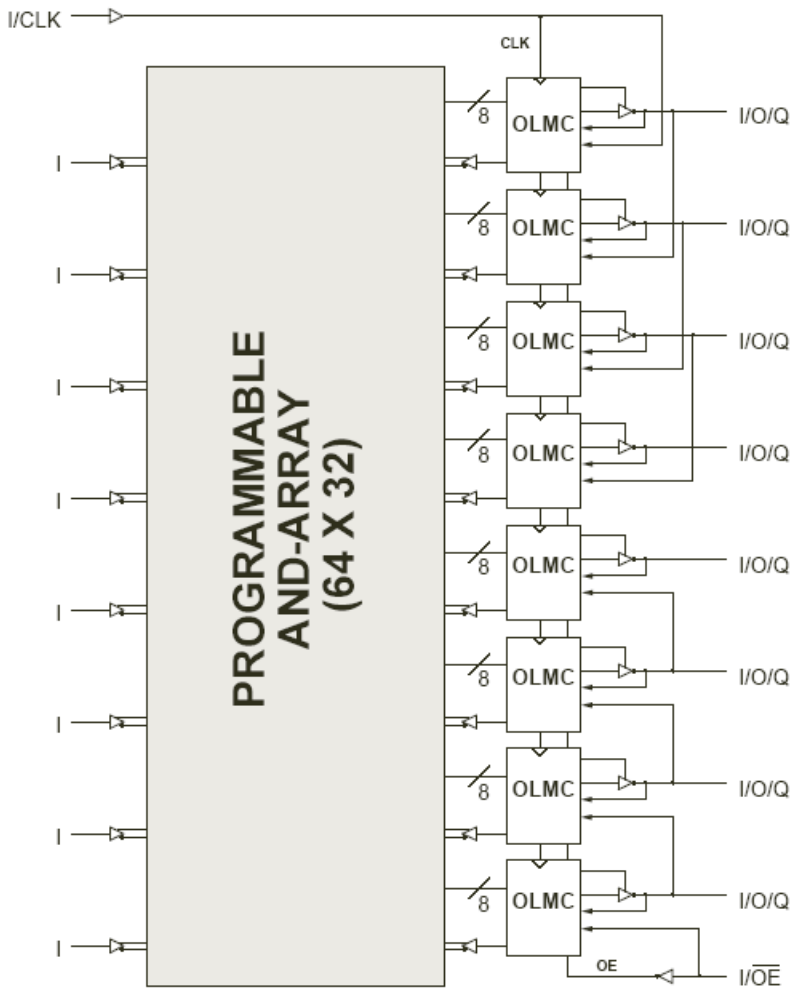
L: active Low

H: active High

P: programmable polarity

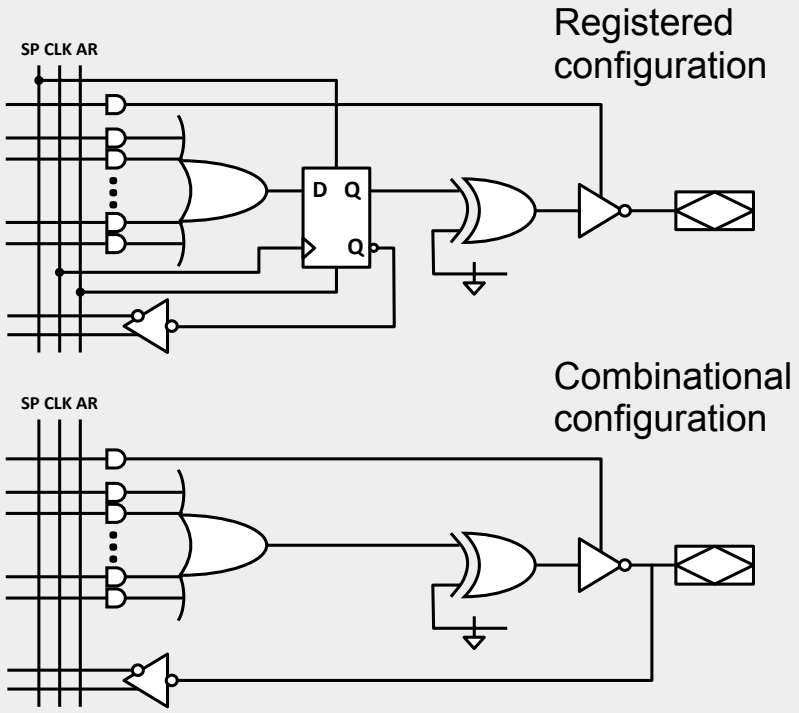
R: registered

GAL (Generic Array Logic)



PAL-like architecture, but with programmable output functions.

OLMC: Output Logic Macrocell

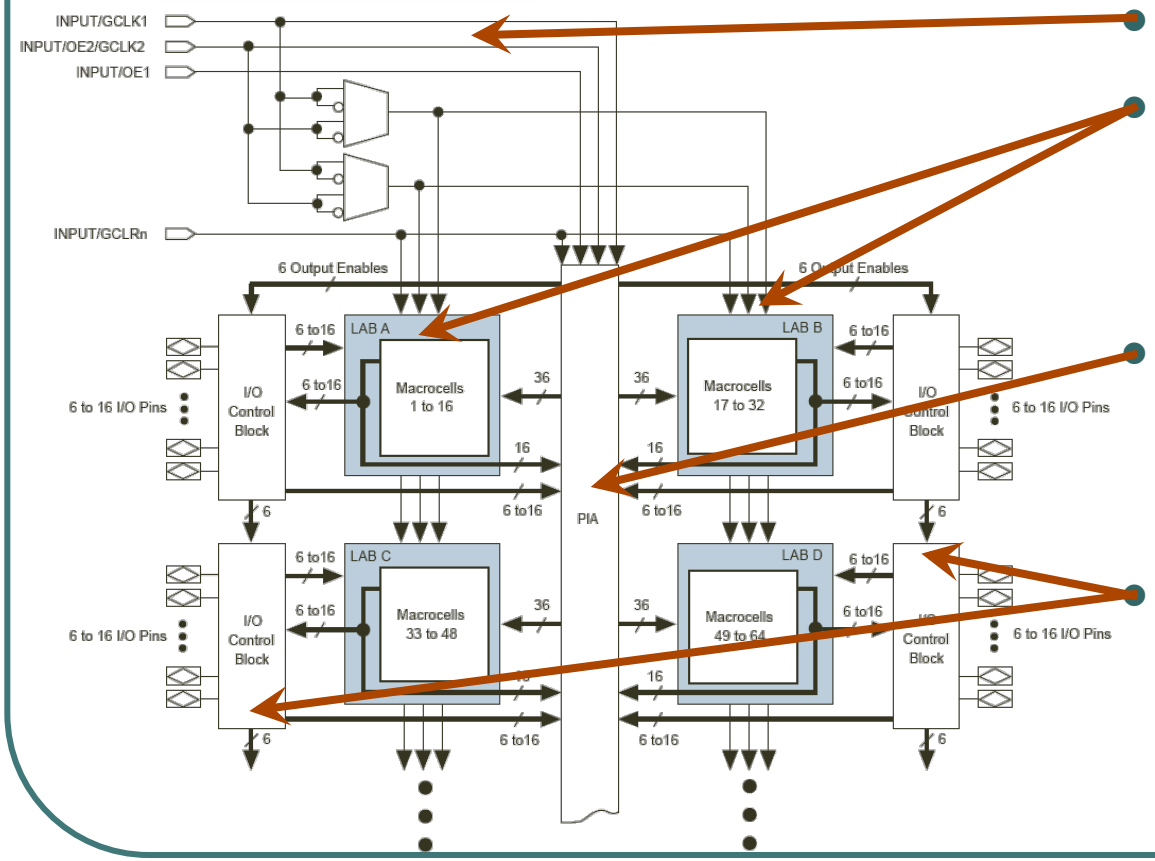


Complex Programmable Logic Devices

- CPLD:
  Complex Programmable Logic Devices
- FPGA:
  Field Programmable Gate Array
- Different from simple PLDs
  - Complex arquitecture
  - Higher amount of logic resources
- CPLD & FPGA manufacturers
  - Xilinx
  - Altera
  - Actel
  - Atmel
  - Lattice
  - Cypress

CPLD: architecture

Altera MAX 7000



Global signals

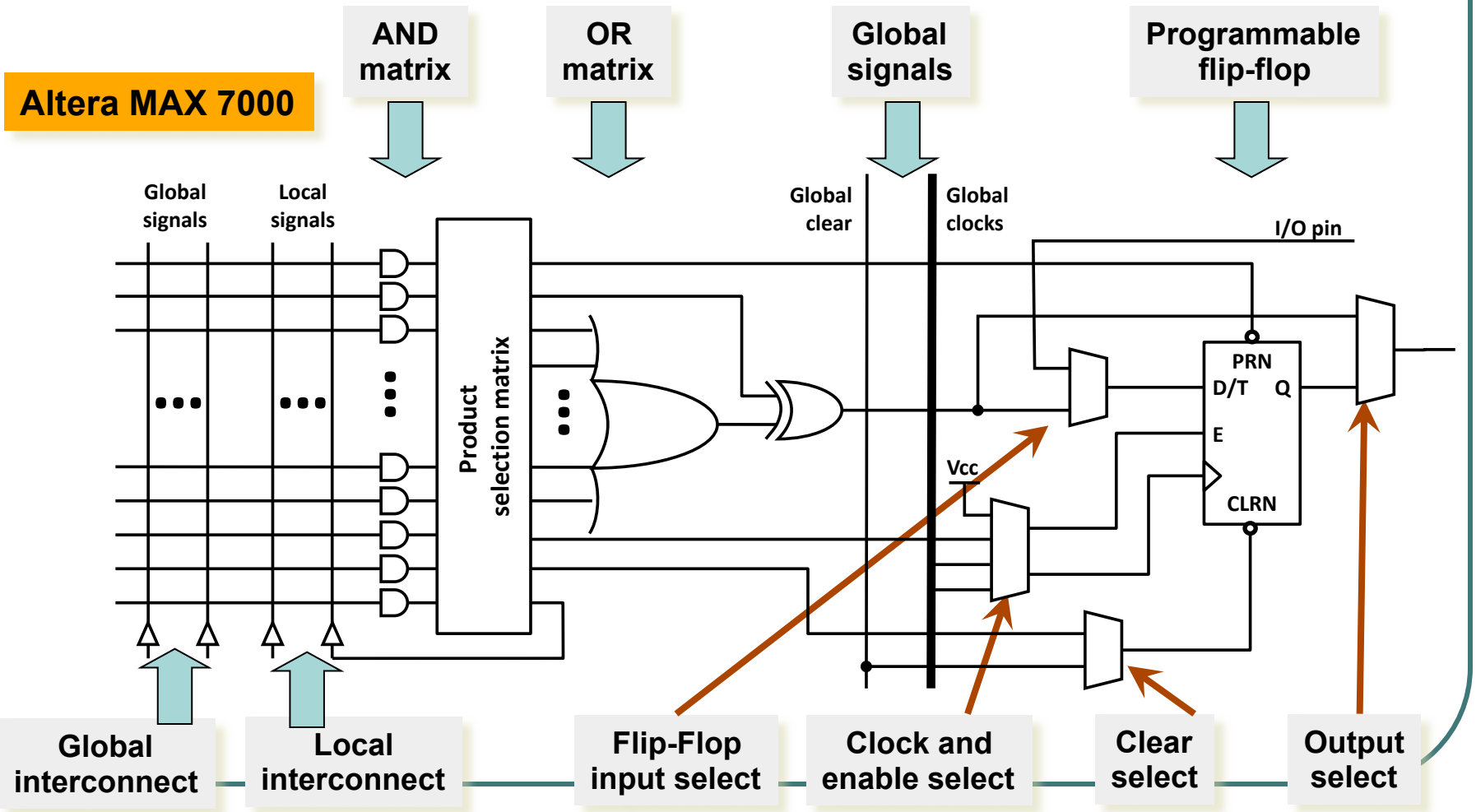
LAB, Logic Array Blocks
1 LAB = 16 macrocells

PIA, Programmable Interconnect Array

Input/Output blocks

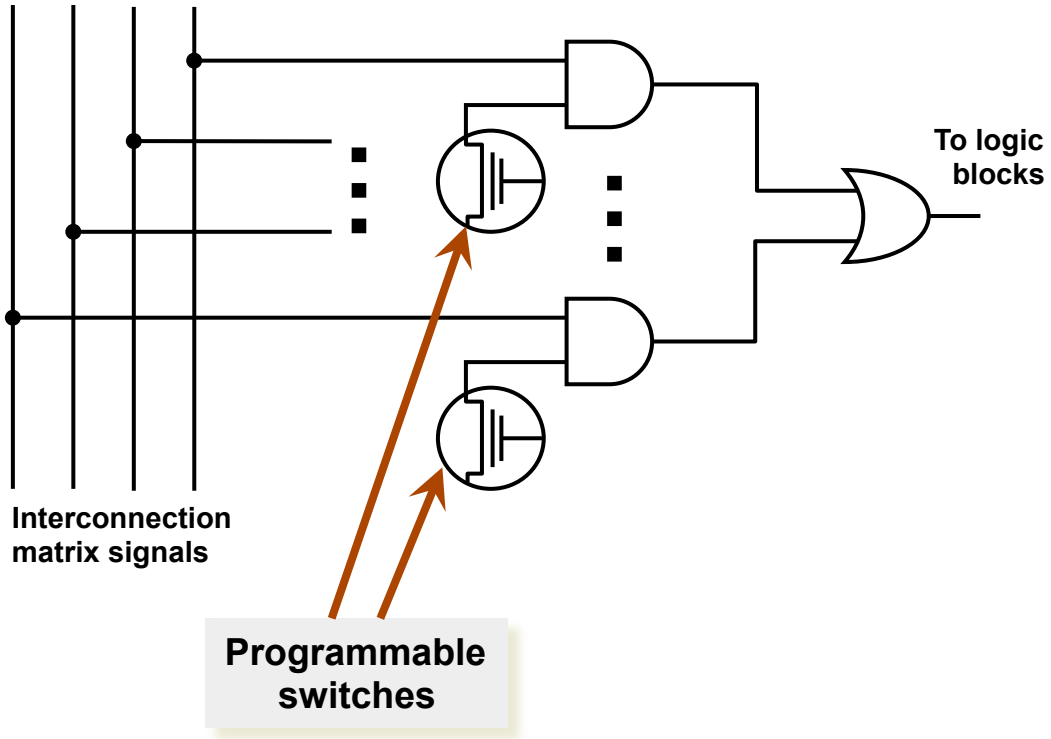
Figure extracted from “MAX 7000 Programmable Logic Device Family Data Sheet”, version 6.6, Altera Corporation, june 2003.

CPLD: macrocell



CPLD: interconnection matrix

Global Interconnection Matrix (PIA)



- PIA inputs
  - I/O pins
  - LAB outputs
- PIA outputs
  - LAB inputs

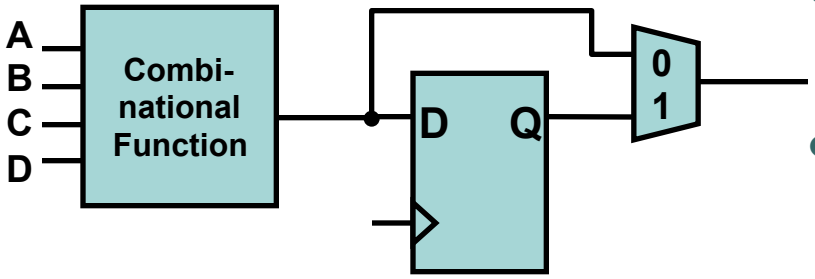
CPLD: characteristic briefing

- PAL structure, with registers and interconnection logic
- Medium capacity (up to 25,000 equivalent gates)
- Medium/high speed
- High power comsumpsion
- EPROM technology (reprogrammable, non volatile)
- Cheap
- Size limited by interconnection matrix
- ISP (In-System Programming). JTAG.

FPGAs

- Field Programmable Gate Arrays
- Designed to overcome CPLD size limitations, using advanced architectures
- High variety of logic resources
  - Combinacional logic
  - Sequencial logic
  - RAM memory
  - Clock managers
  - Global signals
  - Multipliers
- Manufacturers
  - Xilinx
  - Altera
  - Actel
  - Atmel

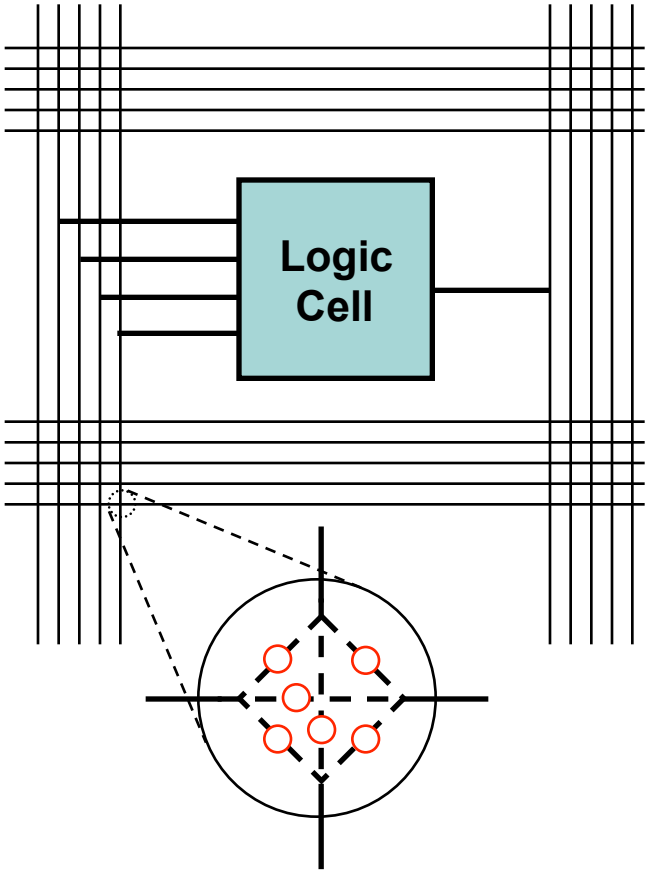
FPGA: basic logic cell



- Combinacional function + flip-flop
- Other possibilites:
  - 2 CF + 1 FF
  - 2 CF + 2 FF
- Aditional functionality:
  - Carry logic
  - 6 and 8 input CF
  - Several clock and reset signals
  - Different flip-flop configuration: level (latch), rising, edge, falling edge

- Combinational Function:
  - LUT (Look-Up Table): SRAM, volatile

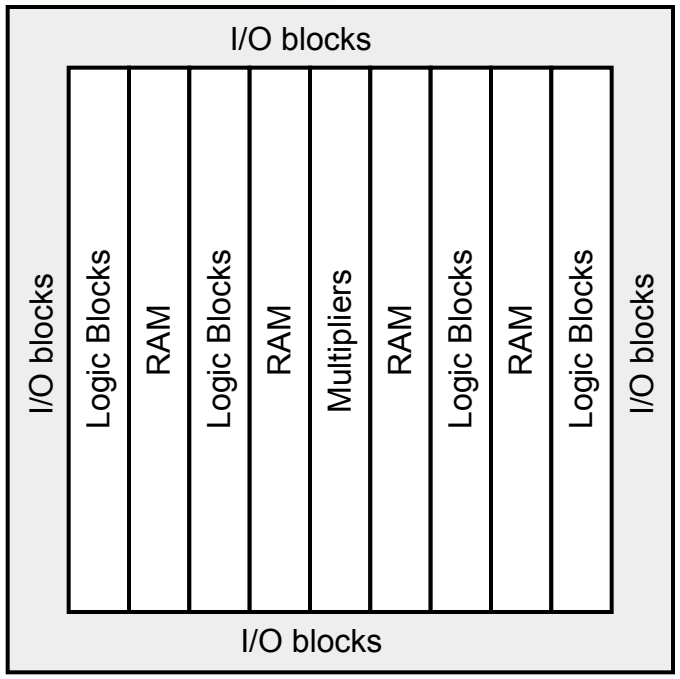
FPGA: interconections



- Programmable interconnections
  - Local:
    - Plenty and fast
    - Connect near cells
  - Global
    - Connect distant cells

General architecture

FPGA (Xilinx)



- Basic elements
  - Logic blocks
  - I/O blocks
  - Programmable interconnection matrixes
- Advanced elements
  - RAM memory
  - Clock managers
  - Multipliers

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