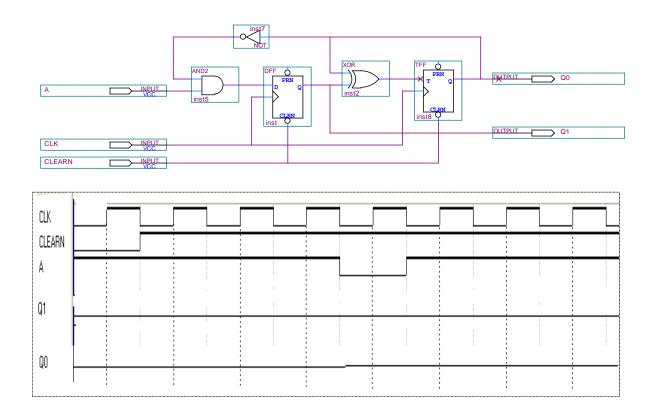
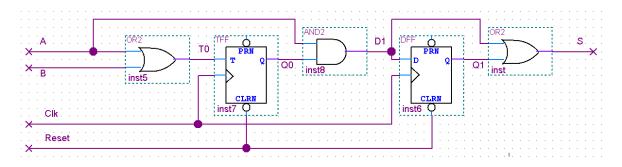


1. Complete the chronogram for the circuit given in the figure.



## 2. Given the following circuit:



- a) Obtain boolean expressions for the State and Output Functions. Consider that A and B are the circuit inputs, and S is the output.
- b) Is it a Moore's circuit, or is it Mealy's? Justify your answer.
- c) Complete the following chronogram, using intermediate variables if needed.

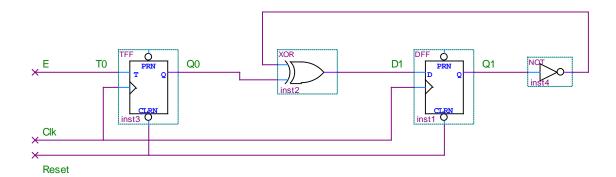


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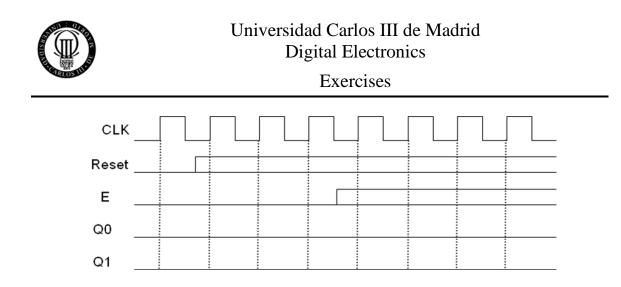
## Exercises

|     |       | 0 ps | 100.0 ns |  | 200.0 ns |  |  | 300.0 ns |  | 400.0 ns |
|-----|-------|------|----------|--|----------|--|--|----------|--|----------|
|     | Na    |      |          |  |          |  |  |          |  | 400.0 ns |
|     | Reset |      |          |  |          |  |  |          |  |          |
|     | Clk   |      |          |  |          |  |  |          |  |          |
| ∎>2 | A     |      |          |  |          |  |  |          |  |          |
| ∎>3 | В     |      |          |  |          |  |  | Ļ        |  |          |
| • 4 | QŨ    |      |          |  |          |  |  |          |  |          |
| 👁 5 | Q1    |      |          |  |          |  |  |          |  |          |
| 🗆 6 | S     |      |          |  |          |  |  |          |  |          |
|     |       |      |          |  |          |  |  |          |  |          |
|     |       |      |          |  |          |  |  |          |  |          |
|     |       |      |          |  |          |  |  |          |  |          |

- 3. Given the circuit shown in the figure:
  - a) Fill in the table below the figure
  - b) Draw its state diagram, including all the possible transitions
  - c) Complete the chronogram



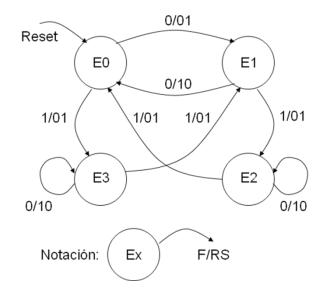
| Ε | <b>Q0</b> | Q1 | <b>T0</b> | <b>D1</b> | <b>Q0</b> <sup>+</sup> | Q1 <sup>+</sup> |
|---|-----------|----|-----------|-----------|------------------------|-----------------|
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |
|   |           |    |           |           |                        |                 |



4. Design the sequential circuit that corresponds to the state diagram shown in the figure, using D flip-flops and logic gates.

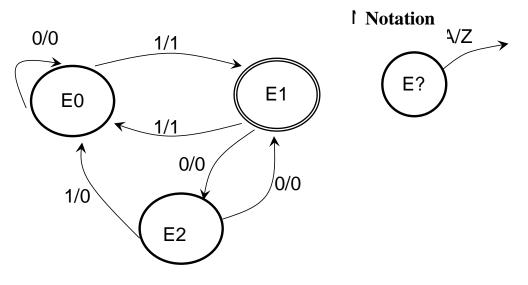
Use the following state encoding:  $\{E_0, E_1, E_2, E_3\} = \{00, 01, 10, 11\}$ . Find the Boolean equations for:

- a) Output functions
- d) State transition functions





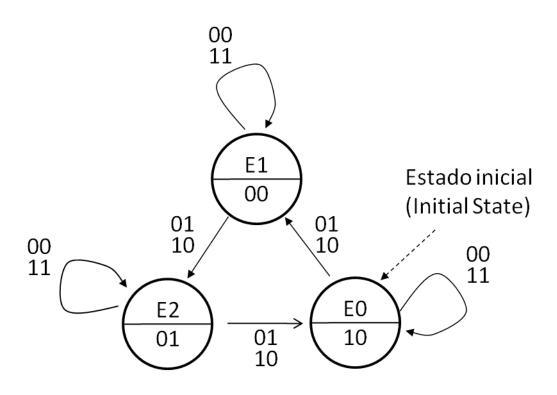
5. Given the following STG, implement the corresponding synchronous sequential circuit, using D flip-flops.



## Obtain:

- a) Inputs and Outputs of the FSM.
- b) States encodings. Justify your decision on the number of flip-flops.
- c) Transitions table.
- d) Simplified state and output functions.
- e) Scheme of the circuit with logic gates and flip-flops. Include in the scheme the clock and reset connections. Consider that E1 is the initial state.
- 6. The STG of the following figure represents the behaviour of a synchronous sequential circuit, which is requested to be implemented with D flip-flops.
  - a) Determine and justify if the diagram corresponds to a Moore's or Mealy's model.
  - b) Determine the minimum number of flip-flops that are needed for the implementation of the circuit.
  - c) Represent the state encoding table.
  - d) Determine the transitions that are not specified in the diagram.
  - e) Represent the transitions table.
  - f) Calculate the simplified state and output boolean functions.
  - g) Draw the circuit. It is not necessary to represent the combinational logic at the D inputs of the flip-flops (they can be left indicated as D0, D1, D2, etc.)





- 7. We want to design an engine controller that has two buttons M and P, to start and stop it, respectively:
  - M: start button
  - P: stop button

The controller generates an output S for starting (S=1) or stopping the engine (S=0), depending on the combination of the pressed buttons and the current state of the engine.

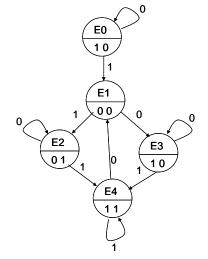
The functionality of the engine is defined by the following specifications:

- We suppose that initially the engine is stopped.
- If the engine is stopped and we push M (M=1), the engine will not start running until we release M (M=0).
- If the engine is running and we push P (P=1), the engine will not stop until we release P (P=0).
- We suppose that we can not push M and P at the same time.
- If we push M while the engine is running, it will not have any effect.
- If we push P while the engine is stopped, it will not have any effect.

Obtain the State Transition Graph of a **Moore's model** finite state machine for the functionality described before. The different states, inputs and outputs of the system must be clearly indicated. **Consider the solution with the least possible number of states.** 



- Exercises
- 8. Given the following State Transition Graph:



Answer the following questions, justifying your answers:

- a) Is it Moore's, or is it a Mealy's model?
- e) How many inputs, and how many outputs does it have?
- f) How many flip-flops are necessary to implement the circuit?
- g) Implement the circuit using T flip-flops and logic gates.
- 9. An aeronautics company wants to design an automatic pilot for an aircraft using a synchronous sequential circuit.

The automatic pilot needs to control the engines of the plane to maintain it at some altitude in a specified range, delimited by two values: maximum altitude and minimum altitude.

The plane has a height sensor which provides two bits  $(A_1, A_0)$  with the following meaning:

"10" means that the plane is above the maximum allowed altitude.

"01" means that the plane is below the minimum allowed altitude.

"00" means that the altitude is between both limits.

There is a signal RC ("Remote Control") to indicate if the aircraft is controlled by the ground station (if it is "0") or by the automatic pilot (if it is "1"). And there is another signal FL ("Fuel Level") to indicate if the fuel level is high ("1") or low ("0").

The automatic pilot controls the engines through two signals  $(M_1,M_0)$  with the following meaning:

"11" engines at maximum power, plane rises fast.

"10" engines at medium power, plane rises slowly.

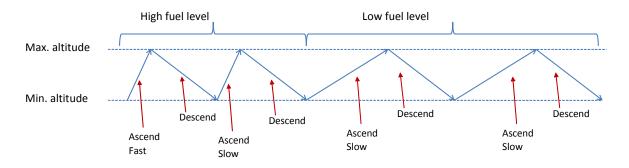
"01" engines at low power, plain descends.

"00" engines are controlled by ground station.

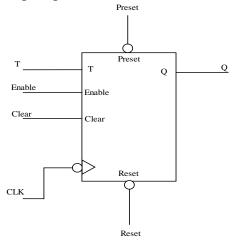
The automatic pilot has to take the following actions:



- If the ground station is controlling the aircraft, the engines signal should be "engines controlled by ground station", taking priority over any other received signals.
- If the maximum altitude is reached, the plane has to descend until it reaches the minimum altitude.
- If the minimum altitude is reached, the plane has to ascend.
- If the fuel level is low and the plane is ascending, the engines will work at medium power.
- If the fuel level is high and the plane is ascending, the engines will work at maximum power.
- a) Point out which signals are the inputs and outputs of the circuit.
- b) Find the STG of the circuit that implements the automatic pilot operation, pointing out if it is Moore's or Mealy's and justifying your answer.



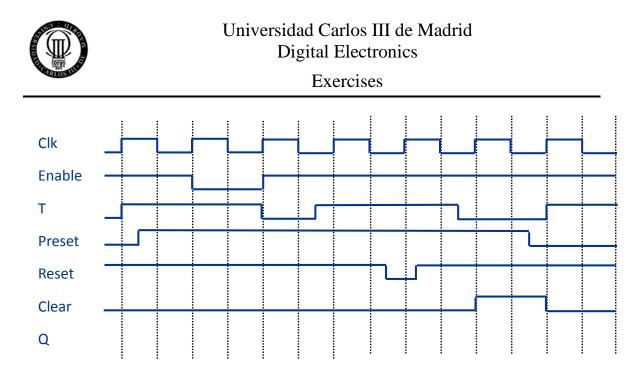
10. Given the following T flip-flop:



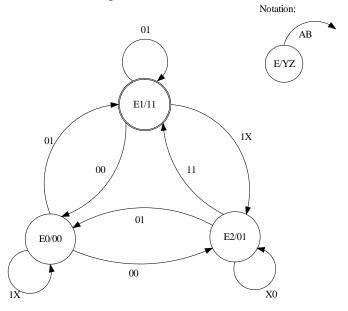
Notes:

- Clear is active-high and synchronous. It has priority over T and enable inputs.
- Preset and Reset are asynchronous and active-low.
- Enable is synchronous and active-high.
- The clock is falling-edge triggered.

Complete Q in the following chronogram:



11. Consider the following STG, where E1 is the reset state, A and B are the inputs of the circuit and Y, Z are the outputs.

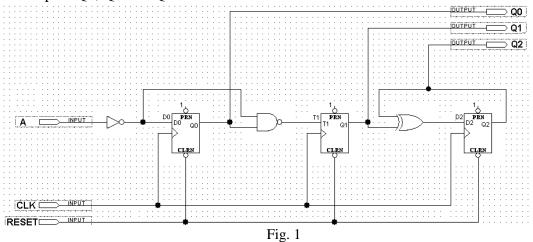


- a) Is this a Mealy or a Moore Design? Justify your answer.
- b) Which is the minimum necessary number of flip-flops for implementing this design?
- c) Obtain the Transition table. Choose the appropriate state encodings to get the least possible number of logic gates in the system outputs implementation.
- d) Draw the circuit scheme for this design using rising edge triggered D flip-flops with active-low preset and clear inputs. Use 4:16 decoders and additional logic gates for implementing the inputs of the D flip-flops. Implement the system outputs using logic gates.

Note: The decoder(s) inputs and outputs are active high.



12. Consider the synchronous circuit of the fig.1. This circuit has A as input and three outputs Q0, Q1 and Q2.



- a) Is it a Mealy or a Moore design? Justify your answer.
- b) Obtain the state functions (D0, T1 and T2):
- c) Fill in the following chronogram:

