ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS AT PHYSICAL LEVEL

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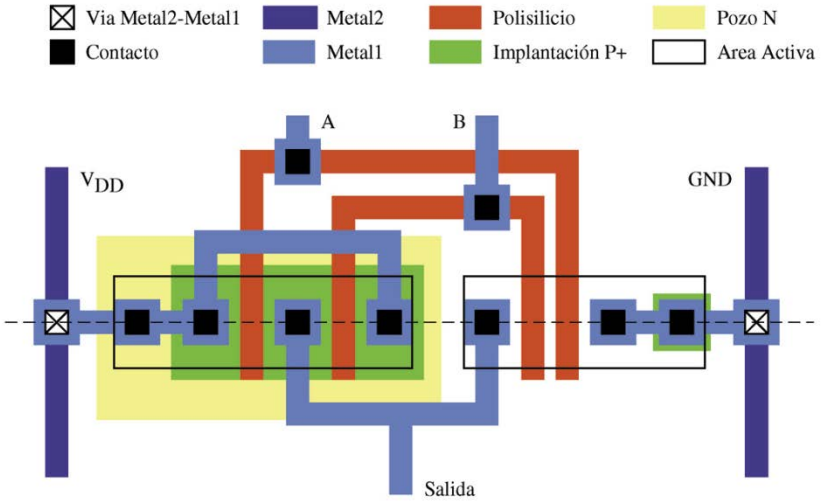
Outline

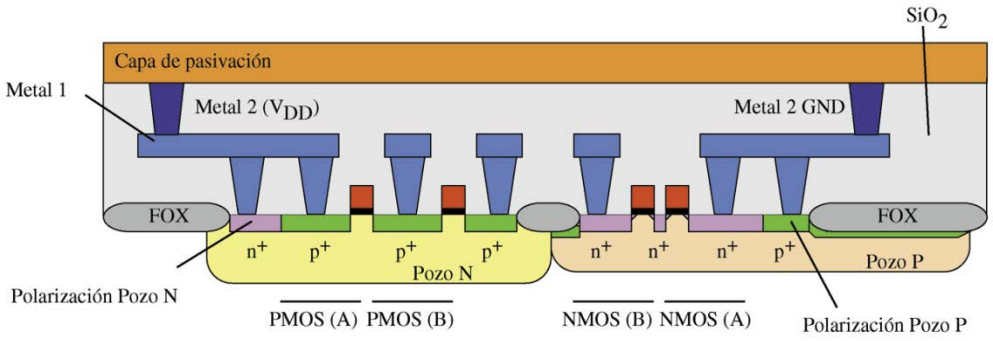
- Required masks for CMOS integrated circuits manufacturing.
  - Layout for a NAND gate
  - Layout for an inverter
- Design rules
- Examples

Required masks for CMOS integrated circuits manufacturing

- Masks are used in order to select the areas in silicon where the different fabrication steps must be applied.
- The graphical representation of required masks that define a circuit to be fabricated is named *layout*.
- A layout consists of a set of rectangles that represent the different layer masks:
  - Substrates and wells
  - Diffusion areas
  - Polysilicon
  - Metal interconnections
  - Contacts and via

Required masks for CMOS integrated circuits manufacturing

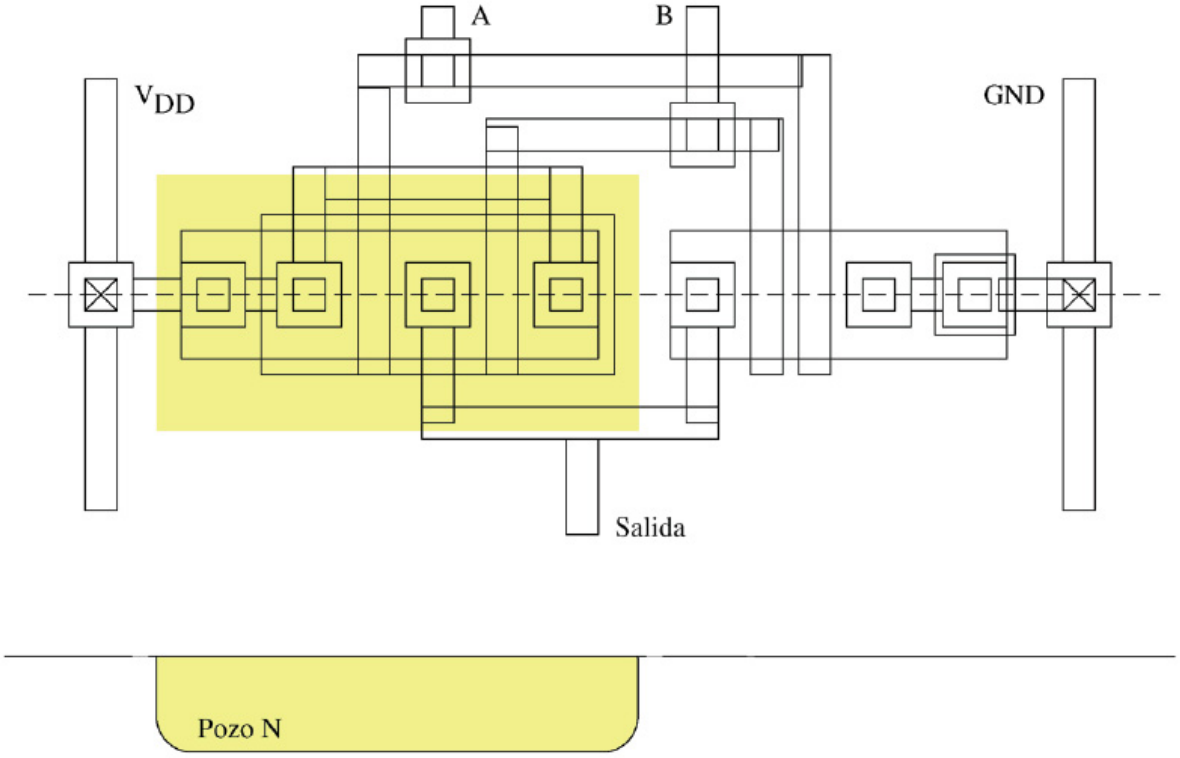




A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing

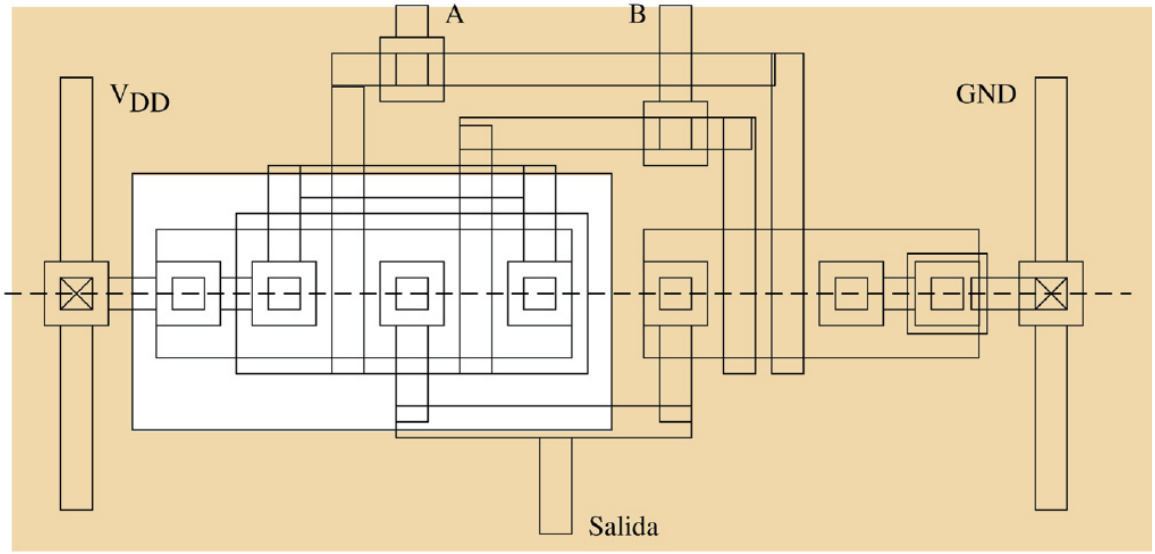
- N-well implantation

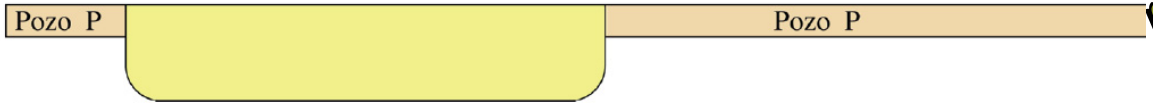


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- P-well implantation

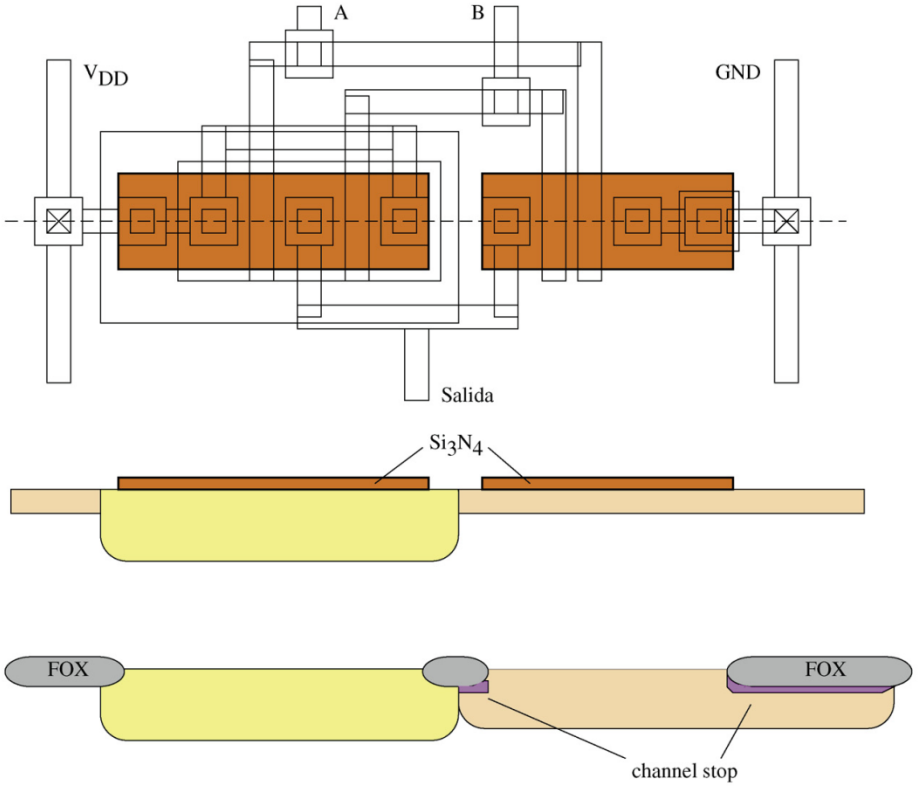




A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

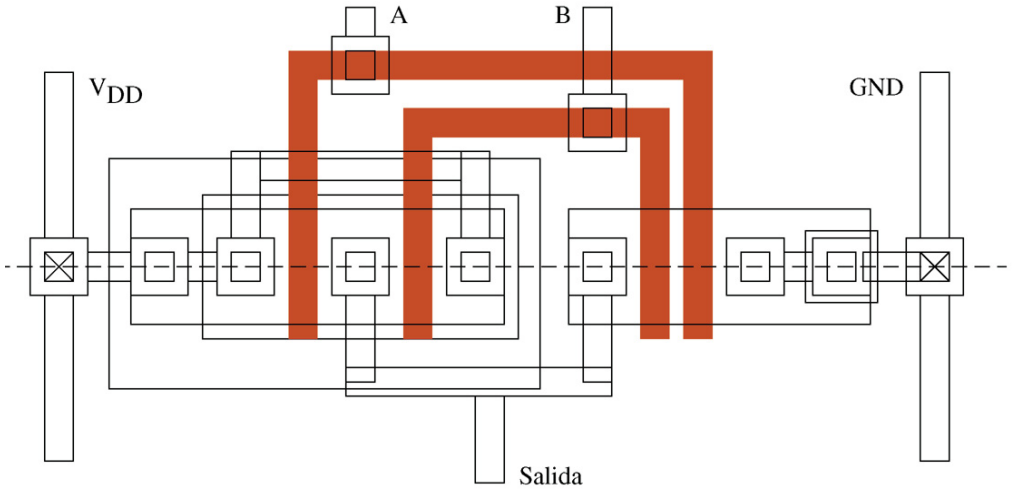
- Active areas mask and thick oxide aimed at isolating transistors

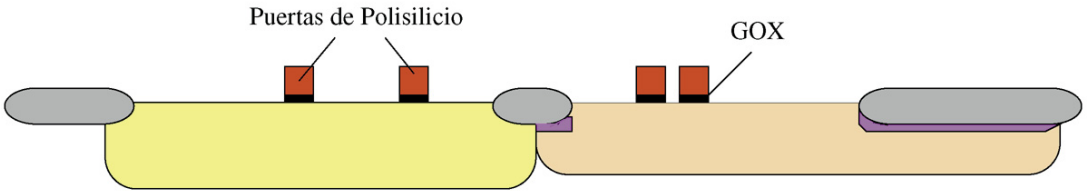


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Polysilicon for transistor gates

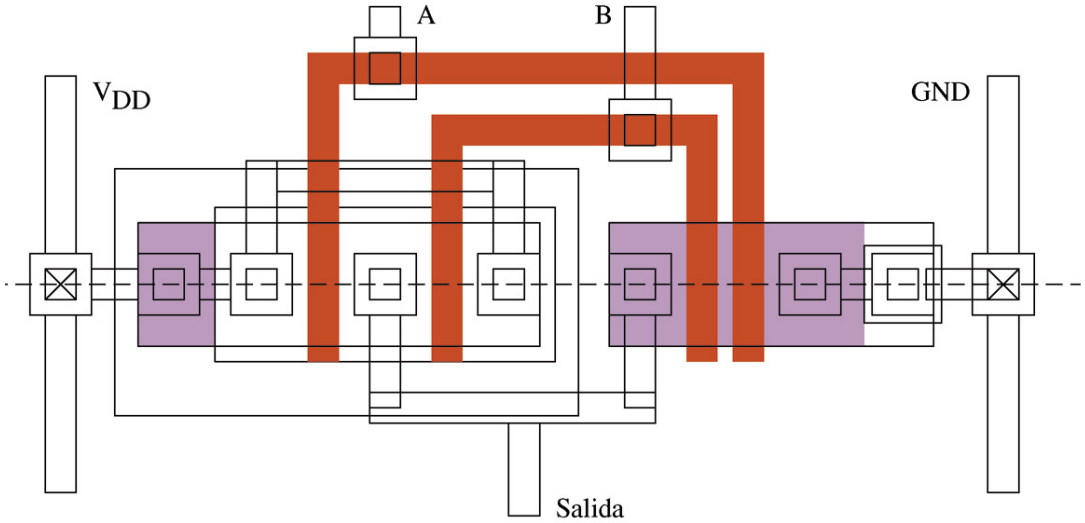


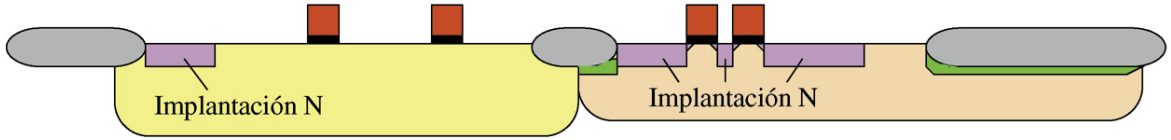


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- N+ dopants implatation





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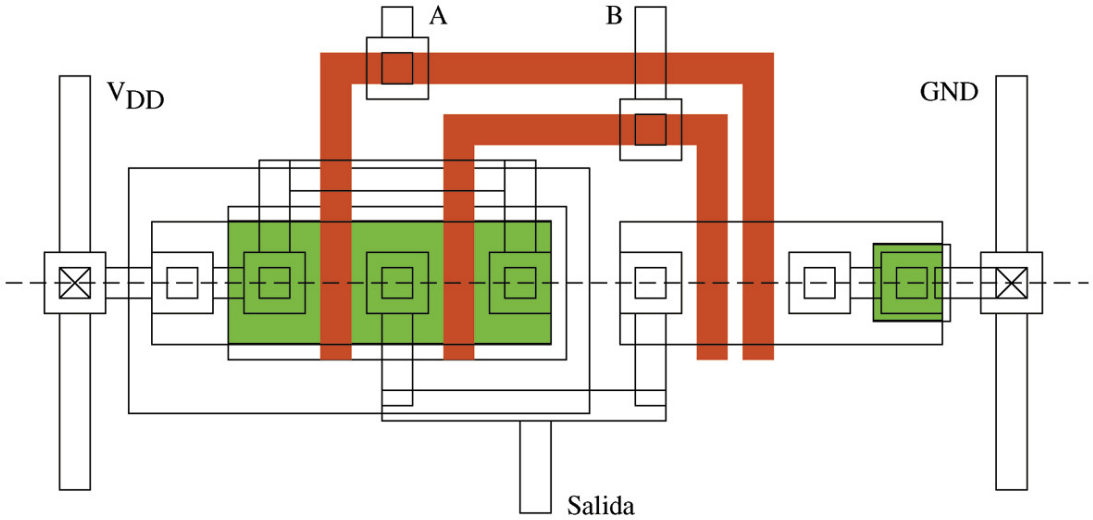
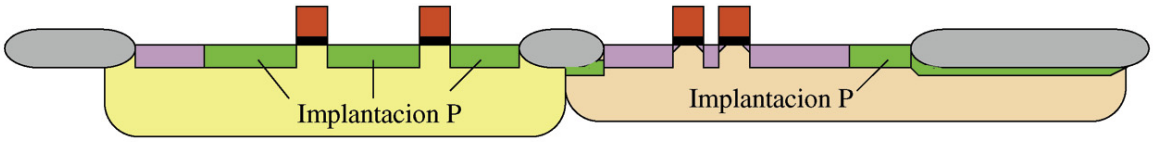
Required masks for CMOS integrated circuits manufacturing : NAND gate

- P+ dopants implantation

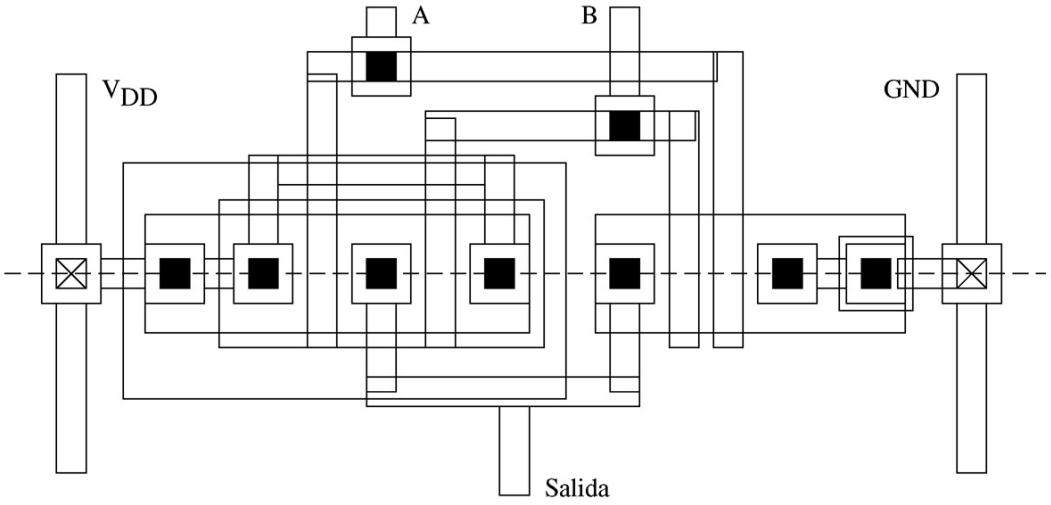




A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

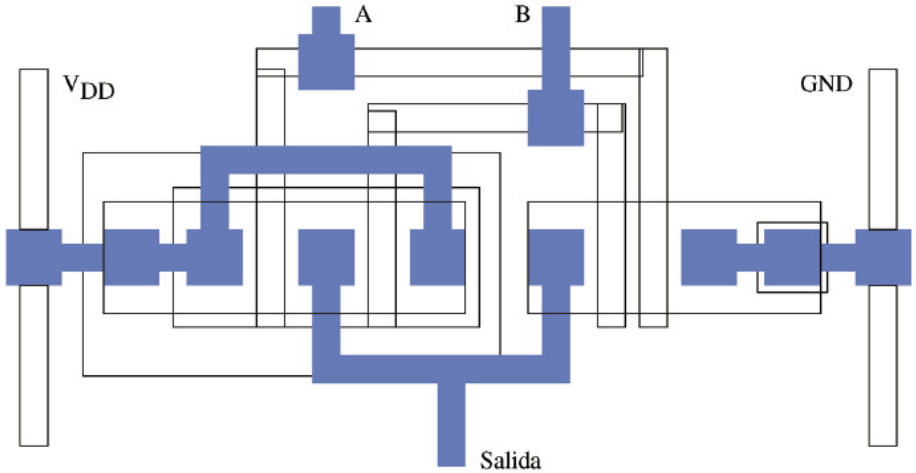
- Adding insulator just keeping free the necessary areas to implement connections



A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

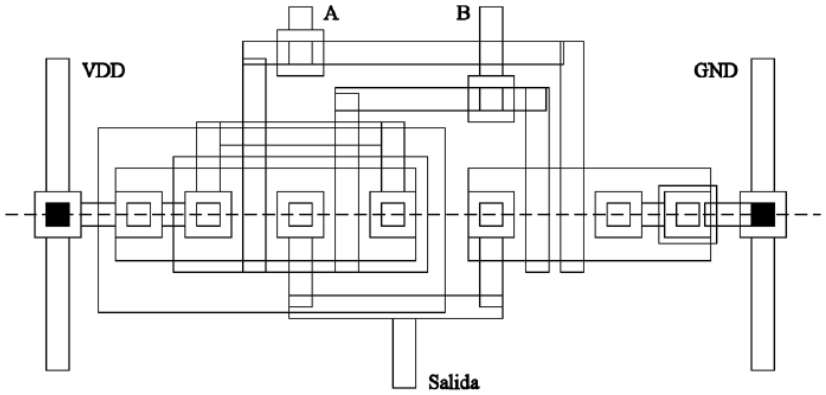
- Metalization: first layer

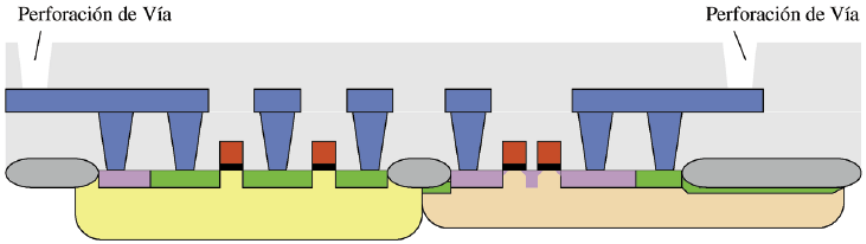


A. Rubio et al., "Diseño de circuitos y sistemas integrados" Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Adding insulator just keeping free the necessary areas to implement connections between two metal layers (via)

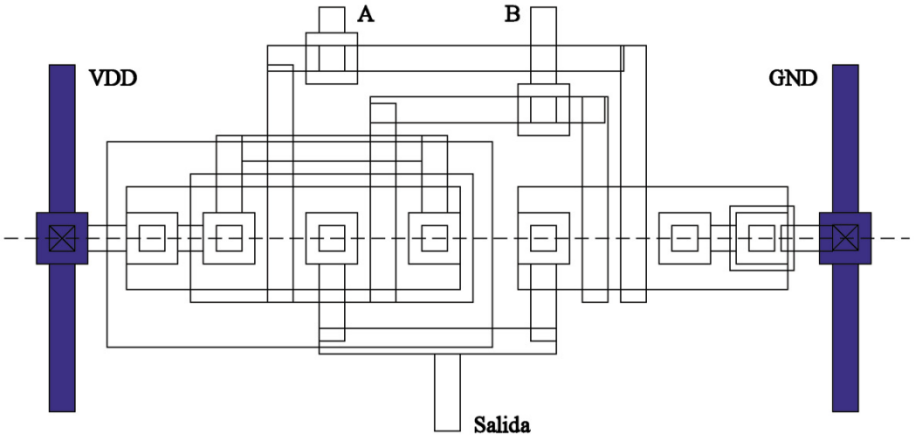


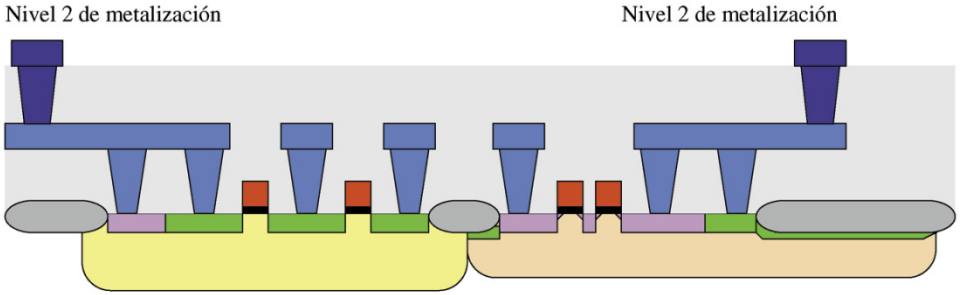


A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : NAND gate

- Metalization: second layer

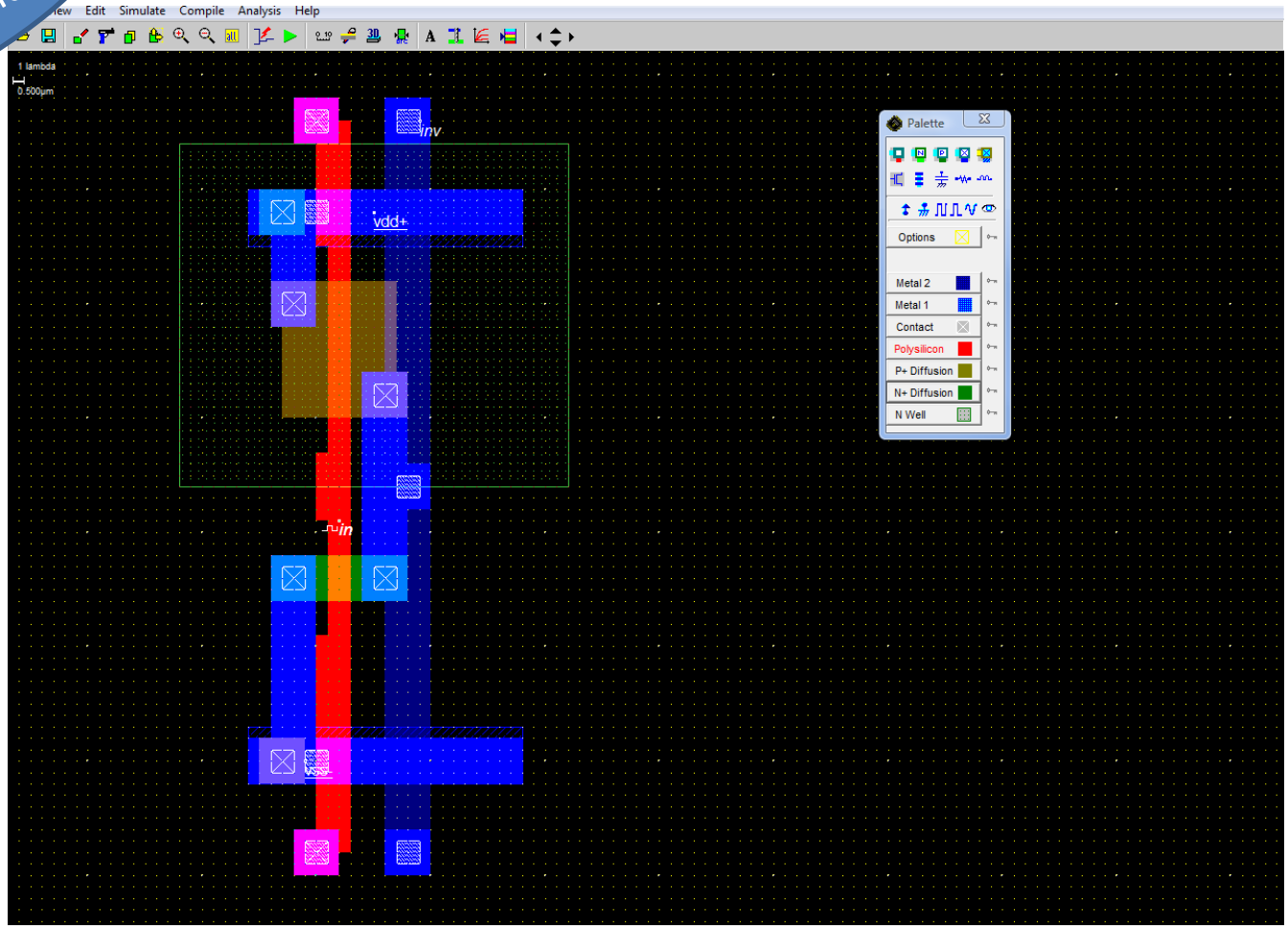




A. Rubio et al., “Diseño de circuitos y sistemas integrados” Ediciones UPC, 2003.

Required masks for CMOS integrated circuits manufacturing : inverter gate

Microwind



Design rules

- They are the necessary set of rules that allows the designer to specify the design for its implementation on the silicon wafer.

- A complete set of design rules consists of the following elements:
  - Set of layers
  - Relations between the rectangles in the same layer
  - Relations between the rectangles in different layers

- They fix geometric restrictions

Design rules

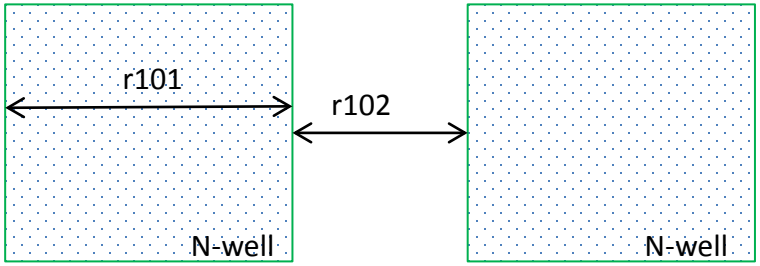
- There are two types:
  - Scalable.- They are represented in base to a parameter (λ)
    - Adimensional rules.
    - 2λ is the minimum size. It depends on the minimum dimension that is possible to etch in the silicion by means of the litographic process.
    - During this course, scalable design rules are used. (Microwind CAD tool)
    - In case of technologies beyond 0.18µm (lower dimensions), the scalability is not linear.
    - These design rules imply the worst case => over-dimensioned circuits
  - Non scalable
    - They are used by the industry

Design rules

Microwind

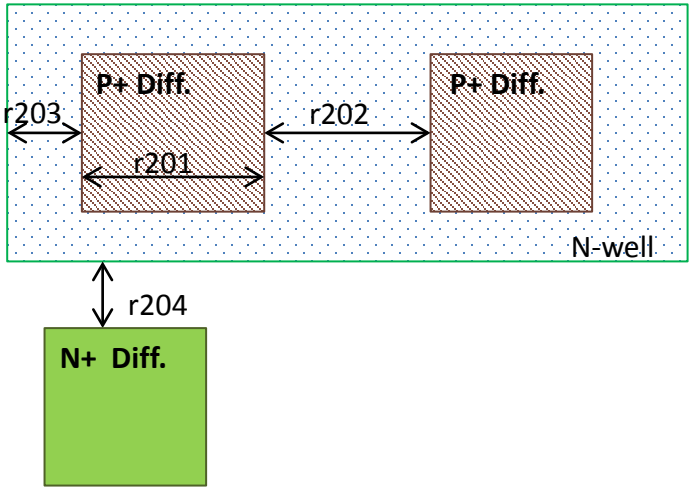
- file.rul

N-well



r101 → Minimum well size
r102 → Minimum distance between wells

Diffusion areas



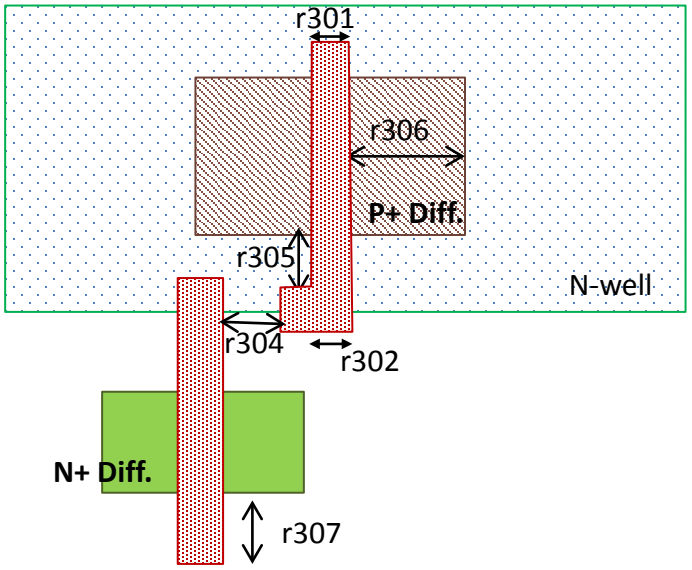
r201 → Minimum P diffusion size
r202 → Minimum distance between P diffusions
r203 → Extra well after diffusion
r204 → Minimum distance between diffusion and well

Design rules

Microwind

- file.rul

Polysilicon



r301 → Minimum polysilicon width
r302 → Minimum polysilicon gate on diffusion N+
r304 → Minimum distance between two polysilicon

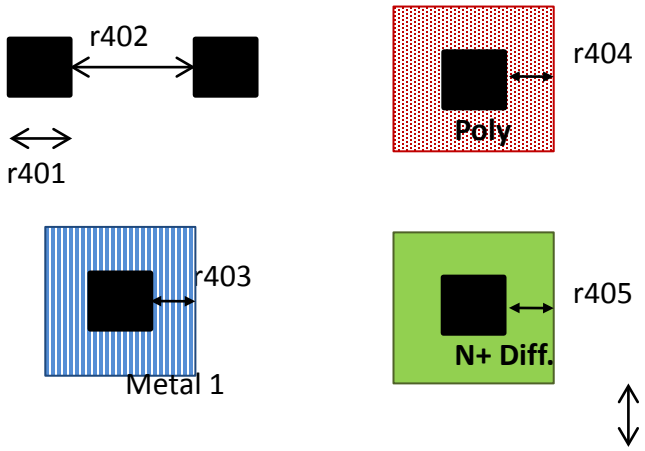
r305 → Minimum distance between polysilicon and other diffusion
r306 → Diffusion after polysilicon
r307 → Extension of polysilicon after diffusion

Design rules

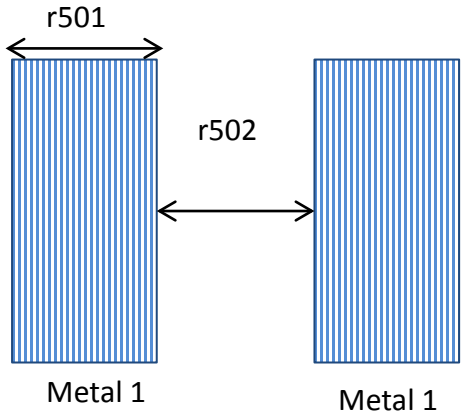
Microwind

- file.rul

Contacts



Metal 1



r401 → Minimum contact widht
r402 → Minimum distance between two contacts
r403 → Extra metal over contact
r404 → Extra polysilicon over contact
r405 → Extra diffusion over contact

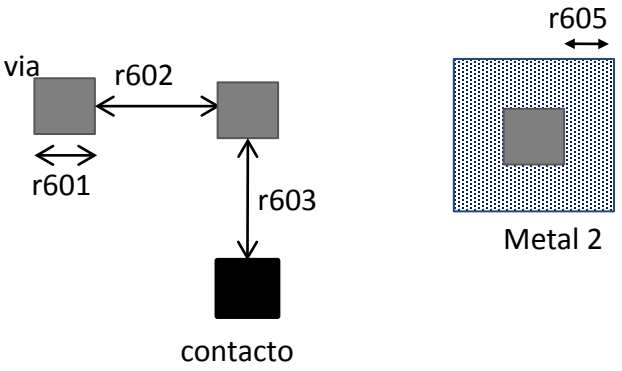
r501 → Minimum metal width
r502 → Minimum distance between metals

Design rules

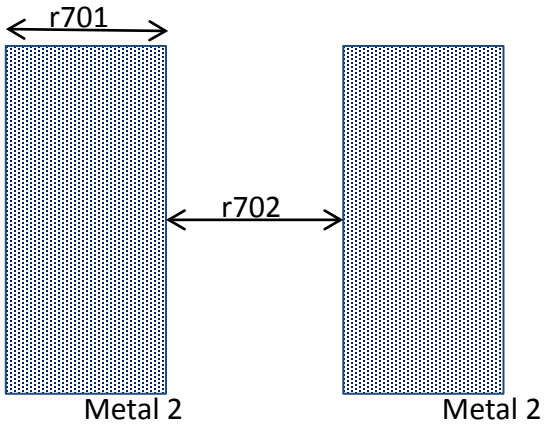
Microwind

- file.rul

Via



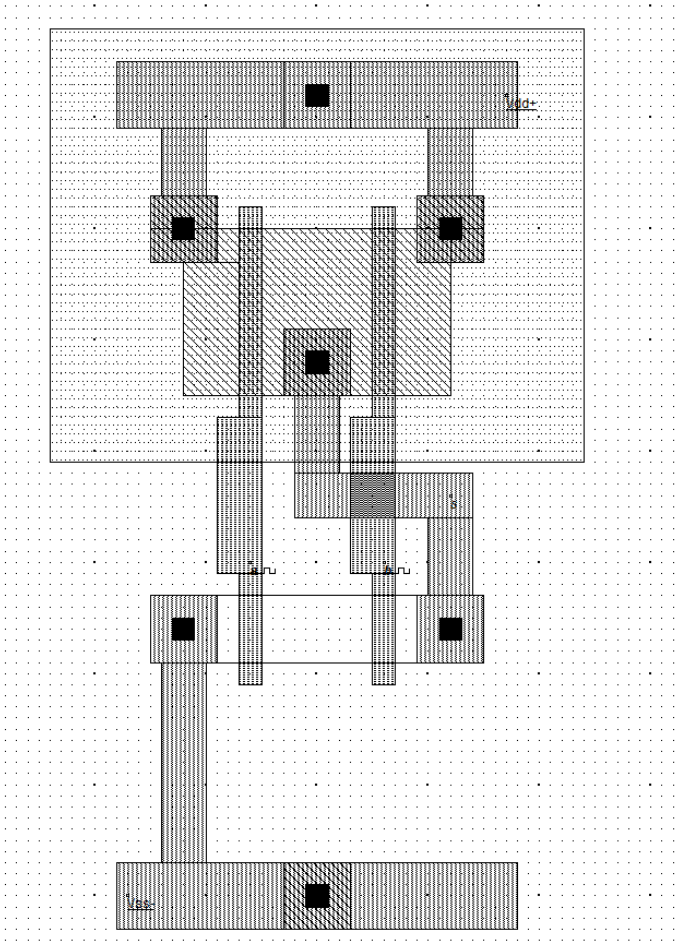
Metal 2

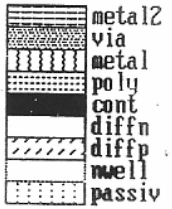


r601 → Minimum via width
r602 → Minimum distance between two via
r603 → Minimum distance between via and contact
r604 → Extra metal 1 over via
r605 → Extra metal 2 over via

r701 → Minimum metal 2 width
r702 → Minimum distance between two metal 2

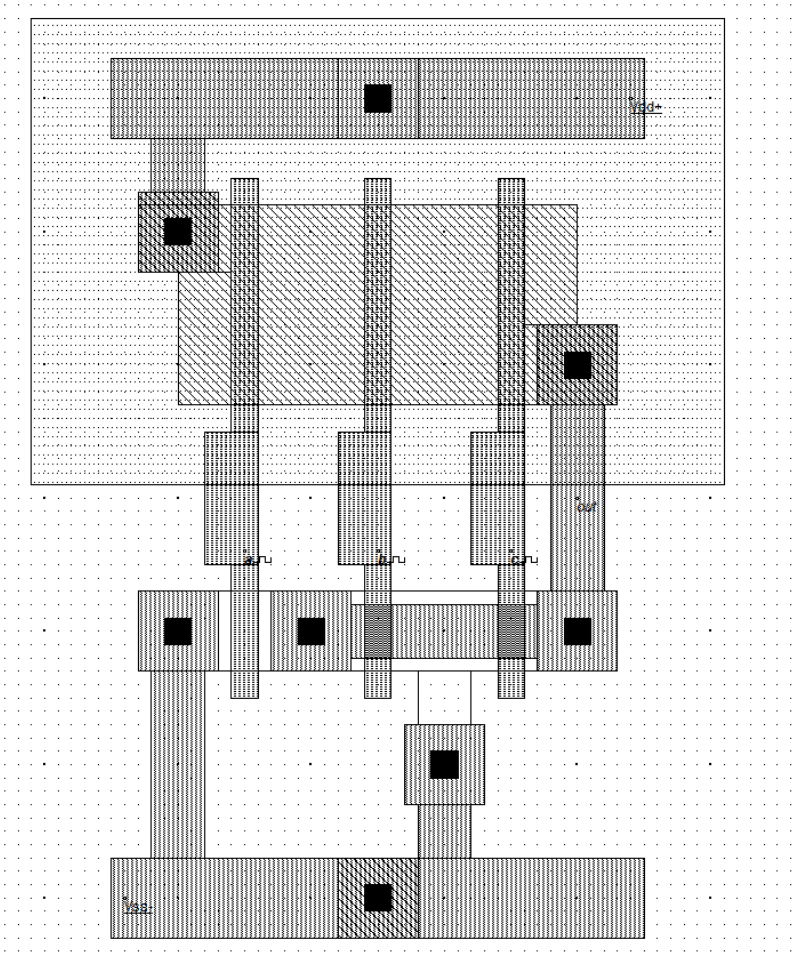
Examples





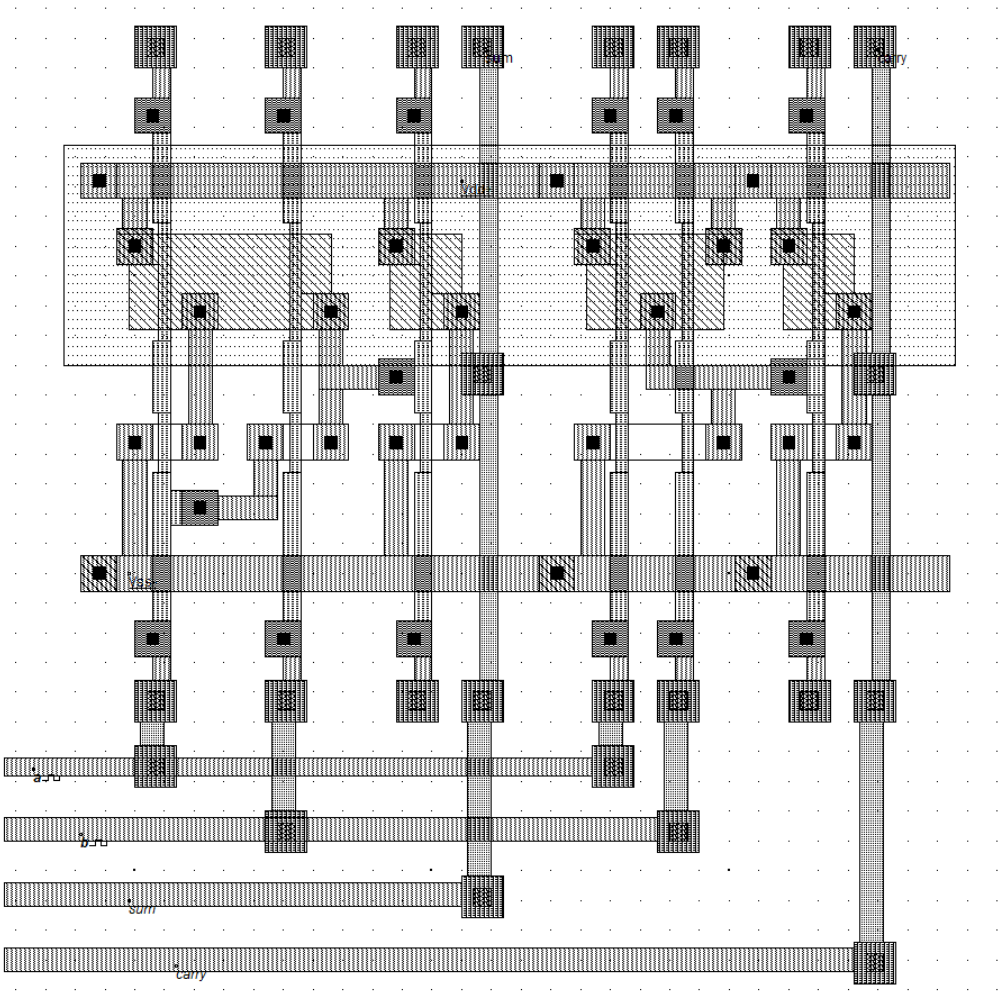
2-inputs NAND

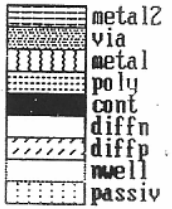
Examples



3-inputs NOR

Examples


vdd
vss
a
b
sum
carry


metal2
via
metal
poly
cont
diffn
diffp
nwell
passiv