INTRODUCTION TO INTEGRATED CIRCUITS

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Outline

- **1.1 Integrated Circuits. Advantages and disadvantages over non integrated circuits.**
  - **Digital Circuits Implementation**
  - **Advantages of ICs**
  - **Moore's Law**
- **1.2 Design process of an integrated circuit. Abstraction Levels.**
  - **Bottom-up and bottom-down methodologies.**
  - **Design process: steps and tools.**
  - **Abstraction levels: Gajski-Kuhn Y-chart**

Integrated Circuits implementation (I)

- **Discrete components (standard)**
  - **74xx, 54xx**
- **Integrated Circuits**
  - **ASIC: Application Specific Integrated circuit**
- **Programmable circuits**
  - **PLD, SPLD: (Simple) Programmable Logic Devices**
  - **CPLD: Complex Programmable Logic Devices**
  - **FPGA: Field Programmable Gate Array**
- **Microprocessors**

Integrated Circuits implementation (II)

- **Microprocessor systems**
  - **Microprocessor and additional components (standard components)**
  - **SoC: System on Chip (ASIC)**
  - **SoPC: System on Programmable Chip (FPGA)**

Advantages of Integrated Circuits

- **Size: small**
- **Speed: very high**
  - **Board: f < 100 MHz**
  - **FPGA: 500 MHz**
  - **ASIC: f < 3 GHz**
- **Cost: depends on the number of manufactured units**
  - **Initial cost: design and prototyping (100.000€)**
  - **Cost per unit: 1-200€**
  - **Worthwhile for large numbers of production units (>10.000 units/year)**
- **Reliability: high; better noise inmunity**
- **Power consumption: low**

Moore's Law (Intel co-founder)

- **The maximum number of transistors that can be integrated in a I.C. will double about every 2 years (20 months)**

CPU Transistor Counts 1971-2008 & Moore's Law

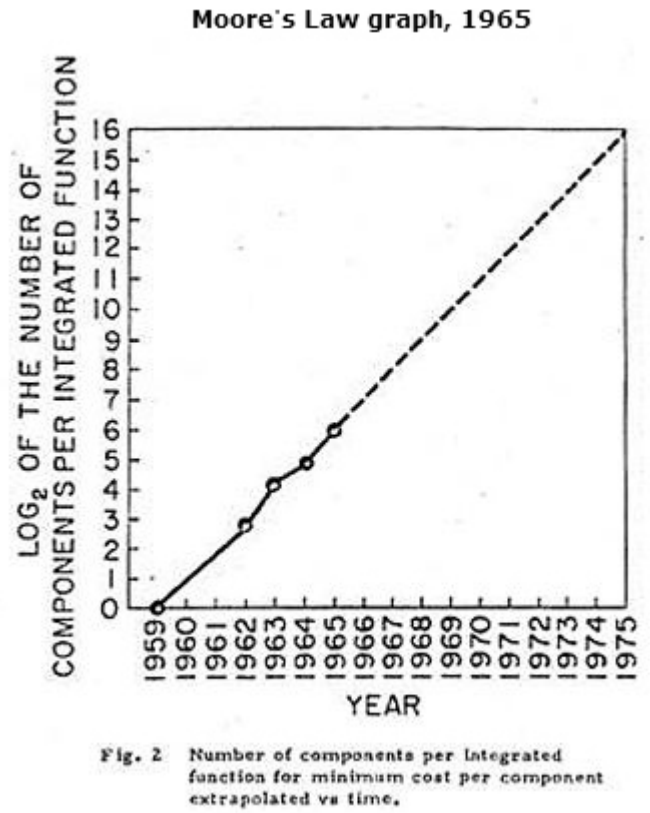
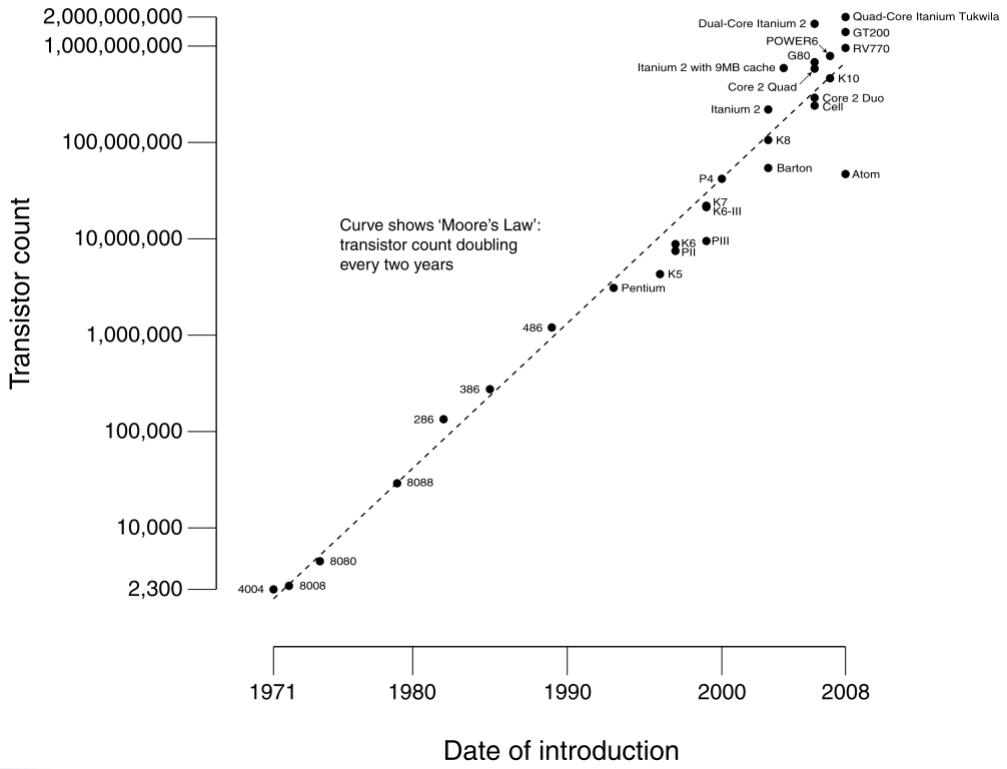


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.



Abstraction Levels

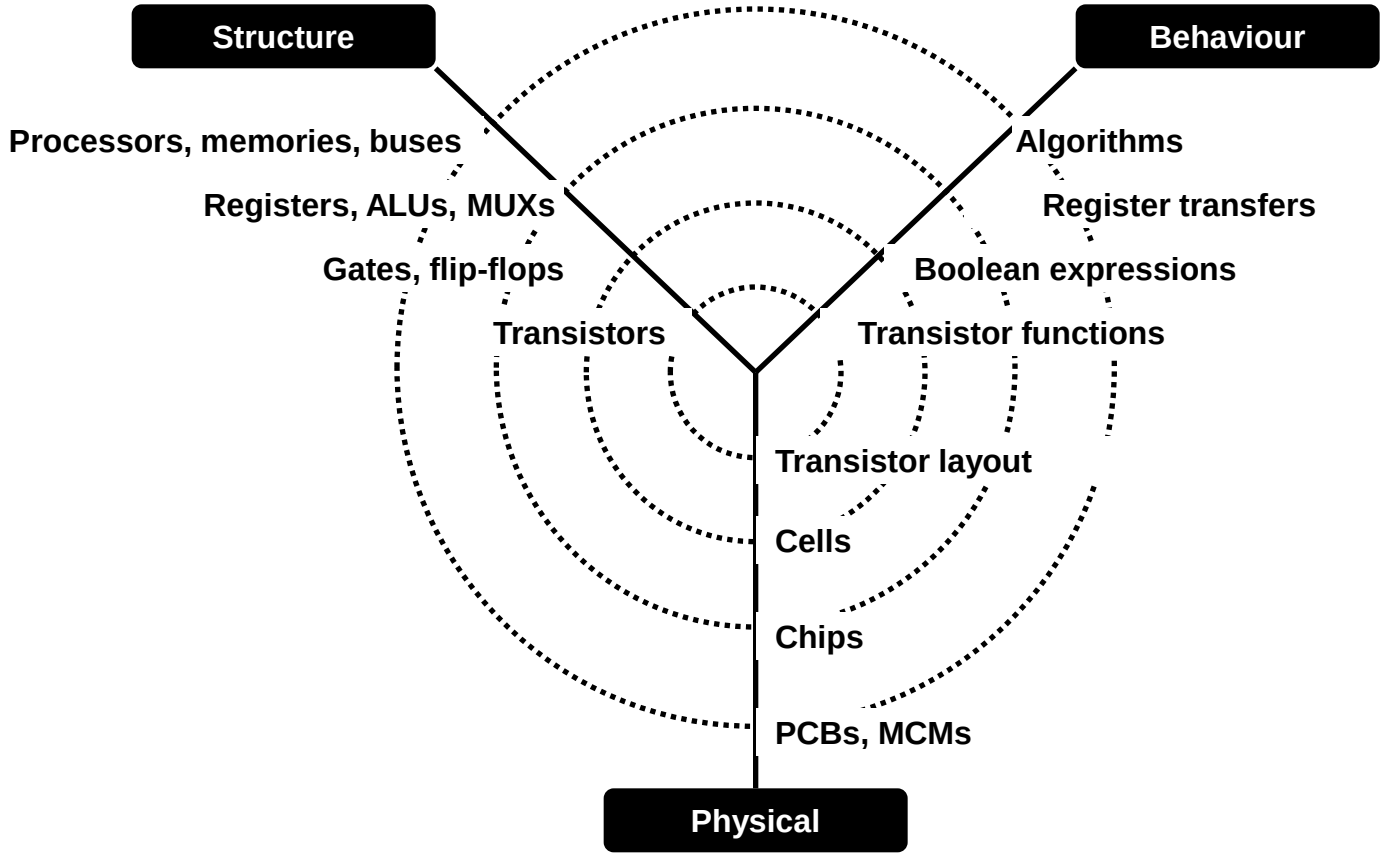
☞Levels:

- ❑System
- ❑Algorithm
- ❑Register Transfer Level (RTL)
- ❑Logic (gates)
- ❑Physical (transistors)

☞Domains:

- ❑Behavioral
- ❑Structural
- ❑Physical

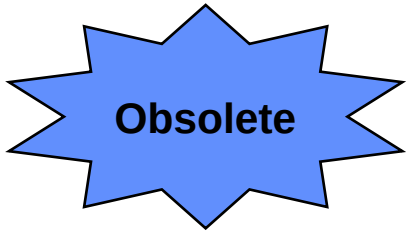
Abstraction Levels: Gajski-Kuhn Y-chart



Design Process

☞ Bottom-up Methodology

- ❑ Specification
- ❑ Block partition
- ❑ Logic gates design (schematic)
- ❑ Block assembly
- ❑ Physical design



☞ Top-down Methodology

- ❑ Specification
- ❑ Architectural design
- ❑ Detailed design
- ❑ Physical design

- ❑ Use of Hardware Description Languages (HDL)
- ❑ Intensive use of simulation and automatic synthesis

Design process of integrated circuits

- **Functional specification**
  - System description, chronograms
- **Architectural design**
  - RT design (registers, buses, state machines...)
- **Detailed design**
  - Automatic Synthesis
  - Logic Design (gates, flip-flops, ...)
- **Physical design**
  - Transistors, place & route
- **Manufacturing and test, or programming**
- **Operation**

Automatic Tools

Design tools

- **Simulation**
  - Functional description
  - RTL description (synthesizable)
  - List of gates
  - with delays
- **Synthesis**
  - Transform RTL descriptions into logic gates
  - Optimize logic for area and/or speed
  - Provides with logic delays
- **Place & Route**
  - Places and interconnects logic gates
  - Extracts delays for interconnections

Hardware Description Languages Usefulness

- **HDLs allow to:**
  - **Design in a higher abstraction level**
  - **Simulate designs for operation validation**
    - ✓ **Simulation is more efficient when performed at a higher abstraction level**
  - **Sinthesize designs to obtain an optimal implementation, depending on the target:**
    - ✓ **Area**
    - ✓ **Speed**
- **Essential for modern designs with:**
  - **Very large scale integration (>10K gates)**
  - **Design on ASIC or CPLD/FPGA**