CMOS INTEGRATED CIRCUITS FABRICATION PROCESSES

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Outline

- Fundamental processes
  - Wafer manufacture
  - Thermal oxidation
  - Doping processes
    - Ion implantation
    - Solid-state diffusion
  - Photolithography
  - Thin-film removal
  - Thin-film deposition
- CMOS process sequence (process flow)

Fundamental processes: Wafer manufacture

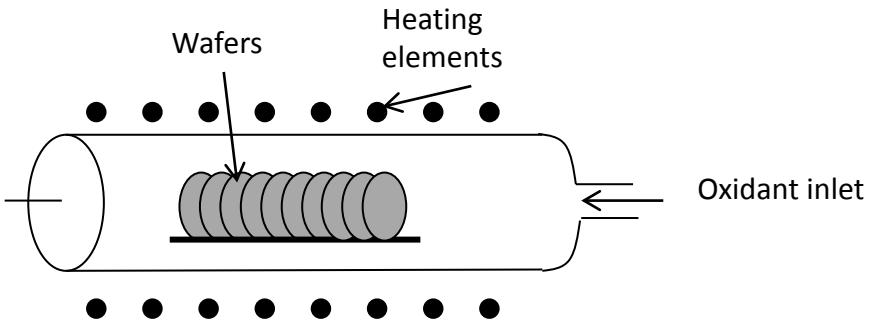
- **Wafer production requires three processes:**
  - **Silicon refinement**: Several processes are necessary in order to obtain polycrystalline chunks of silicon with the enough purity.
    - Silica in a furnace at 2000ºC with carbon source

      $SiO_2(solid)+2C(solid) \rightarrow Si(liquid)+2CO(gas)$
    - Chemical reduction processes
  - **Crystal growth**: Czochralski method
  - **Wafer formation:** 1 mm thick (thickness increases with wafer diameter)

http://www.youtube.com/watch?v=aWVywhzuHnQ

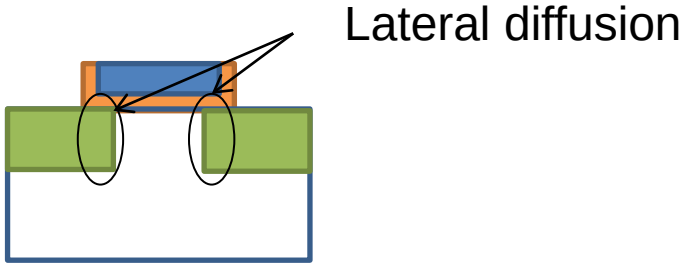
Fundamental processes: Thermal oxidation

- Silicon within an oxidant at elevated temperatures will form a thin layer of oxide (SiO_2) on all exposed surfaces.
- SiO_2 is an essential element in CMOS technology:
  - High quality dielectric such as gate oxides
  - Used for implantation, diffusion and etch masks
  - Near ideal silicon-oxide interface
- The silicon wafer is exposed at high temperatures (900-1200ºC) to a gaseous oxidant:
  - O_2: dry oxidation
  - water vapor: wet oxidation



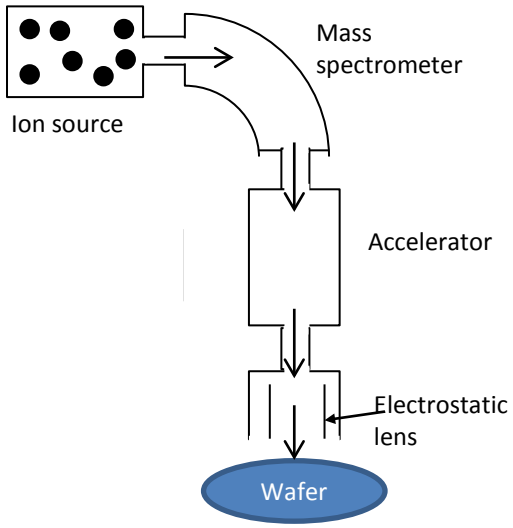
Fundamental processes: Doping processes

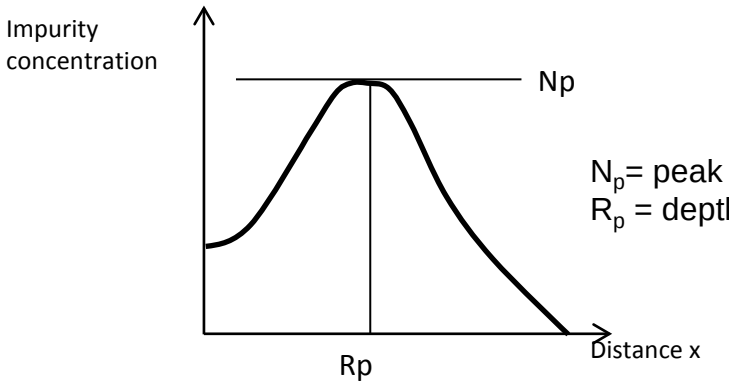
- Controlled introduction of dopant impurities into silicon
  - N-type dopants: P, As, Sb
  - P-type dopant is B
- Solid state diffusion has been the traditional doping process. Diffusion is directly proportional to the concentration gradient and thermal energy



Doping process: Ion implantation

- Ion implantation is the most used method in modern CMOS fabrication
- Dopant atoms are ionized, then accelerated through a large electric potential (few kilovolts to megavolts) toward a wafer. The highly energetic ions bombard and implant into its surface.



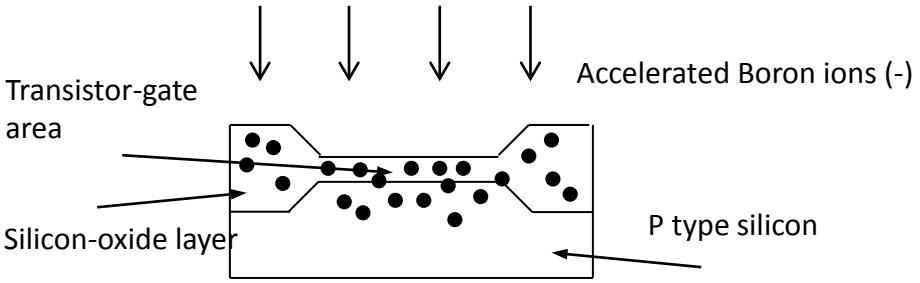


N_p= peak concentration
R_p = depth of the implant

Implant doping profile is given by a Gaussian distribution

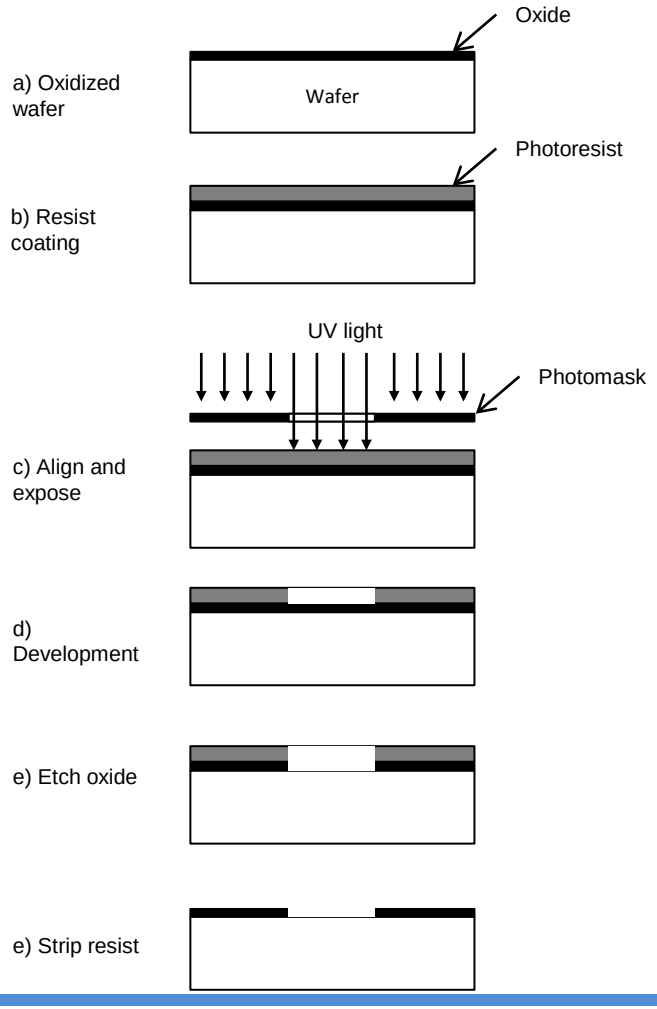
Doping process: Ion implantation

- High degree of lattice damage. It is repaired with annealing at high temperatures agitating dopant impurities into lattice sites.
- Compared with solid-state diffusion, ion implantation has the advantages of being a low-temperature and a highly controlled process.
- Nowadays, diffusion is used to redistributing dopants after the ion implantation



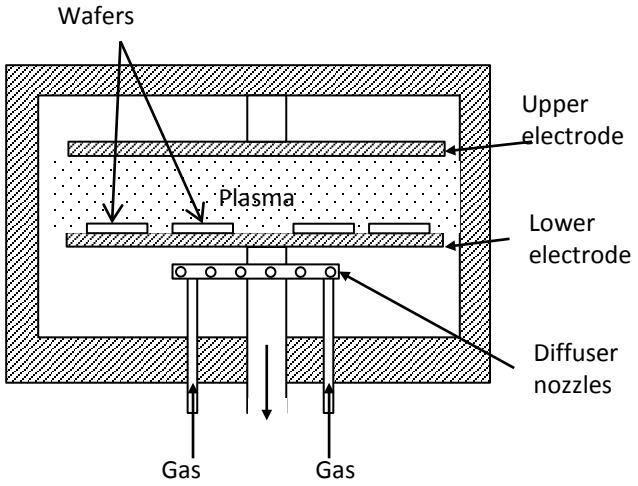
Fundamental processes: Photolithography

- Process used to select the parts in a wafer that must be affected by a given fabrication process
- A light-sensitive polymer called photoresist serve as ion implantation masks and etch masks
- Photoresist can be negative (insoluble (hardened) after exposure to UV) or positive (soluble after exposure to UV light). Positive photoresists present a higher resolution
- Resolution: diffraction of light limits the minimum printable feature size
  - Electron beam



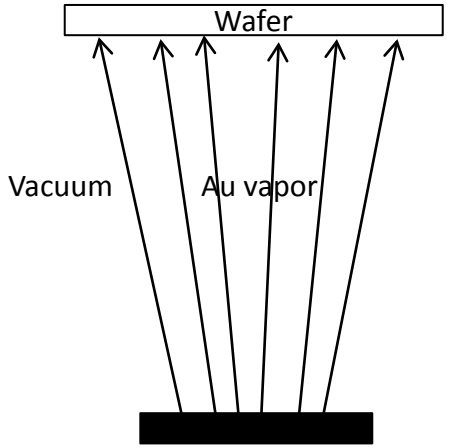
Fundamental processes: Thin-film removal

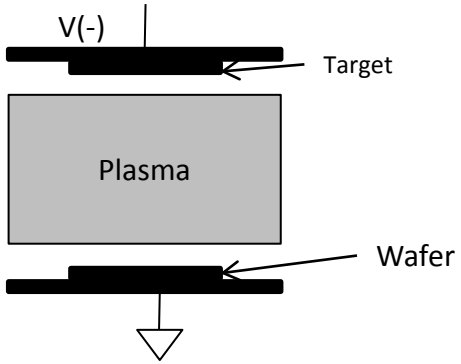
- Processes to remove thin films
  - Wet etching. A chemical solution is used to remove material. Highly selective compared with the dry-etch processes
  - Dry etching.
    - The wafer is bombarded by charged ions that cause material to be ejected off the surface



Fundamental processes: Thin-film deposition

- Methods of depositing thin films of insulators, conductors and semiconductors on the wafer
  - Film thickness uniformity <±5nm
- Physical vapor deposition (PVD). Atoms or molecules pass through a low-pressure gas phase and then condense on the surface of the substrate:
  - Evaporation
  - Sputter deposition (similar to dry etching)





Fundamental processes: Thin-film deposition

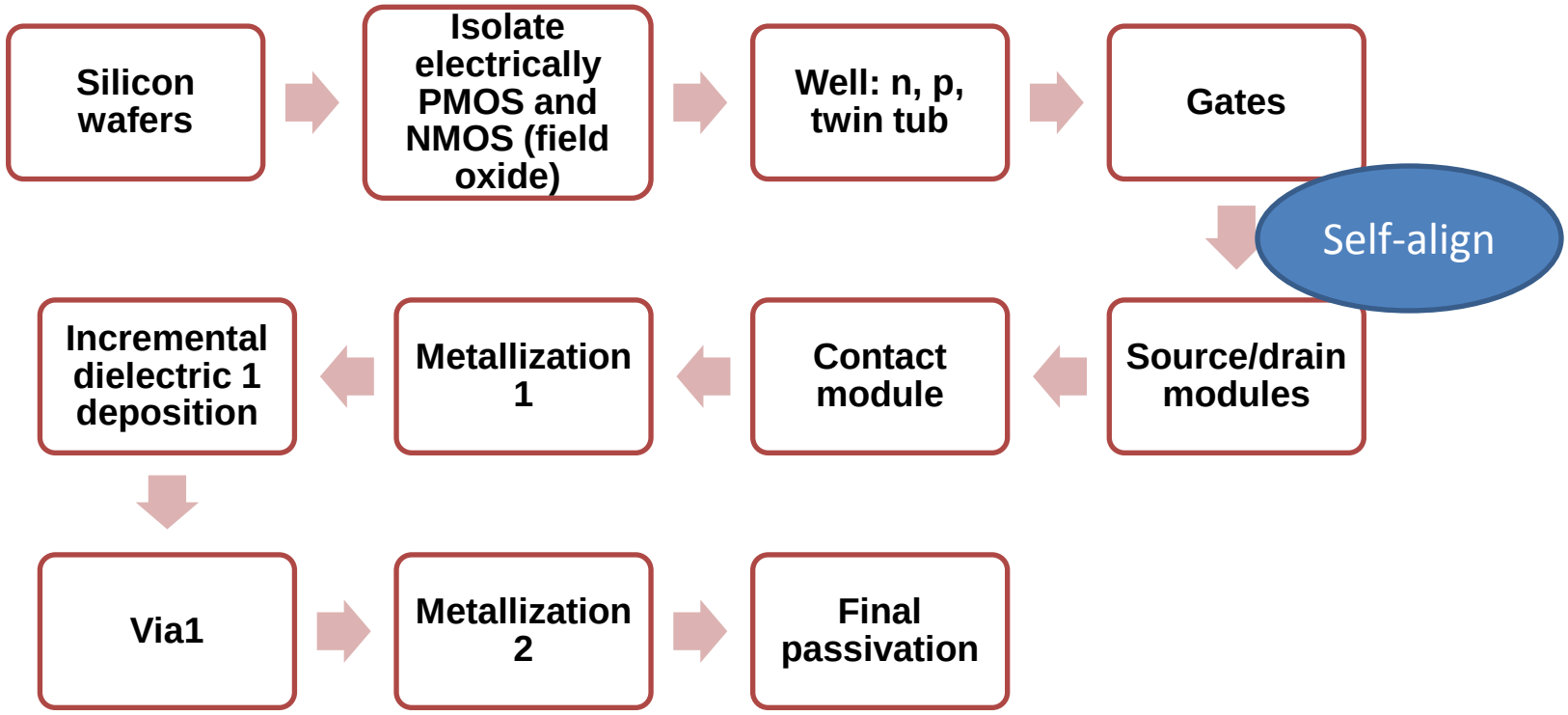
- Chemical vapor deposition (CVD). Reactant gases are introduced into a chamber where chemical reactions between the gases at the surface of the substrate produce the desired film.
- At atmospheric pressure at relatively low temperatures CVD can be applied in a reactor similar to an oxidation tube furnace
- At low pressure the process can yield better films but at the expense of a higher deposition temperature.

Polisilicon→ Thin-film deposition of silicon on SiO_2

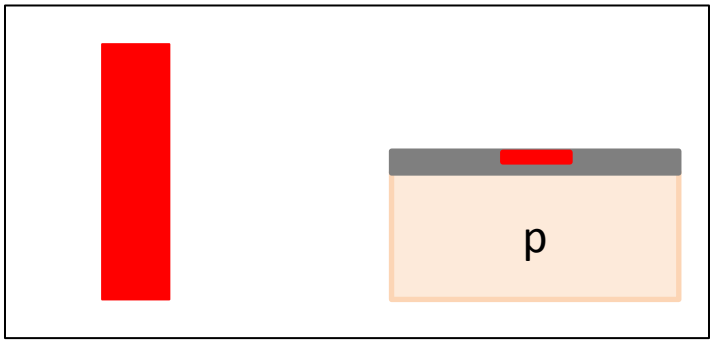
Metallization→ AlCu/Ti

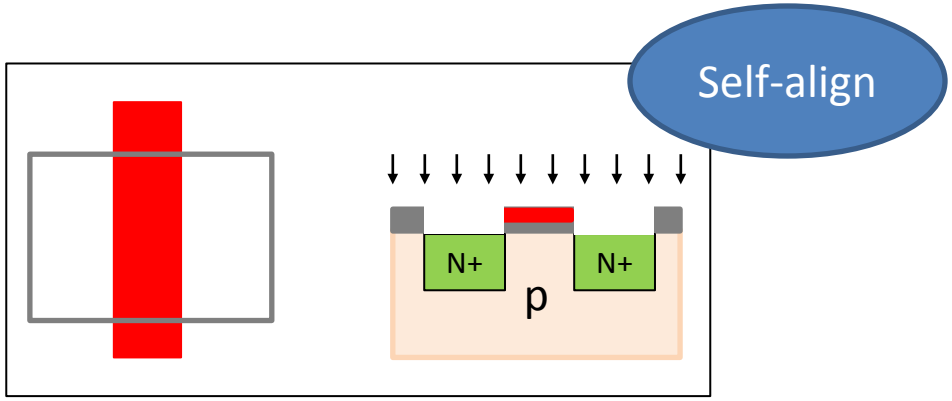
CMOS process sequence

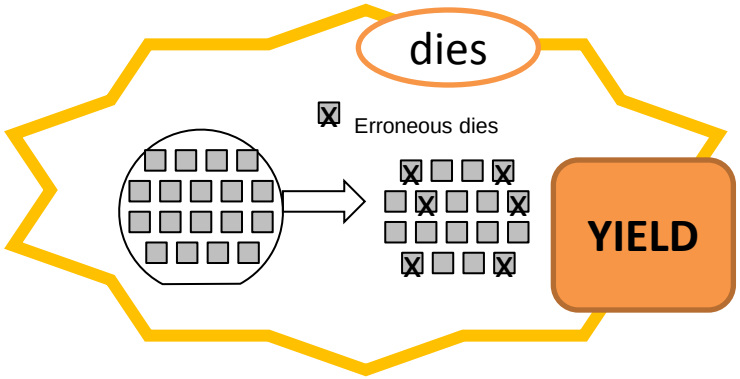
- Several hundred steps are required to manufacture ICs on a silicon wafer.



CMOS process sequence







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