MANUFACTURIING AND PACKAGING OF ICs

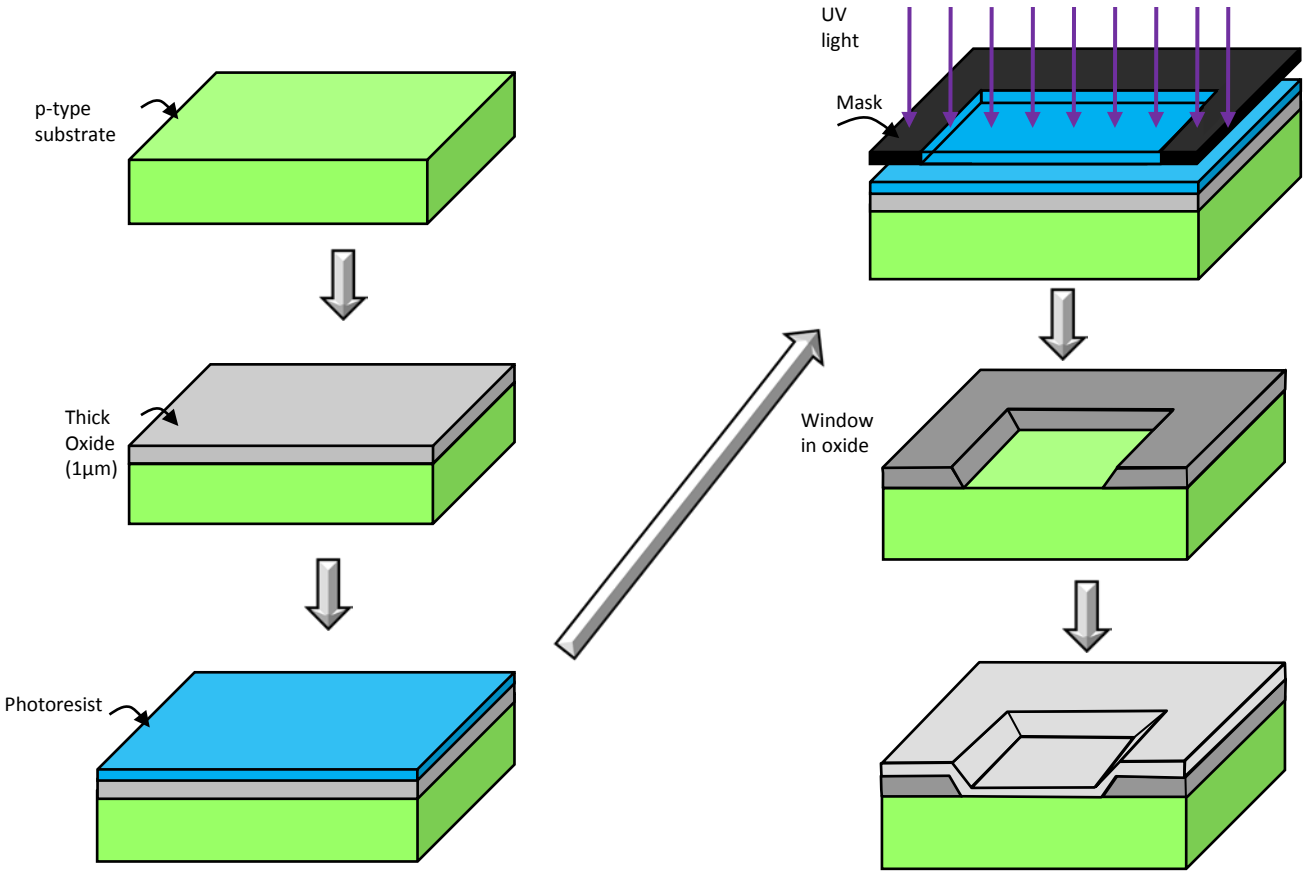
Authors:
Celia López
Mario García
Marta Portela
Almudena Lindoso
Luis Entrena
Enrique San Millán

CC BY NC SA

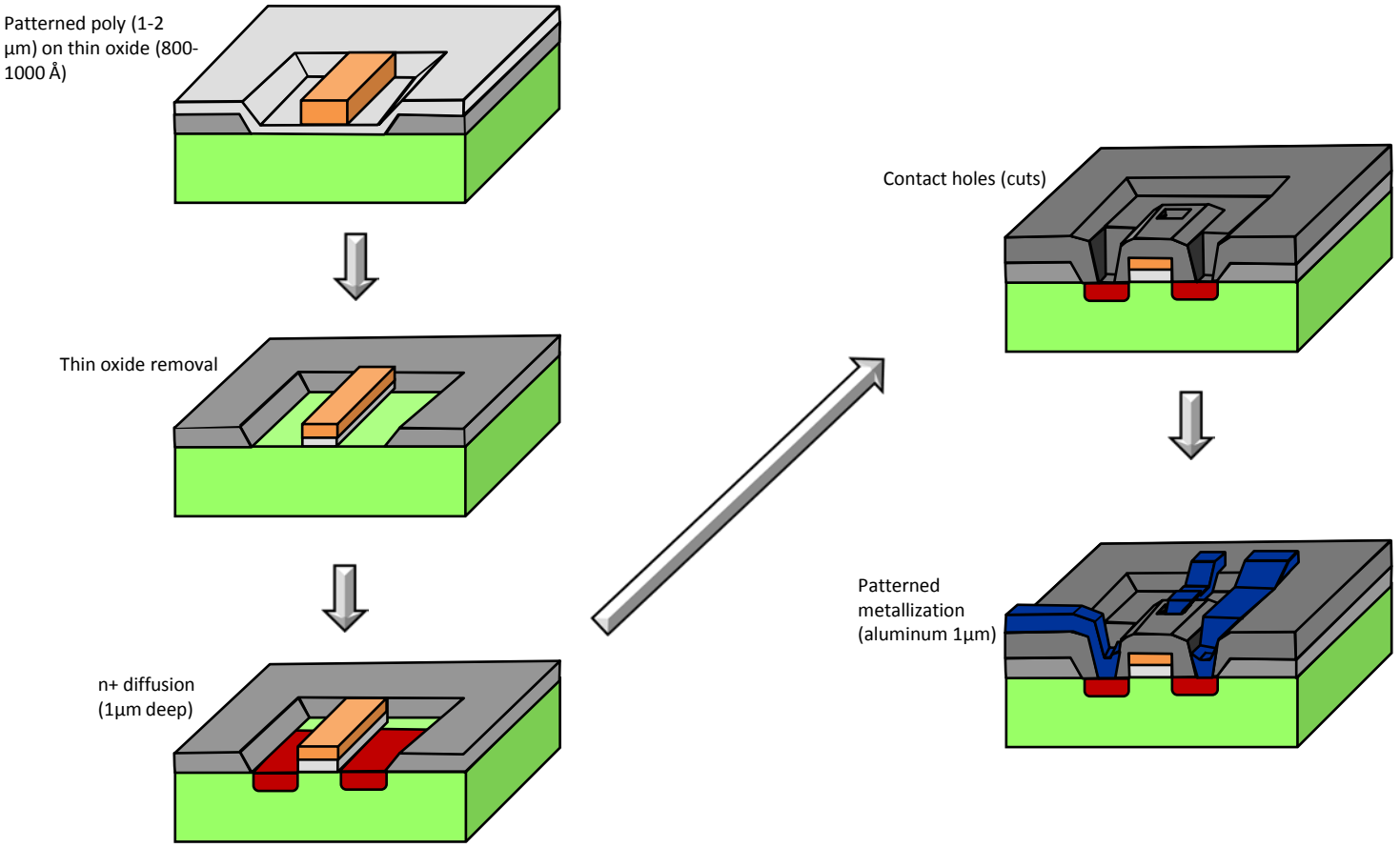
Outline

- Fabrication process of a CMOS circuit
  - NMOS transistor fabrication
  - Inverter fabrication
    - One well
    - Two wells (Twin-tub)
- Packaging of ICs
- Application Specific Integrated Circuits: kind and features

NMOS transistor fabrication(1/2)

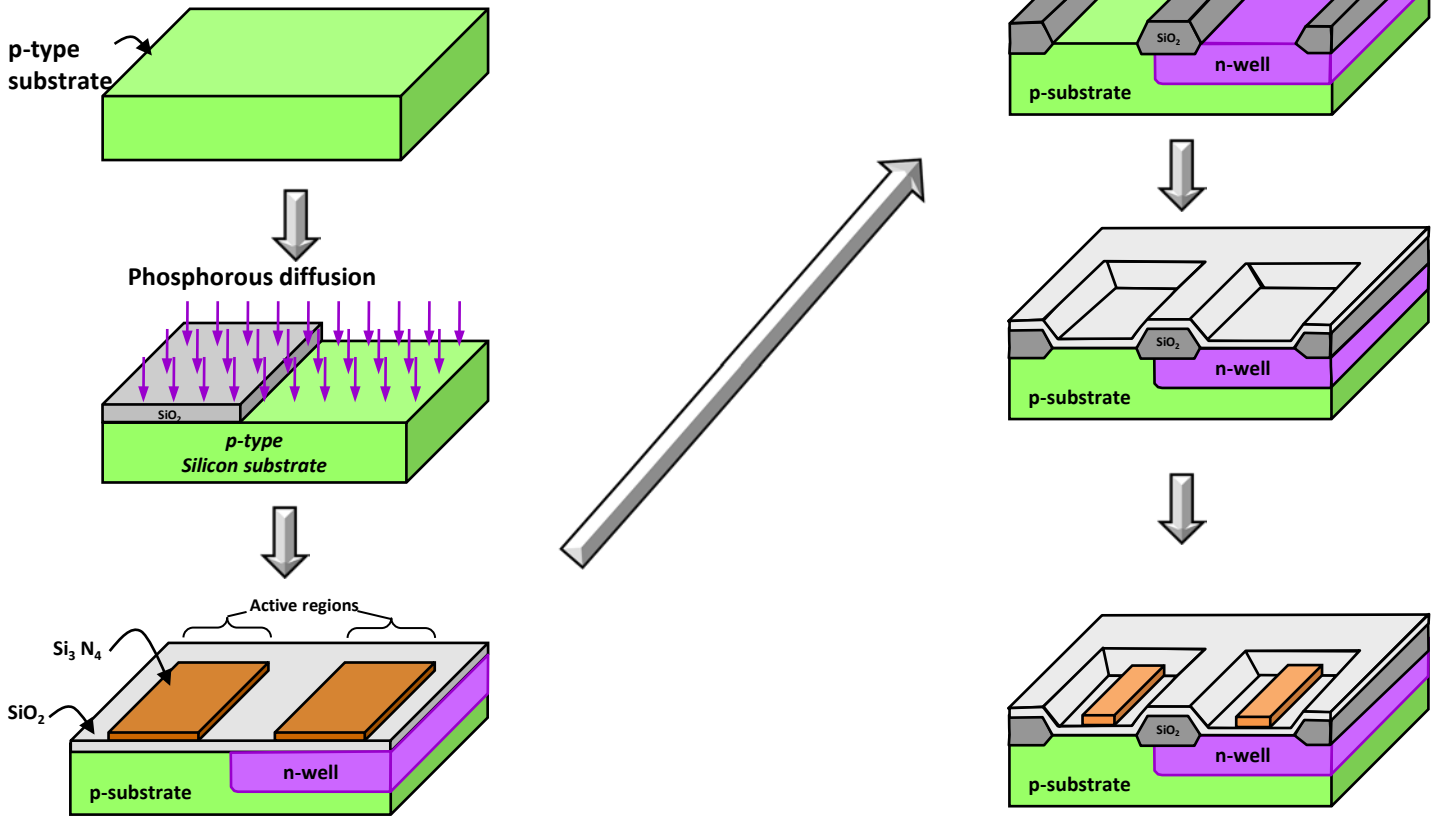


NMOS transistor fabrication(2/2)



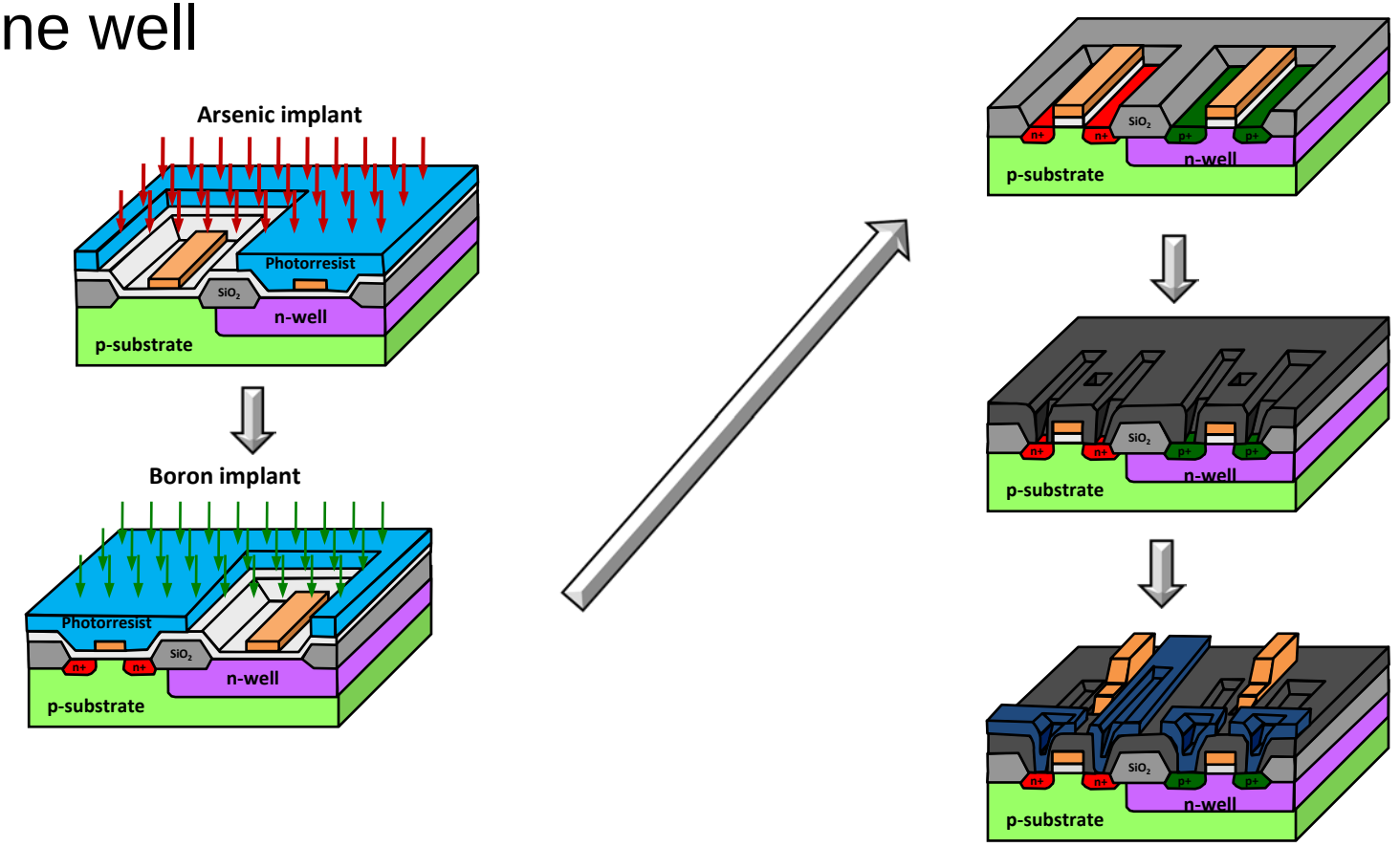
CMOS inverter fabrication (1/3)

- One well



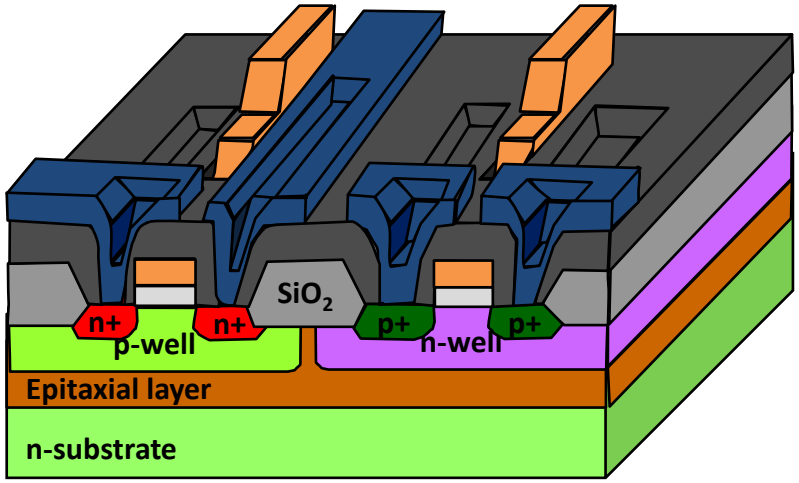
CMOS inverter fabrication (2/3)

- One well



CMOS inverter fabrication(3/3)

- Two well (twin-tub)



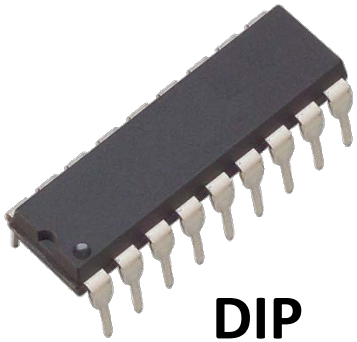
Packaging

- Objectives:
  - Isolation. Isolate the circuit against external factors like dust or humidity.
  - Connectivity. Pins allow the connection of input and output signals with the corresponding layers in the integrated circuit.
  - Heat dissipation. During normal behavior, the circuits generates heat that must be dissipated. The generated heat must scape through the package. Sometimes, when the package does not dissipate enough heat, adding a heat sink on the packaging is necessary.
  - Use. Since the integrated circuit die is very fragile, the package makes the handling, allocation and mounting easy.

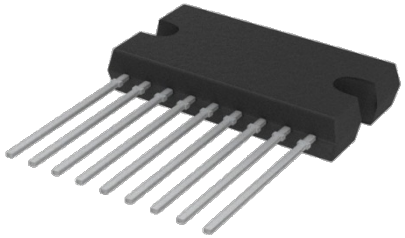
Packaging: Kind

Kind	Nº pins	Mount
DIP (Dual In-Line Package) SIP (Single In-Line Package) ZIP (Zig-Zag In-Line Package)	5-64	Insertion
SOIC (Small Outline Integrated Circuit) TSOP (Thin Small Outline Package) SSOP (Shrink Small Outline Package) TSSOP (Thin Shrink Small Outline Package) QSOP (Quarter-size Small Outline Package) VSOP (Very Small Outline Package)	8-32	Surface-mounted
LCC (Leaded Chip Carrier) PLCC (Plastic Leaded Chip Carrier) CLCC (Ceramic Leaded Chip Carrier)	16-200	Surface-mounted Insertion by using a socket
FP (Flat Pack) QFP (Quad Flat Pack) PQFP (Plasic Quad Flat Pack) CQFP (Ceramic Quad Flat Pack) TQFP (Thin Quad Flat Pack) LQFP (Low profile Quad Flat Pack)	10-300	Surface-mounted
PGA (Pin Grid Array) PPGA (Plastic Pin Grid Array) CPGA (Ceramic Pin Grid Array)	68-500	Insertion
BGA (Ball Grid Array)	>500	Surface-mounted

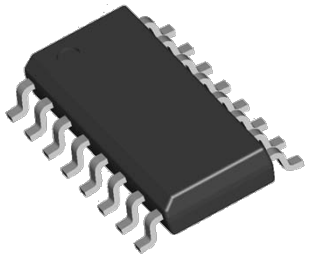
Packaging: Kind



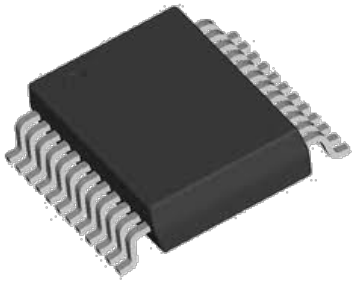
DIP



SIP

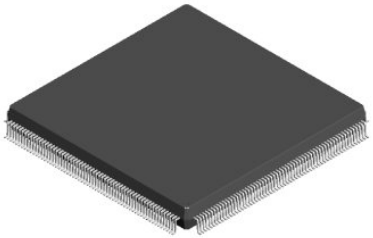


SOIC

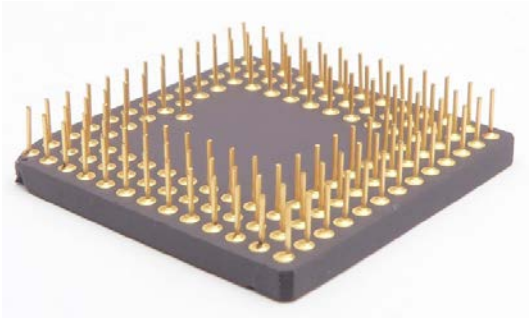


SSOP

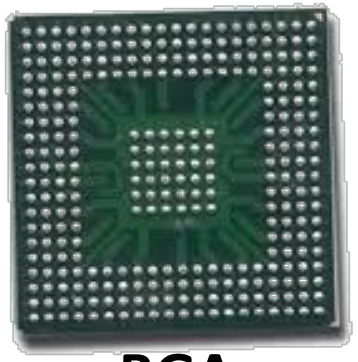
PLCC



QFP



PGA



BGA

Packaging: Multi-chip modules

- Multi-Chip Modules (MCM)
- It is a package that includes several circuits mounted in the same base and interconneted. Therefore, they are used as a single chip.
- There are several types of MCM with different integration level
- Examples: Pentium Pro, Xenos (GPU in Xbox)

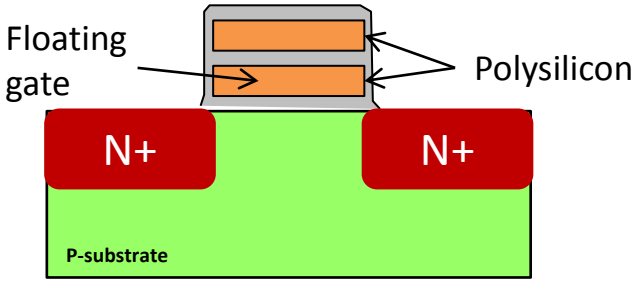
Type	Density interconnection (cm/cm^2)	Line width (µm)	Space among lines (µm)	Description
MCM-L	30	750	2250	Laminated MCM. The substrate is a multi-latyer printed circuit board (PCB). Low wiring densisty .
MCM-C	20-40	125	125-375	Ceramic substrate MCM. Medium wiring densisty.
MCM-D	200-400	10	10-30	Silicon substrate deposited MCM. High wiring densisty.

Application Specific Integrated Circuit

- ASICs : digital, analog or mixed circuits.
- Different possible implementations:
  - Full-custom
  - Semi-custom
    - Partially prefabricated: gate array
    - Partially predesigned: standard cells, macrocells, IP (Intelectual Property) blocks
  - Totally prefabricated circuits: programmable circuits
    - CPLDs (Complex Programmable Logic Devices)
    - SRAM FPGAs (Field-Programmable Gate Arrays)
    - Antifuse FPGAs

Application Specific Integrated Circuit

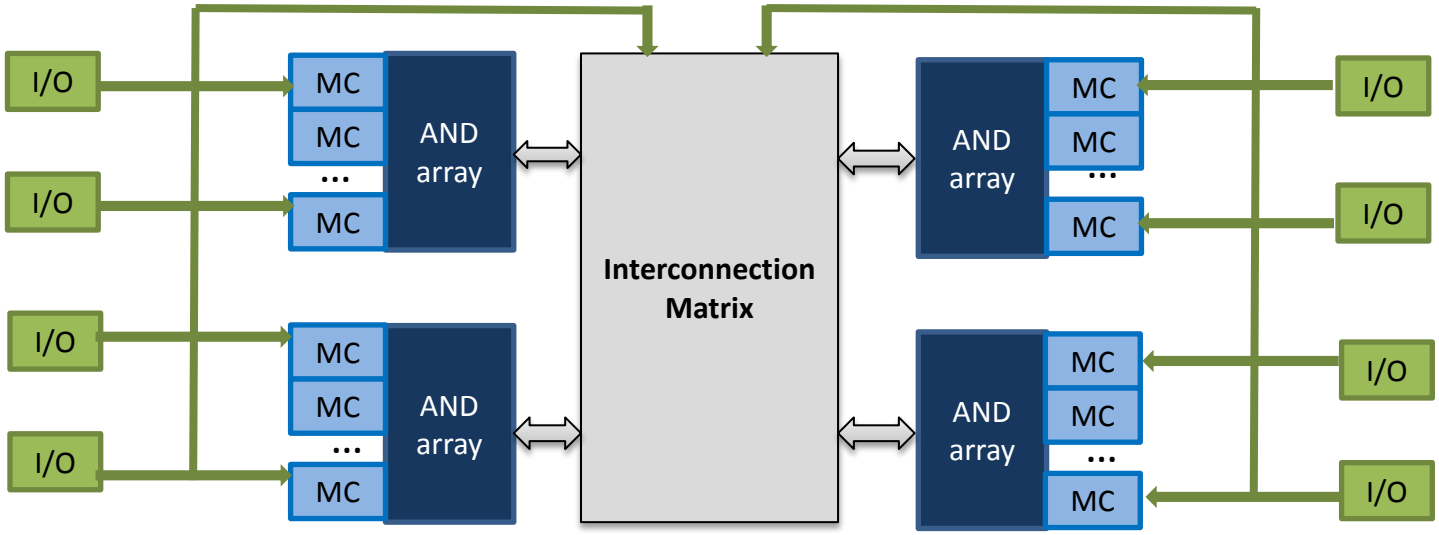
- Programmable circuits: CPLDs
  - Programming technology: Floating gate MOS transistor



    - If the transistor has not been programmed, it works in normal way.
    - Programmable threshold voltage.
      - When a voltage level, high enough, is applied in the transistor gate, the carriers can gain enough energy to go through the insulator, being trapped in the floating gate. Cell remains programmed when the voltage is removed.
  - Non-volatile
  - Reprogrammable
  - High power consumption

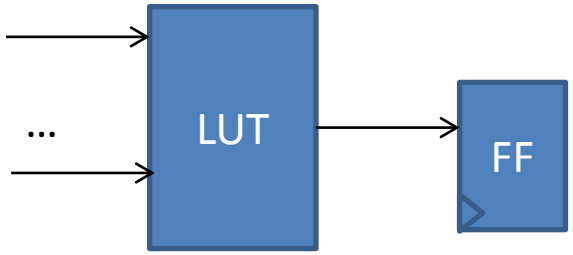
Application Specific Integrated Circuit

- Programmable circuits: CPLDs
  - Basic structure
    - Programmable interconnections
    - Logic blocks: Product terms, macrocells with flip-flops, inverters and multiplexers.
    - I/O cells



Application Specific Integrated Circuit

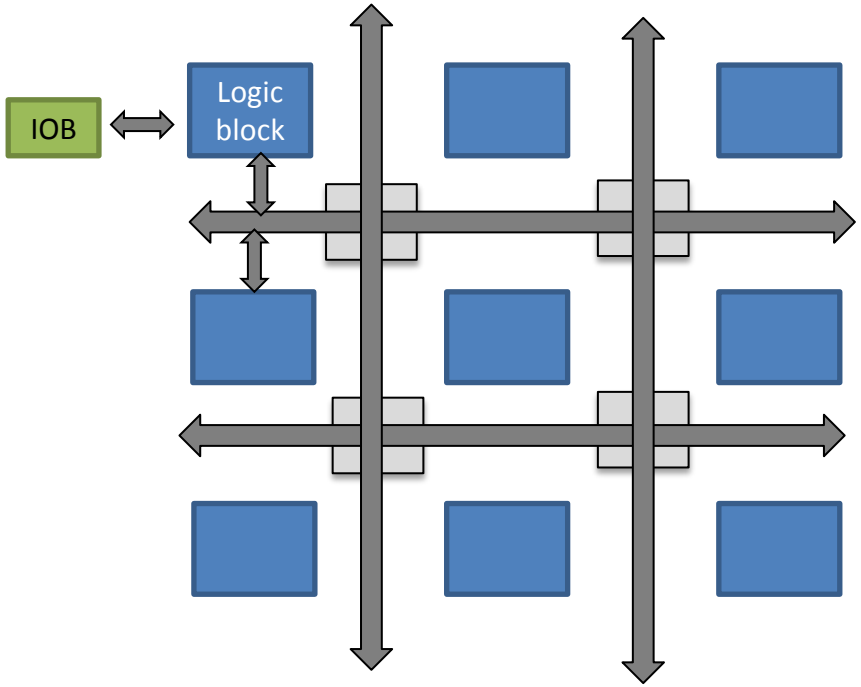
- Programmable circuits: SRAM FPGAs
  - Programming technology: SRAM cells for storing the circuit configuration
  - Basic cell
    - Flip-flop
    - Look-up Table (LUT)



  - Volatile devices
  - Reprogrammable
  - Higher integration capability → Higher complexity
  - Dynamic reconfiguration is possible

Application Specific Integrated Circuit

- Programmables circuits: SRAM FPGAs
  - Its internal structure consists in a matrix distribution of logic cells interconnect and connected to the input/output blocks by programmable routing channels



Application Specific Integrated Circuit

- Programmable circuits: Antifuse FPGAs
  - Programming technology: Antifuse. The necessary connections consists in shorcircuits produced during the programming process. In order to program the device, the antifuse (two electrodes separated by a thin insulator layer) is connected to a high voltage level that breaks the insulator producing a permanent shortcircuit.
  - Non volatile
  - Non reprogrammable
  - Fast devices→ Used for high-speed applications
  - Electric stability → high reliability
  - Specific devices are necessary in order to programm the antifuse FPGAs. These devices provide the voltage pulses with the suitable value and duration.
  - Internal structure: Only the interconnections can be programmed. The basic cells perform a stablished logic function.