TEST OF INTEGRATED CIRCUITS

Authors:

Enrique San Millán
Mario García
Celia López
Luis Entrena
Almudena Lindoso
Marta Portela

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Design for test

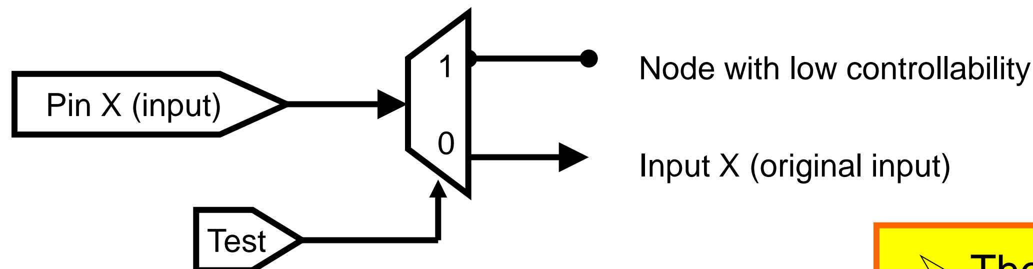
- Goal: increase the controllability and the observability of the circuit internal nodes.
- In general
  - The number of inputs and outputs increases
  - Worse performace (more area and slower)
- Applications:
  - Sequential logic vs. Combinational logic
  - Control logic vs. Data path
  - Asynchronous designs vs. Synchronous designs

Design for test

- DFT techniques
  - Ad-hoc
    - Not general solutions
    - Lower cost
    - More common in PCB designs, but also used in VLSI designs
  - Structured
    - They provide a design methodology for the testability problem
    - ATPG tasks and fault simulation with acceptable costs (sequential circuits)

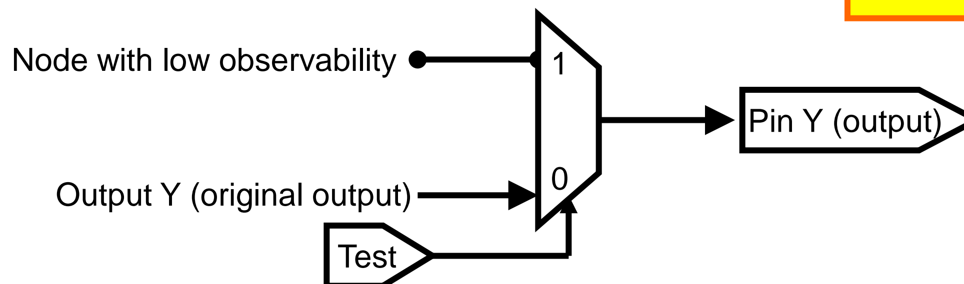
Design for test: soluciones ad-hoc

- Nodes with low testability (test points)
  - Increasing controllability



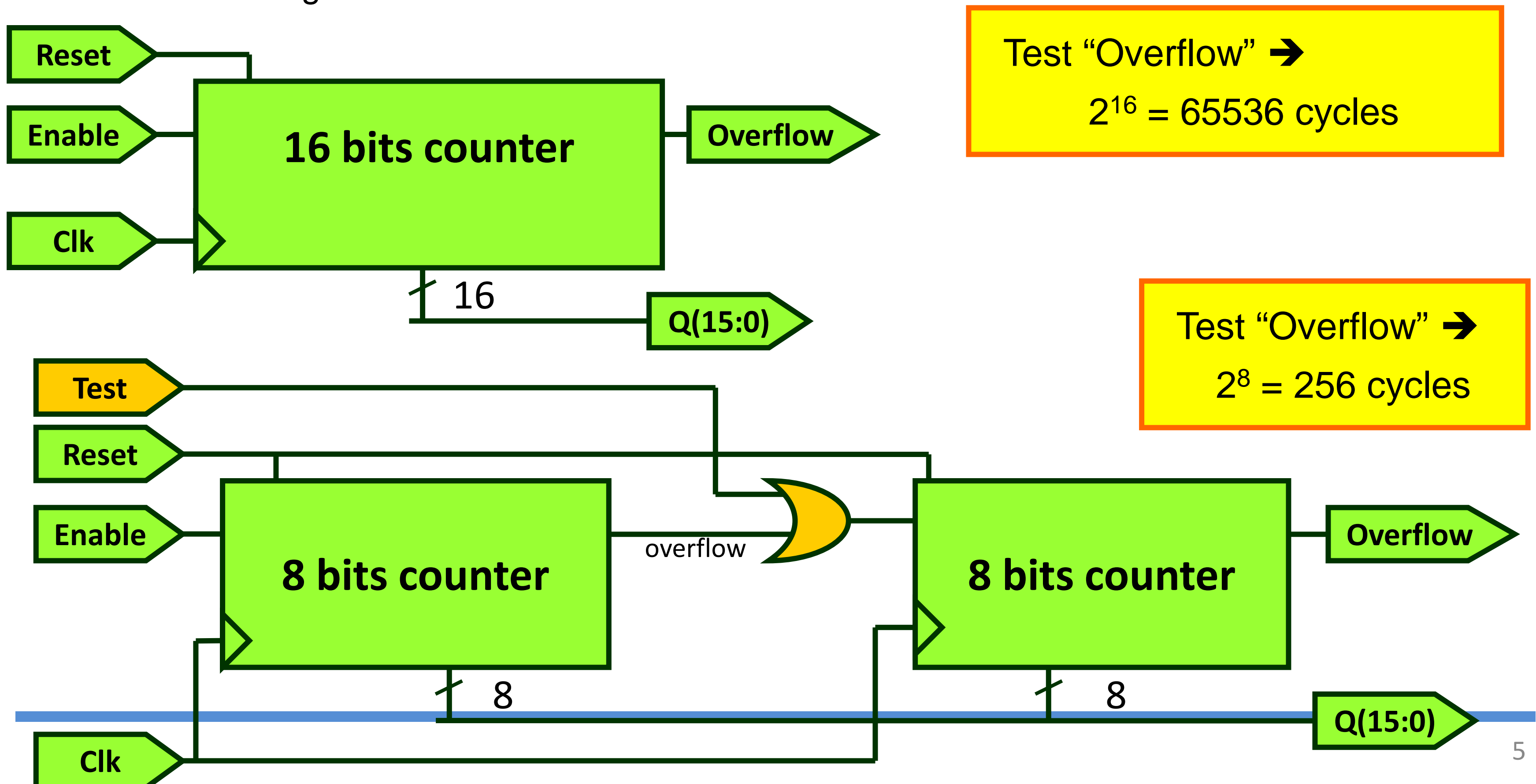
> ➢ They should be pins with low activity
> ➢ Never critical pins: clock, reset, chipselect, etc.

  - Increasing observability



Design for test: ad-hoc solutions

- Sequential circuits
  - Initialization + synchronous logic + avoid redundant logic
  - Partitioning counters



Test "Overflow" → 2^{16} = 65536 cycles

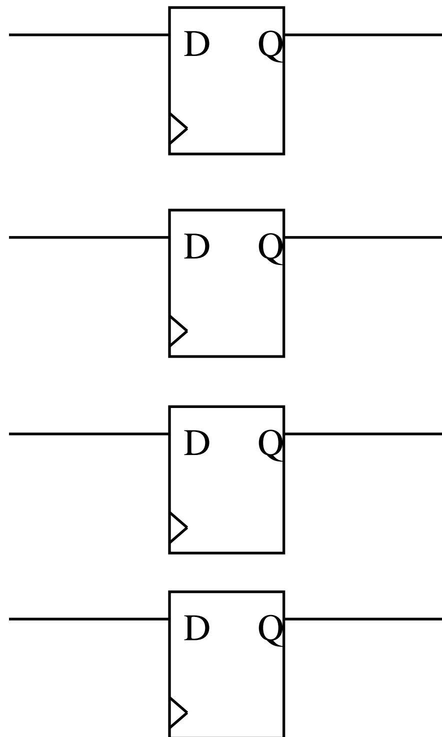
Test "Overflow" → 2^{8} = 256 cycles

Design for test: structured techniques

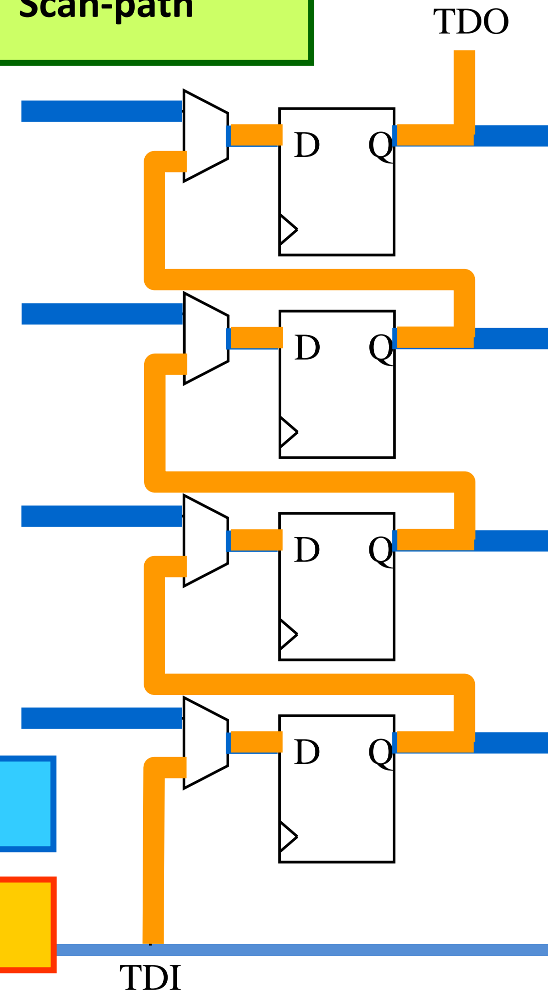
- Valid for synchronous circuits with only one clock edge
- Translate the problem of testing a sequential circuit into a problem of testing a combinationa circuit
- Affect the performance (area and maximum operating frequency)
- Two operation modes: TEST and NORMAL
- There are CAD tools that automatically insert those test structures, and automatically generate the test vectors
- The most common are:
  - Scan-Path
  - Boundary Scan
  - Built-In Self-Test

Design for test: Scan-Path

Flip-flops



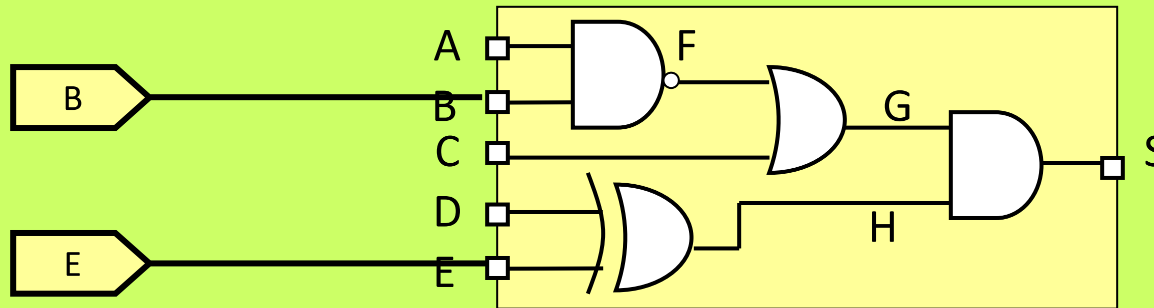
Scan-path



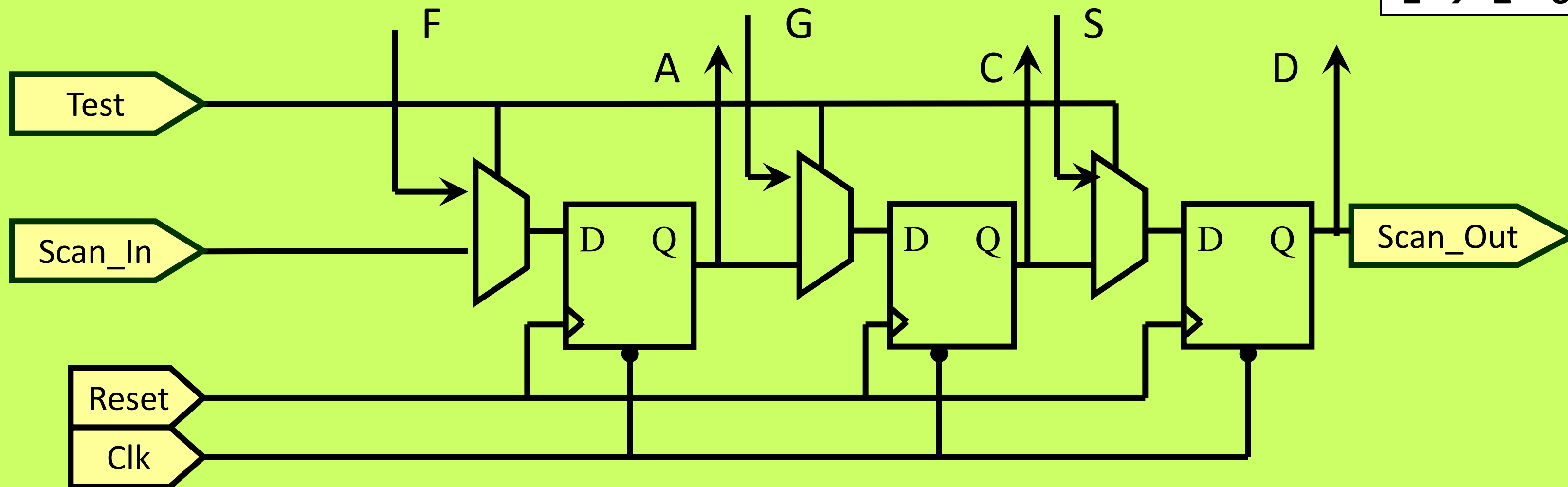
Normal mode

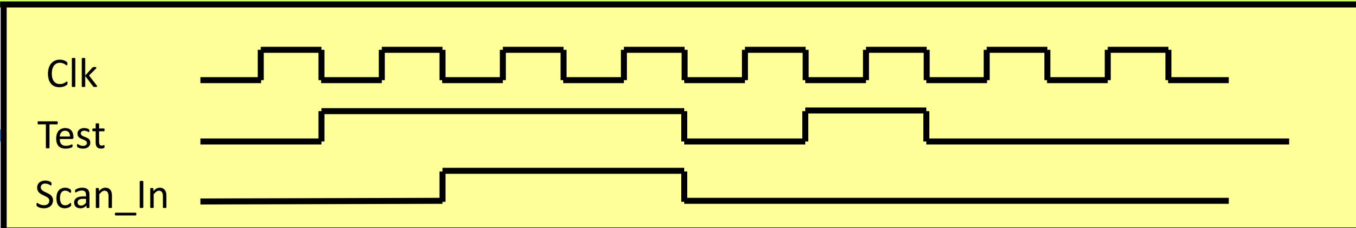
Test mode

Design for test: Scan-Path

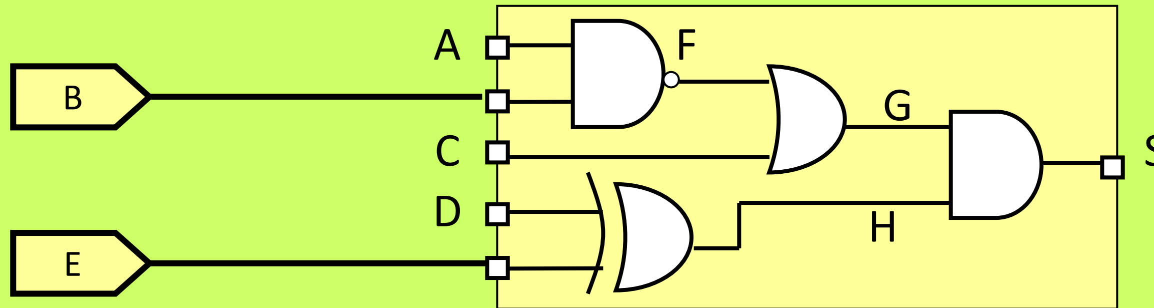


s-a-0 on H
A → 1 - 0
B → 1 - 0
C → 1 - 0
D → 0 - 1
E → 1 - 0





Design for test: Scan-Path



s-a-0 on H
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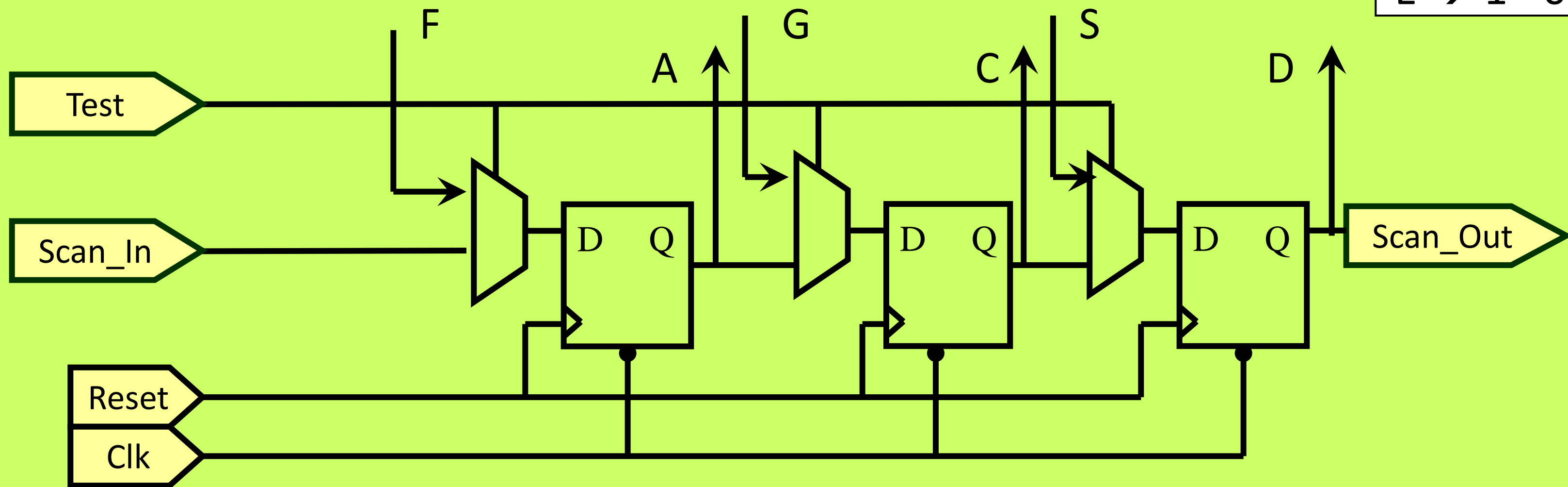

Number of cycles without Scan Path?