UNIVERSIDAD CARLOS III DE MADRID

VHDL Exercises

Integrated Circuits and Microelectronics

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Problem 1

Design a circuit that generates a digital signal S with the following characteristics:

a) Idle level: LOW
b) While in idle, if START is activated during at least one clock cycle, a 10 μs high pulse should be generated. After that, S should go back to LOW again, and then it will be waiting for the activation of G.
c) Then, if G is activated during at least one clock cycle, a 500 ns high pulse should be generated. After that, the system goes back to idle again.
d) Signals START and G will be considered only if they are activated at the corresponding moment: START should be taken into consideration only in idle state, and G only once START has been activated.

The clock frequency that will be used for this circuit is 20 MHz.

Inputs

CLK: circuit clock, falling edge triggered
RESET: asynchronous signal, used to initialize the circuit (active-low)
START: Active-high
G: Active-high

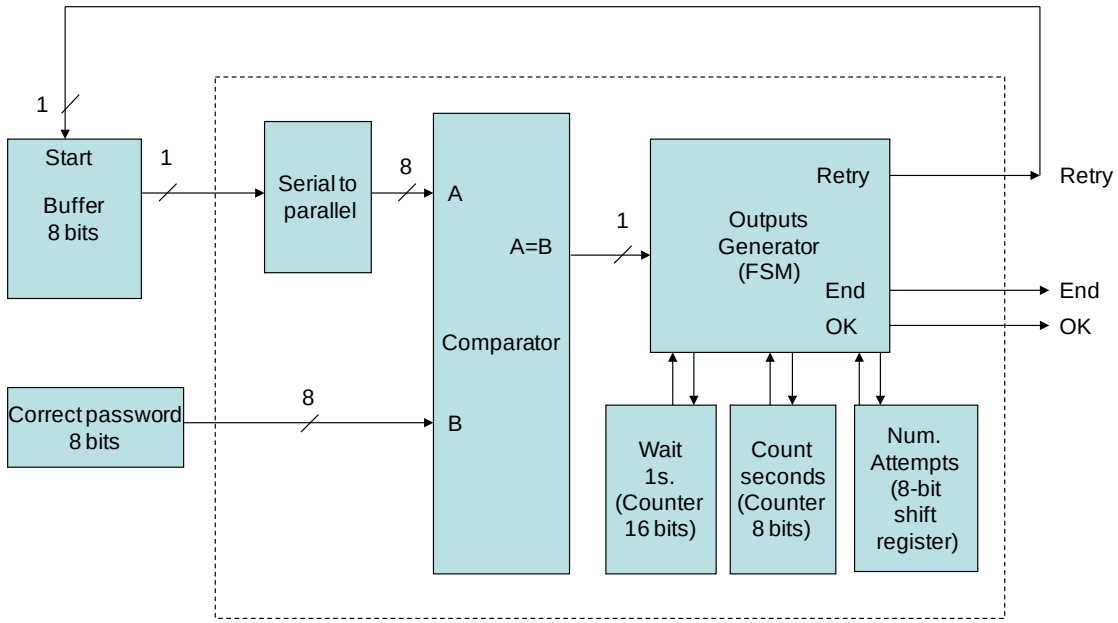
Outputs

S: Pulses signal generated by this circuit

Describe the entity and architecture of this circuit using VHDL

Problem 2

Design a digital circuit that checks if a password that is introduced through a serial input matches a previously stored value in a register (buffer).



Circuit inputs:

CLK: circuit clock, rising edge triggered. Frequency: 50 kHz

RESET: asynchronous signal, used to initialize the circuit, active-low.

SERIAL_IN: signal used to receive bits corresponding to the password attempt

(serial).

PASSWORD: 8-bit input used to receive the correct password (parallel).

Circuit outputs:

END: signal that activates (active-high) when the process has finished.

OK: signal that activates (active-high) when the password is correct.

RETRY: Signal that activates each time that a new password attempt is introduced.

The circuit should work according to the following specifications:

The circuit receives, bit by bit, a 8-bit password attempt through the input SERIAL_IN. The correct password is previously stored in an external buffer outside the circuit, and it can be read at any time through the 8-bit input PASSWORD.

So that the correct password can be compared with the password attempt, the circuit first converts the received bits of the password attempt into an 8-bit datum. Once this operation is completed, both data are compared with a comparator.

With the comparison result 3 outputs are generated:

END output is activated if the process has finished, because the password is correct, or because the maximum number of attempts has been reached.

OK output is activated if the result of the comparison indicates that both data are equal.

RETRY output is activated to indicate that the system is ready for a new attempt (when the comparison fails but still the maximum number of attempts has not been reached).

This output has a special synchronization. For security reasons, each time that a wrong password is detected the circuit will use a delay until a new attempt is allowed. This delay will be increasing with each wrong password (double time with each attempt). The first time the delay will be 1s. The second time the delay will double (2s.), the third time will be 4s, and so on, until a maximum of 8 possible attempts is reached. In this case, if the maximum number of attempts is reached, the END output will be activated.

a) Describe in VHDL the entity of the full circuit.
b) Design in VHDL an entity and architecture to describe an 8-bit shift register. Besides the reset and clock inputs, it has a SERIAL_IN input, an R/L input to indicate the direction of the shifting (right if R/L=0 and left if R/L=1), and the output is the value of the register (8 bits).
c) Design a process that describes a comparator of two 8-bit data. The output is EQUAL (1 if A is equal to B, 0 if they are different).
d) Design a process that describes a 16-bit counter. This counter will have inputs clock, reset, enable, and an output that will be activated when the counter arrives at the necessary value that corresponds to one second.
e) Design with a process an 8-bit counter with inputs clock, reset, enable and an 8-bit output with the count value.
f) Using the previously designed elements, describe the entity of the full circuit. Consider the following tips:
    1. For the serial-parallel converter, the shift register of b) can be considered. Use right shifting.
    2. Fort the outputs generator block, use the 16-bit counter, the 8-bit counter, and an instance of the shift registrar of b) to obtain the x2 multiplications (multiply by two is equivalent to shifting one bit right and introducing a 0 in the LSB).
g) Describe in VHDL a testbench for the circuit. Justify the selection of tests that you have considered for it.

IMPORTANT NOTE: Everything in the circuit has to be completely synchronous, except for the initialization with an asynchronous reset. Comment conveniently the code and include diagrams to simplify the understanding of your code.