UNIVERSIDAD CARLOS III DE MADRID

MODULES 2-4 EXAM

Integrated Circuits and Microelectronics

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INTEGRATED CIRCUITS AND MICROELECTRONICS EXAM

NAME AND SURNAME:	**GROUP:**

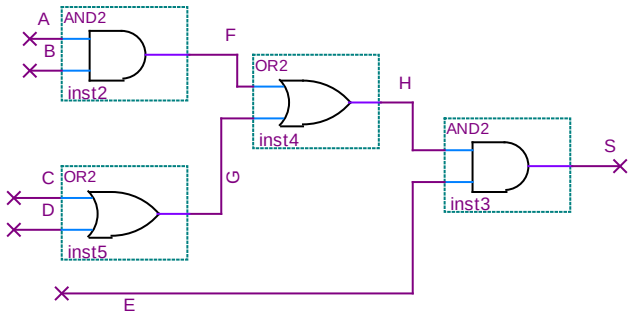
Question 1 (1.75 points)

Diffusion and ion implantation are processes used during the manufacturing process of integrated circuits.

1) Explain both processes and what they are used for.
2) Compare both techniques and explain the advantages and disadvantages of each one with respect to the other.

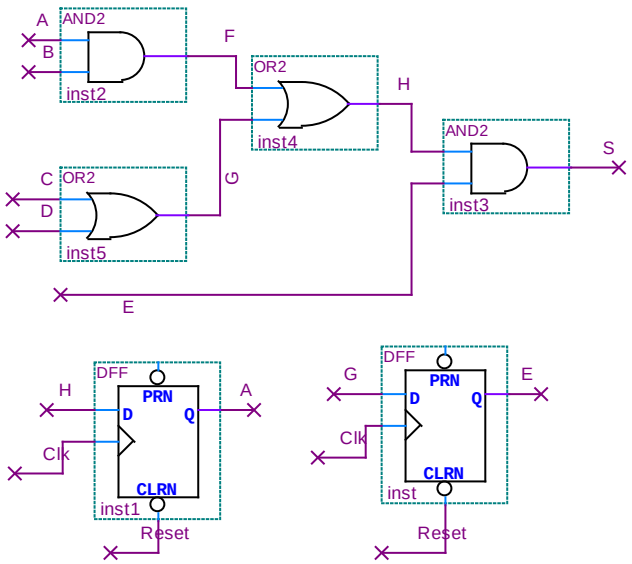
Question 2 (2.75 points)

a) Generate a test vector for the fault stuck-at 0 in net F for the following combinational circuit.



b) Determine the fault coverage obtained with the test vector generated in the previous point. Which is the minimum number of test vectors necessary to obtain 100% stuck-at fault coverage? Determine them.

c) Consider now the following circuit:



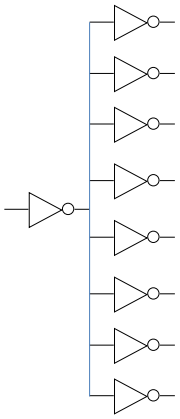
Add the scan-path structure along with the necessary logic to test the circuit.

d) Considering the circuit of section c), draw a timing diagram to show the test process for detecting the stuck-at 0 fault in F. This timing diagram must include all the

necessary inputs and outputs to perform the test. Point out in the timing diagram which test step is being performed at every moment.

Question 3 (2.75 points)

a) Consider the following circuit, where all the inverters have standard size, and the output ones have the delay of a standard inverter (t_{pi}).



Modify the circuit, without changing the transistors sizes, to obtain the lowest possible delay in the critical path of the circuit (path with highest delay), trying to add the least possible area.

b) Now we want to optimize the delay of an integrated circuit output gate. The equivalent load that this gate has at its output is 5000 times the standard load. To get this reduction is used an increasing width size (W) buffer chain with 5 inverters, using the following relation:

W, 3W, 5W, 7W, 9W

1. Calculate the delay (as a function of the delay of a standard inverter) that the gate has before and after adding the buffers chain.
2. Calculate the area increase (as a function of the size of a standard inverter A_i)
3. Obtain the delay that would be obtained with the optimal solution, and calculate the area overhead that is needed for this solution.

	Delay	Area overhead
Initial		-
W, 3W, 5W, 7W, 9W		
Optimal solution		

Note: your solution must include this table with the solutions

Question 4 (2.75 points)

Consider the layout circuit in Fig. 1.

a) Obtain the associated transistors level circuit.
b) Represent using logic gates the circuit, pointing out which part corresponds to each part.
c) Draw the transverse section of the layout for the line MN.

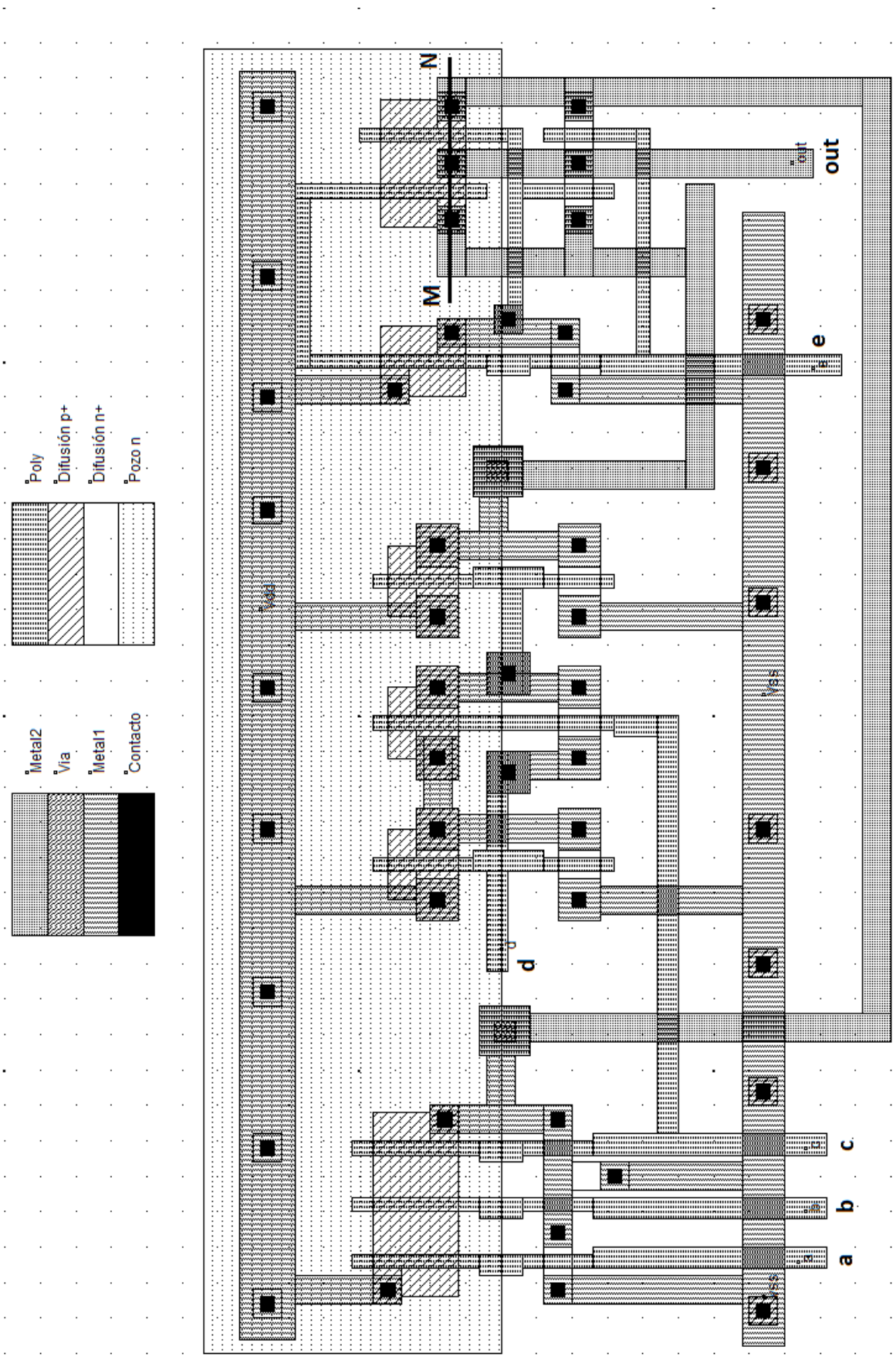

Poly
Difusión p+
Difusión n+
Pozo n
Metal2
Via
Metal1
Contacto
N
M
out
e
d
a
b
c

Fig. 1