UNIVERSIDAD CARLOS III DE MADRID

Layout Exercises

Integrated Circuits and Microelectronics

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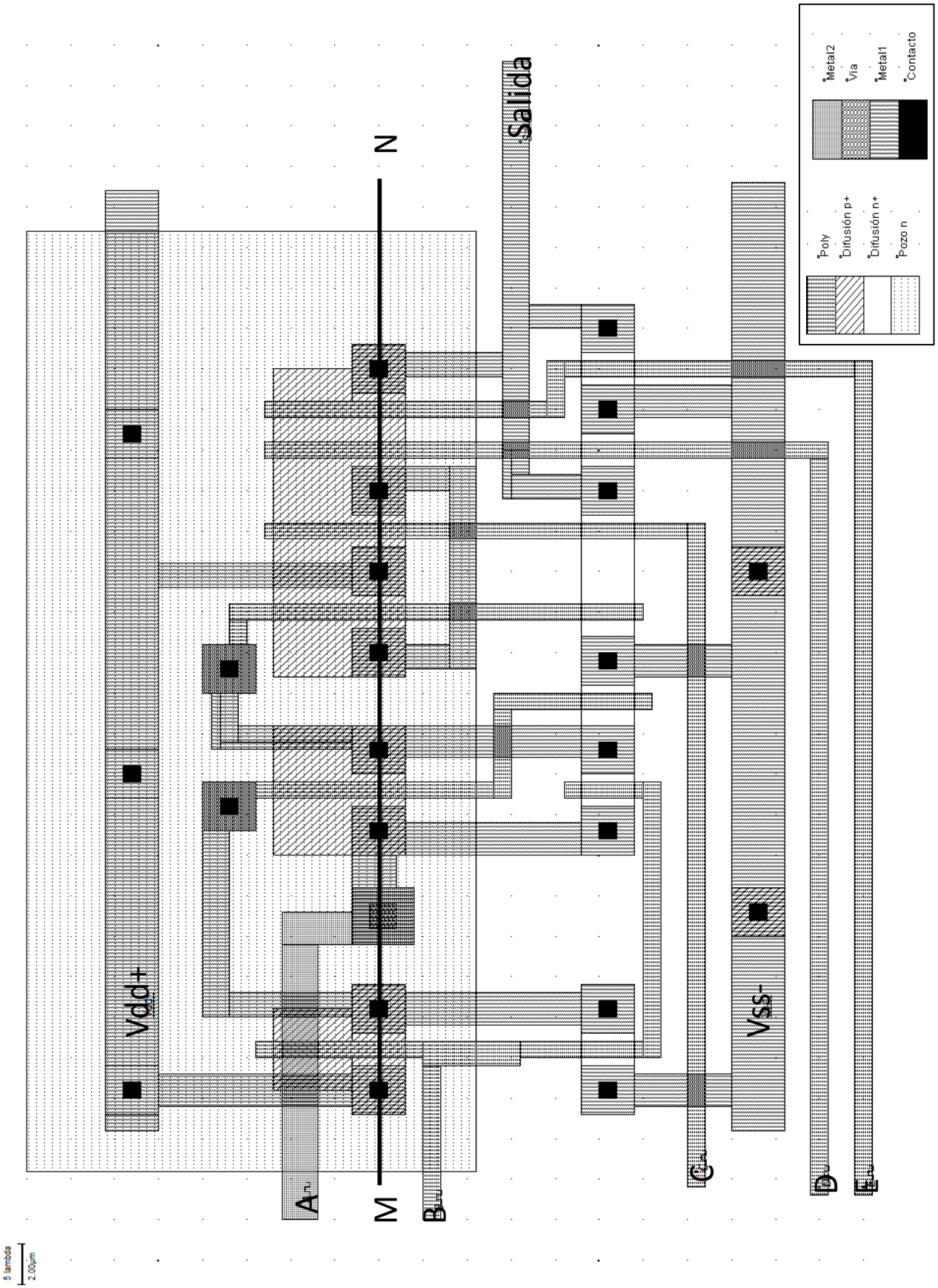
Exercise 1

Answer the following questions regarding the layout shown in the figure:

a) Obtain the corresponding transistor level scheme.
b) Represent with logic gates the circuit. Point out which set of transistors corresponds to each logic gate.
c) Draw the cross section of the layout through the line MN.
d) Let be the logic function y=a+b (logic OR). Design *y* by only using pass transistor logic. Describe the transistor scheme and draw the corresponding layout.


Metal2
Via
Metal1
Contacto
Poly
Difusión p+
Difusión n+
Pozo n
Salida
N
M
Vdd+
Vss-
A
B
C
D
E
5 lambda
2.00µm

Exercise 2

Consider the layout circuit in Fig. 1.

a) Obtain the associated transistors level circuit.
b) Represent using logic gates the circuit, pointing out which part corresponds to each part.
c) Draw the transverse section of the layout for the line XY.

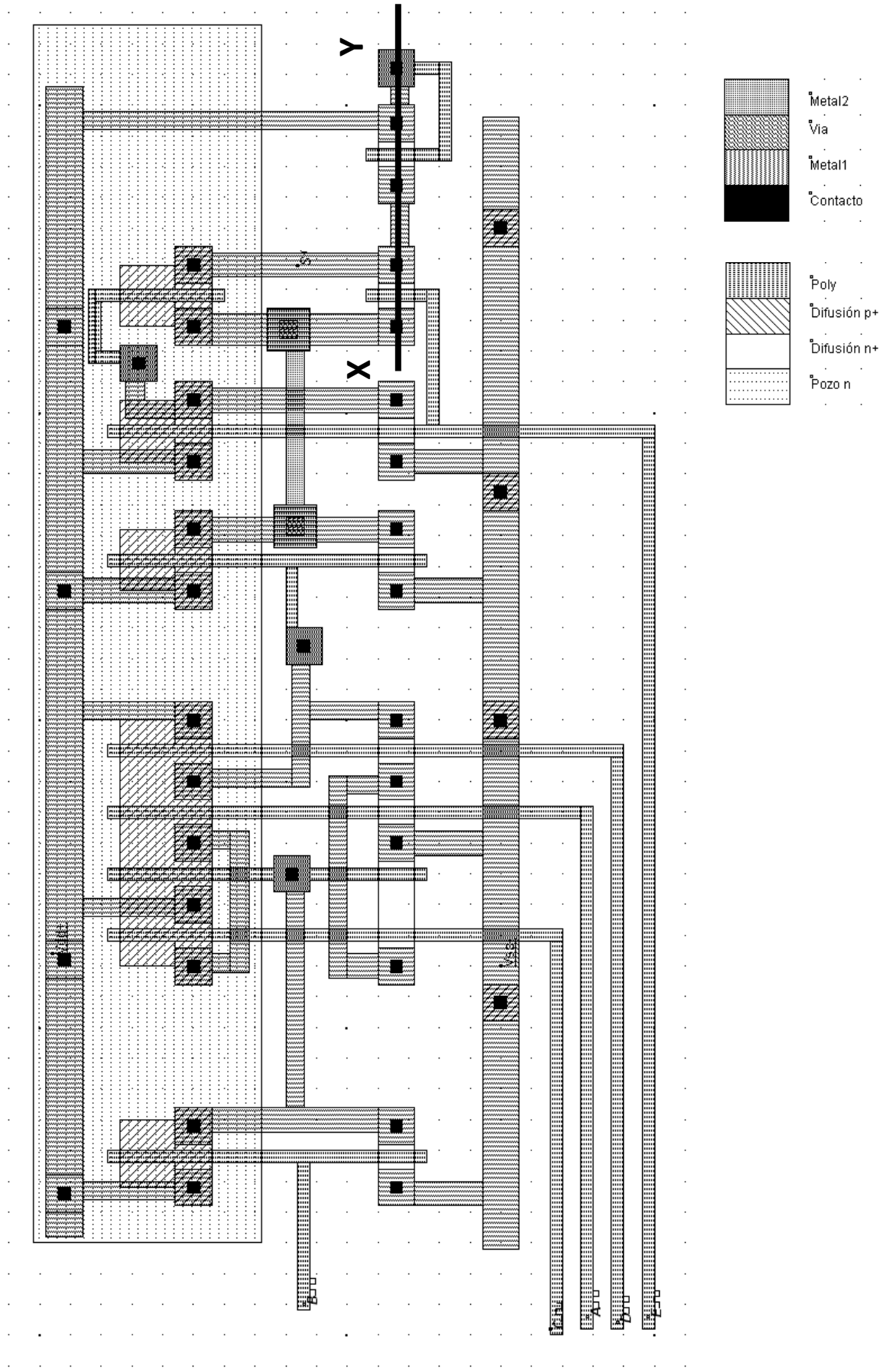

Y
X
Metal2
Via
Metal1
Contacto
Poly
Difusión p+
Difusión n+
Pozo n

Fig. 1