



Universidad
Carlos III de Madrid

Instrumentación Electrónica con Microprocesador II: Procesadores Avanzados

**Microprocesadores empotrados en FPGAs.
Entorno de desarrollo de Xilinx**

Marta Portela García



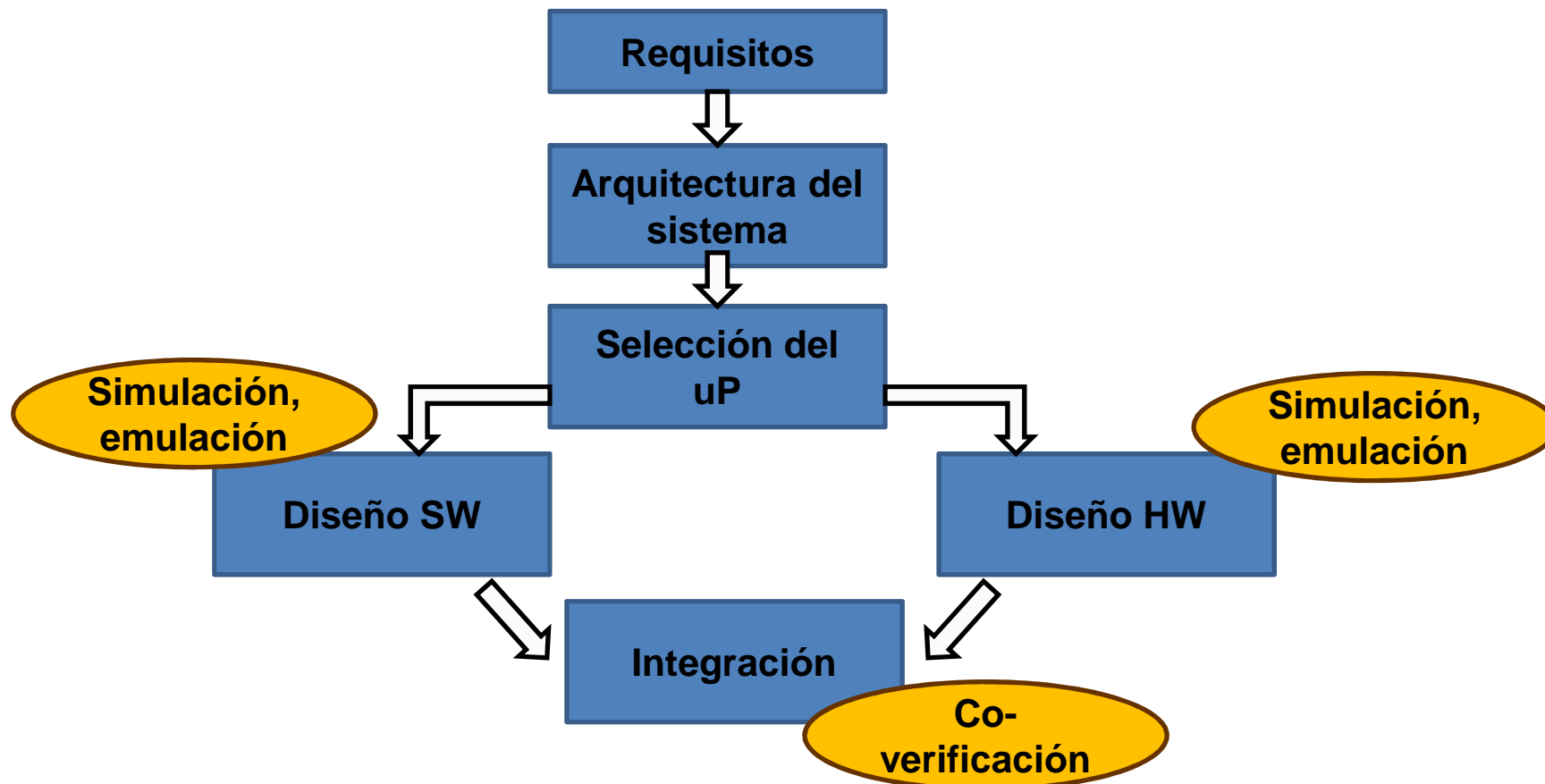


DISEÑO DE SISTEMAS EMPOTRADOS

- Sistemas de alta complejidad. El desarrollo del diseño debe ser rápido (time-to-market) y efectivo en coste.
- Herramientas para el desarrollo de sistemas empotrados que facilitan la tarea de diseño y la aceleran.
 - Xilinx → Integrated System Environment (ISE) Design Suite: Embedded Edition
- Integración de HW y SW
- División de la implementación (Co-diseño)

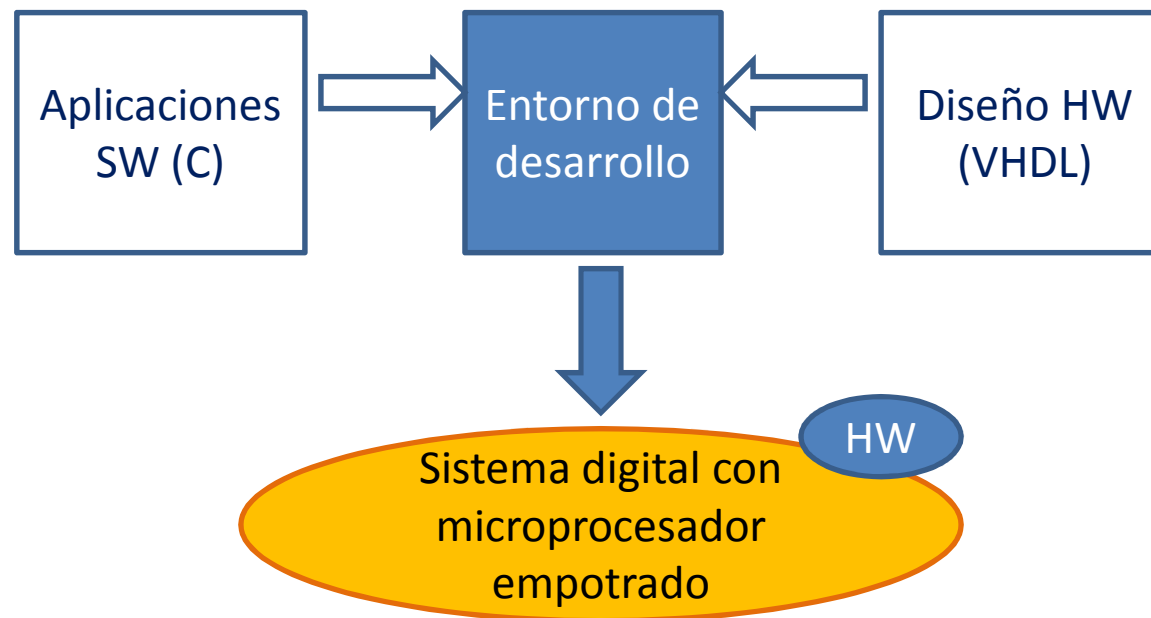
DISEÑO DE SISTEMAS EMPOTRADOS

- ¿Qué funciones debe realizar el hardware y cuáles el software?



HERRAMIENTAS NECESARIAS PARA EL DISEÑO DE SISTEMAS CON uPs EMPOTRADOS

- Entorno de desarrollo con un compilador cruzado
- Programador
- Depurador hardware (OCD → JTAG)

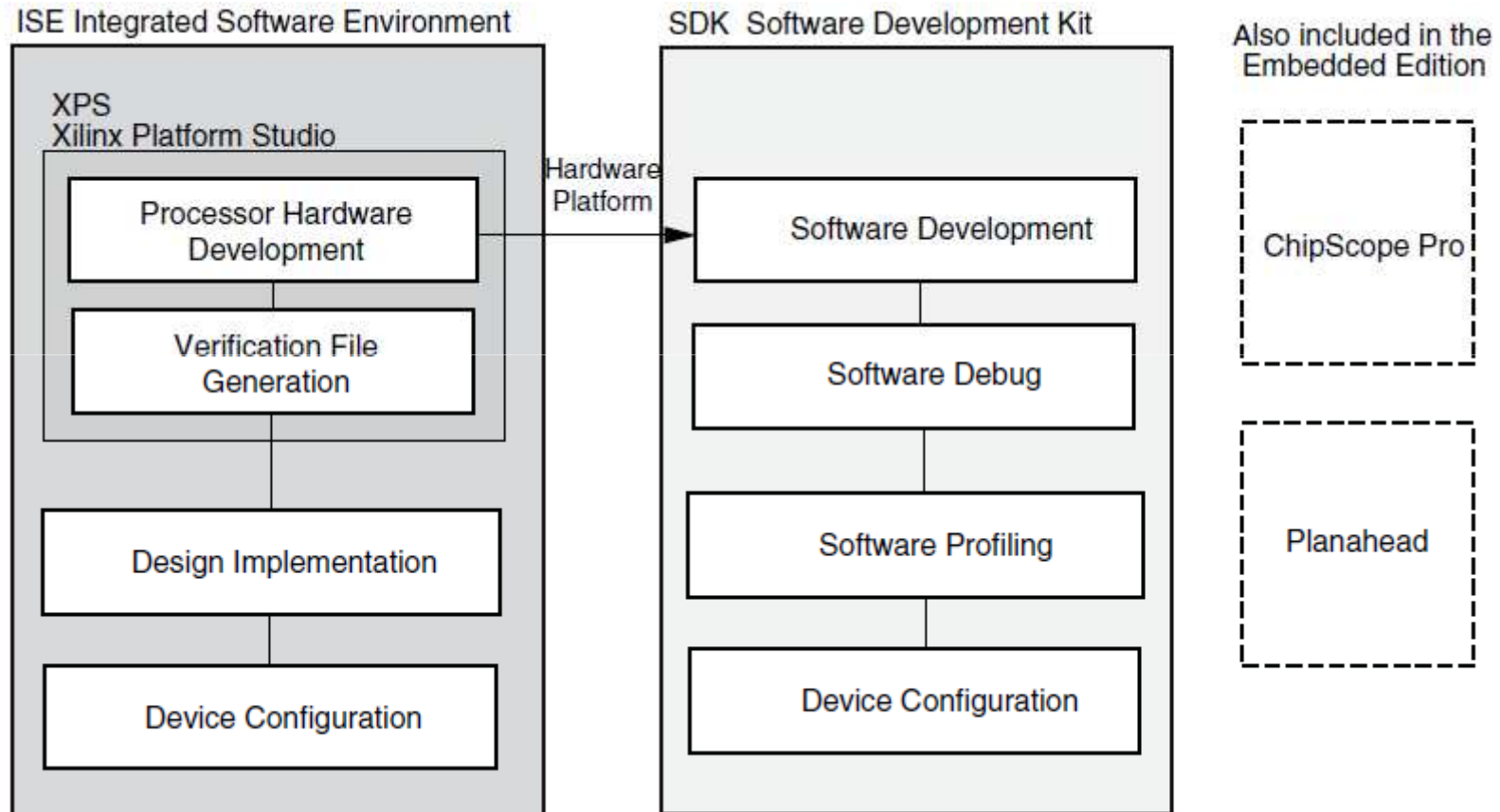




HERRAMIENTAS DE DISEÑO. ISE DESIGN SUITE: EMBEDDED EDITION

- **ISE** (Integrated Software Environment). Entorno de desarrollo necesario para utilizar el resto de herramientas.
- **EDK** (Embedded Development Kit)
 - **XPS** (Xilinx Platform Studio). Para el diseño de la parte HW del sistema con procesador empotrado.
 - Base System Builder (BSB)
 - Platform Generator
 - Library Generator (LibGen)
 - **SDK** (Software Development Kit). Para el diseño en C/C++ de la aplicación SW y su verificación.
 - **Otros componentes:**
 - HW IP
 - Drivers y librerías
 - Compilador GNU y depurador SW para
- **PlanAhead, ChipScope Pro**

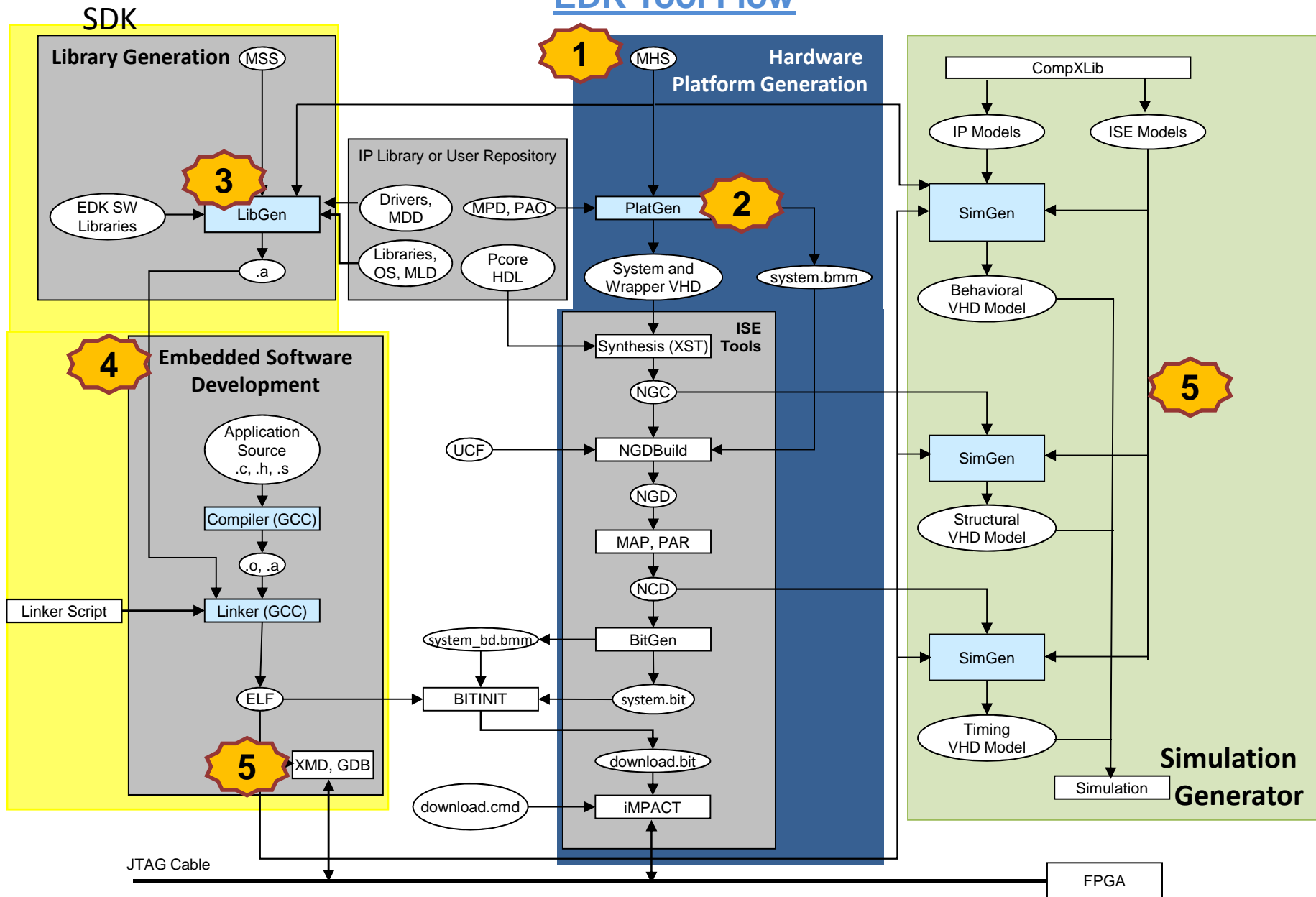
HERRAMIENTAS DE DISEÑO. ISE DESIGN SUITE: EMBEDDED EDITION



"EDK Concepts, Tools, and Techniques. Guide to Effective Embedded System Design" Xilinx



EDK Tool Flow





CREAR UN NUEVO DISEÑO: BSB

The screenshot shows the Xilinx Platform Studio interface with the Base System Builder wizard open. The wizard is titled "Base System Builder" and has tabs for Welcome, Board, System, Processor, Peripheral, Cache, Application, and Summary. The "Board" tab is active, showing the "Board Selection" step. The user has selected "I would like to create a system for the following development board". The board details are as follows:

Board Vendor	Board Name	Board Revision
Xilinx	Spartan-3E Starter Board	C

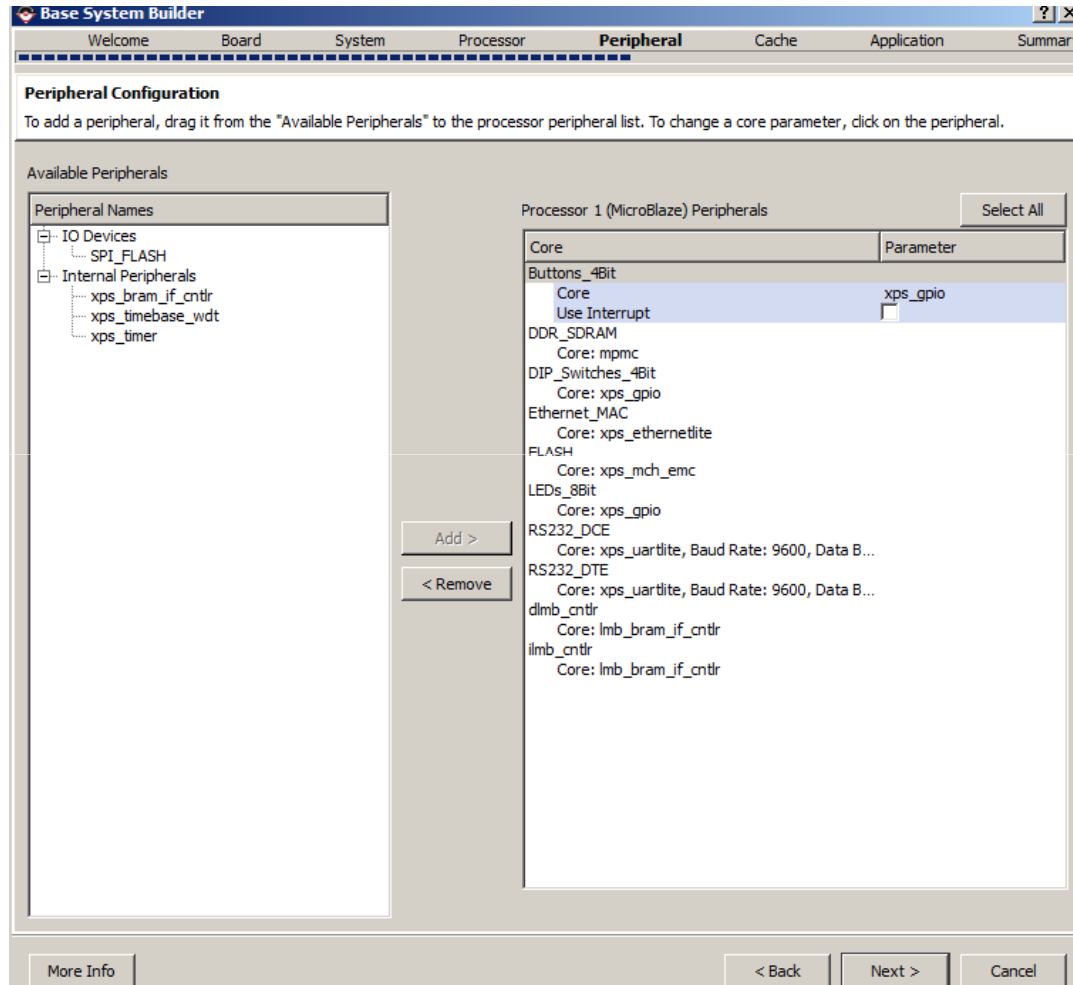
Below the board selection, there is a "Board Information" section with the following details:

Architecture	Device	Package	Speed Grade
spartan3e	XC3S500E	FG320	-4

Additional options include "Use Stepping" (unchecked) and "Reset Polarity" (Active High). The "Related Information" section contains links for "Vendor's Website", "Vendor's Contact Information", and "Third Party Board Definition Files Download Website". A descriptive paragraph follows: "Spartan-3E Starter Kit Board utilizes Xilinx Spartan-3E XC3S500E-4FG320 device. The board includes 2 RS232 serial ports, 4 DIP switches, 4 push buttons, 8 LEDs, VGA port, character LCD display, PS/2 port, push button rotary encoder, SPI analog to digital converter, SPI digital to analog converter, 10/100 Ethernet port, 2MB SPI flash, 16 MB of parallel NOR flash and 32 MB DDR SDRAM. Push button South(RESET) is used as system reset."

At the bottom of the wizard, there are buttons for "More Info", "< Back", "Next >", and "Cancel". The Xilinx Platform Studio interface also shows a "Create new or open existing project" dialog box with options for "Base System Builder wizard (recommended)", "Blank XPS project", and "Open a recent project".

CREAR UN NUEVO DISEÑO: BSB



- Seleccionar la placa
- Configurar el sistema
- Configurar el procesador
- Seleccionar y configurar los periféricos
- Configurar la caché
- Generar el diseño
 - Se generan aplicaciones de test para los distintos periféricos



HW DEL SISTEMA EMPOTRADO: XPS (XILINX PLATFORM STUDIO)

Crear nuevo IP

Panel de conectividad

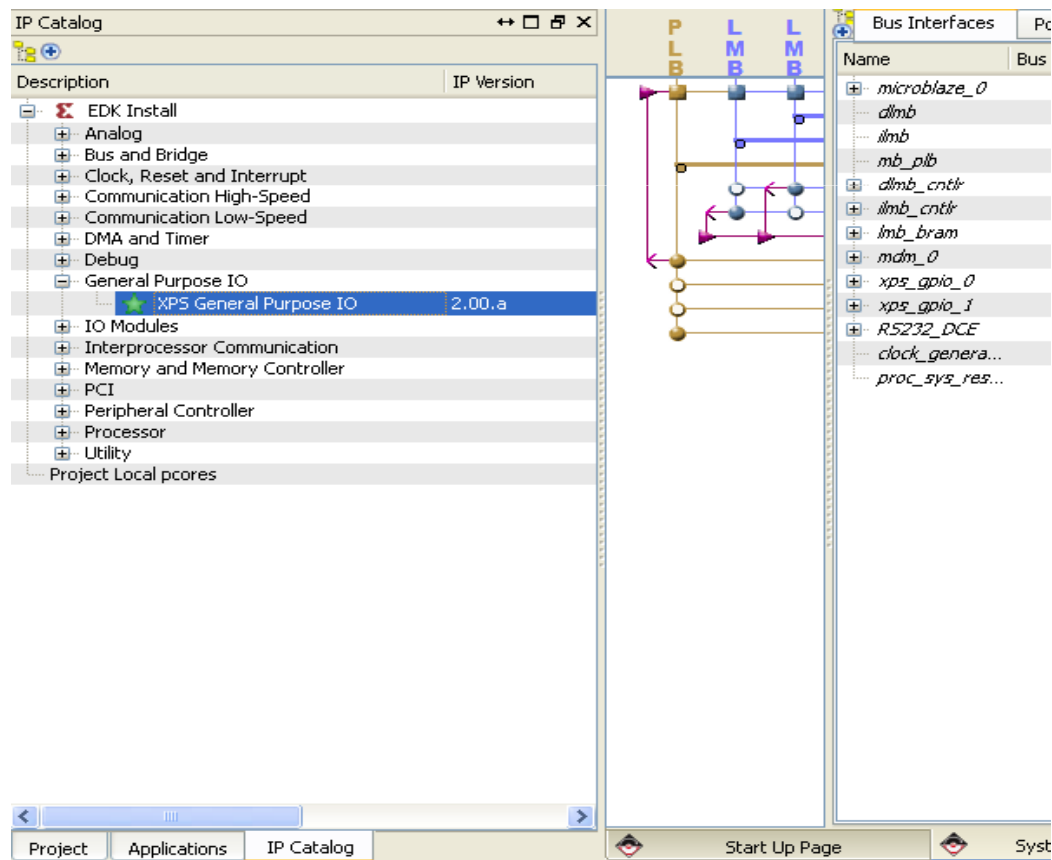
The screenshot displays the Xilinx Platform Studio (XPS) interface. The 'IP Catalog' window on the left lists various IP cores, including XPS IIC, PS2, SPI, UART, DMA, and MicroBlaze. The 'System Assembly View' window in the center shows a block diagram with components like PLB, LMB, and MicroBlaze. The 'Bus Interfaces' table on the right lists the following components:

Name	Bus Name	IP Type	IP Version
microblaze_0		microblaze	7.20.d
dlimb		lmb_v10	1.00.a
lmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.04.a
dlimb_cntr		lmb_bram_if...	2.10.b
lmb_cntr		lmb_bram_if...	2.10.b
DDR_SDRAM		mpmc	5.04.a
FLASH		xps_mch_emc	3.01.a
lmb_bram		bram_block	1.00.a
mdm_0		mdm	1.00.g
Ethernet_MAC		xps_etherne...	3.01.a
Buttons_4Bit		xps_gpio	2.00.a
DIP_Switche...		xps_gpio	2.00.a
LEDs_8Bit		xps_gpio	2.00.a
RS232_DCE		xps_uartlite	1.01.a
RS232_DTE		xps_uartlite	1.01.a
dock_genera...		dock_gener...	3.02.a
proc_sys_res...		proc_sys_re...	2.00.a

Red circles highlight the 'Hardware' menu, the 'IP Catalog' tab, and the 'System Assembly View' tab. A red arrow points to the 'Panel de conectividad' (Connectivity Panel) in the center.

HW DEL SISTEMA EMPOTRADO: XPS (XILINX PLATFORM STUDIO)

- Añadiendo un IP al sistema
 - Pestaña *IP Catalog*
- Modificar la conexión de los buses



HW DEL SISTEMA EMPOTRADO: XPS (XILINX PLATFORM STUDIO)

- Modificar las direcciones

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)
microblaze_0's Address Map					
dmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB
xps_gpio_1	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB
xps_gpio_0	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB
RS232_DCE	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB

- Modificar periféricos

The screenshot shows the XPS configuration environment. On the left, the project tree lists components like `xps_gpio_0`, `xps_gpio_1`, `RS232_DCE`, `clock_gen`, and `proc_sys_0`. A context menu is open over `xps_gpio_0`, with the 'Configure IP ...' option highlighted. A red arrow points from this menu to the configuration window for the selected IP. The configuration window has tabs for 'User', 'System', and 'Buses'. The 'Buses' tab is active, showing configuration for 'Channel 1' and 'Channel 2'. The 'Channel 1' configuration includes:

- GPIO Data Channel Width: 4
- Channel 1 Data Out Default Value: 0x00000000
- Channel 1 Tri-state Default Value: 0xffffffff
- Channel 1 is Input Only: TRUE

HW DEL SISTEMA EMPOTRADO: XPS (XILINX PLATFORM STUDIO)

- Conectar puertos

Name	Net	Direction
External Ports		
microblaze_0		
dmb		
ilmb		
mb_plb		
dmb_cntlr		
ilmb_cntlr		
lmb_bram		
mdm_0		
xps_gpio_0		
GPIO_IO_I	dip_GPIO_in	I
GPIO_IO_O	No Connection	O
GPIO_IO_T	No Connection	O
GPIO_IO	No Connection	IO
xps_gpio_1		
RS232_DCE		
clock_generator_0		
proc_sys_reset_0		

Name	Net	Direction	Range
External Ports			
fpga_0_RS232_DCE_RX_pin	fpga_0_RS232_DCE_R...	I	
fpga_0_RS232_DCE_TX_pin	fpga_0_RS232_DCE_T...	O	
fpga_0_clk_1_sys_clk_pin	dcm_clk_s	I	
fpga_0_rst_1_sys_rst_pin	sys_rst_s	I	
dip_GPIO_in_pin	dip_GPIO_in	I	[0:3]



HW DEL SISTEMA EMPOTRADO: XPS (XILINX PLATFORM STUDIO)

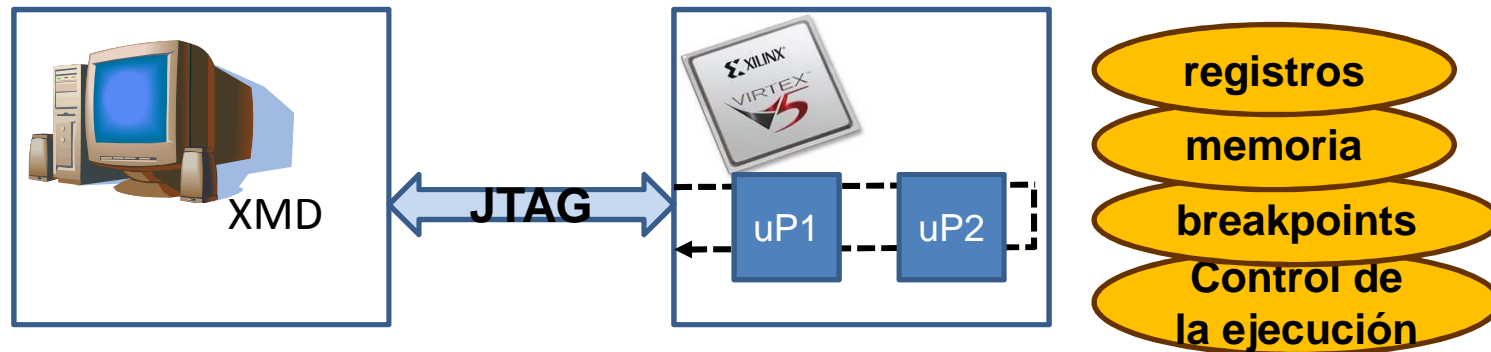
- Asignación de pines → .ucf

The screenshot shows the Xilinx Platform Studio (XPS) interface. On the left, the 'Project Files' tree is visible, with 'UCF File: data/system.ucf' selected. Below it, 'Project Options' are shown, including 'Device: xc3s500efg320-4', 'Implementation: XPS (Xflow)', and 'HDL: VHDL'. The main editor area displays the contents of the selected .ucf file, which contains pin constraints for an FPGA. The constraints are as follows:

```
1 Net fpga_0_RS232_DCE_RX_pin LOC=R7 | IOSTANDARD = LVCMOS33;
2 Net fpga_0_RS232_DCE_TX_pin LOC=M14 | IOSTANDARD = LVCMOS33;
3 Net fpga_0_clk_1_sys_clk_pin TNM_NET = sys_clk_pin;
4 TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 50000 kHz;
5 Net fpga_0_clk_1_sys_clk_pin LOC=c9 | IOSTANDARD = LVCMOS33;
6 Net fpga_0_rst_1_sys_rst_pin TIG;
7 Net fpga_0_rst_1_sys_rst_pin LOC=K17 | IOSTANDARD = LVCMOS33 | PULLDOWN;
8
9 ##### Module LEDs_8Bit constraints
10 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<0> LOC=F9 | IOSTANDARD = LVCMOS33;
11 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<1> LOC=E9 | IOSTANDARD = LVCMOS33;
12 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<2> LOC=D11 | IOSTANDARD = LVCMOS33;
13 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<3> LOC=C11 | IOSTANDARD = LVCMOS33;
14 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<4> LOC=F11 | IOSTANDARD = LVCMOS33;
15 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<5> LOC=E11 | IOSTANDARD = LVCMOS33;
16 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<6> LOC=E12 | IOSTANDARD = LVCMOS33;
17 Net fpga_0_LEDs_8Bit_GPIO_IO_O_pin<7> LOC=F12 | IOSTANDARD = LVCMOS33;
18
19 ##### Pin location constraints for the DIP switches
20 NET dip_GPIO_in_pin<0> LOC=L13 | IOSTANDARD = LVTTTL | PULLUP; # Switch0
21 NET dip_GPIO_in_pin<1> LOC=L14 | IOSTANDARD = LVTTTL | PULLUP; # Switch1
22 NET dip_GPIO_in_pin<2> LOC=H18 | IOSTANDARD = LVTTTL | PULLUP; # Switch2
23 Net dip_GPIO_in_pin<3> LOC=N17 | IOSTANDARD = LVTTTL | PULLUP; # Switch3
```

HW DEL SISTEMA EMPOTRADO: DEPURACIÓN

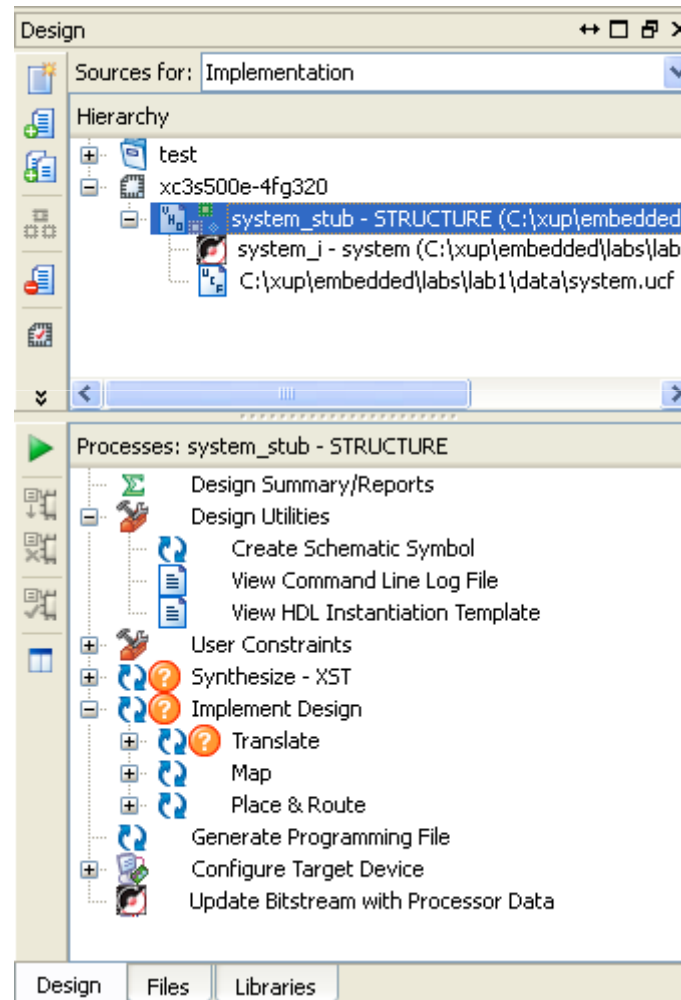
- ChipScope → HW dedicado
- Xilinx Microprocessor Debugger (XMD) → uP



- GNU Debugger (a través del XMD)

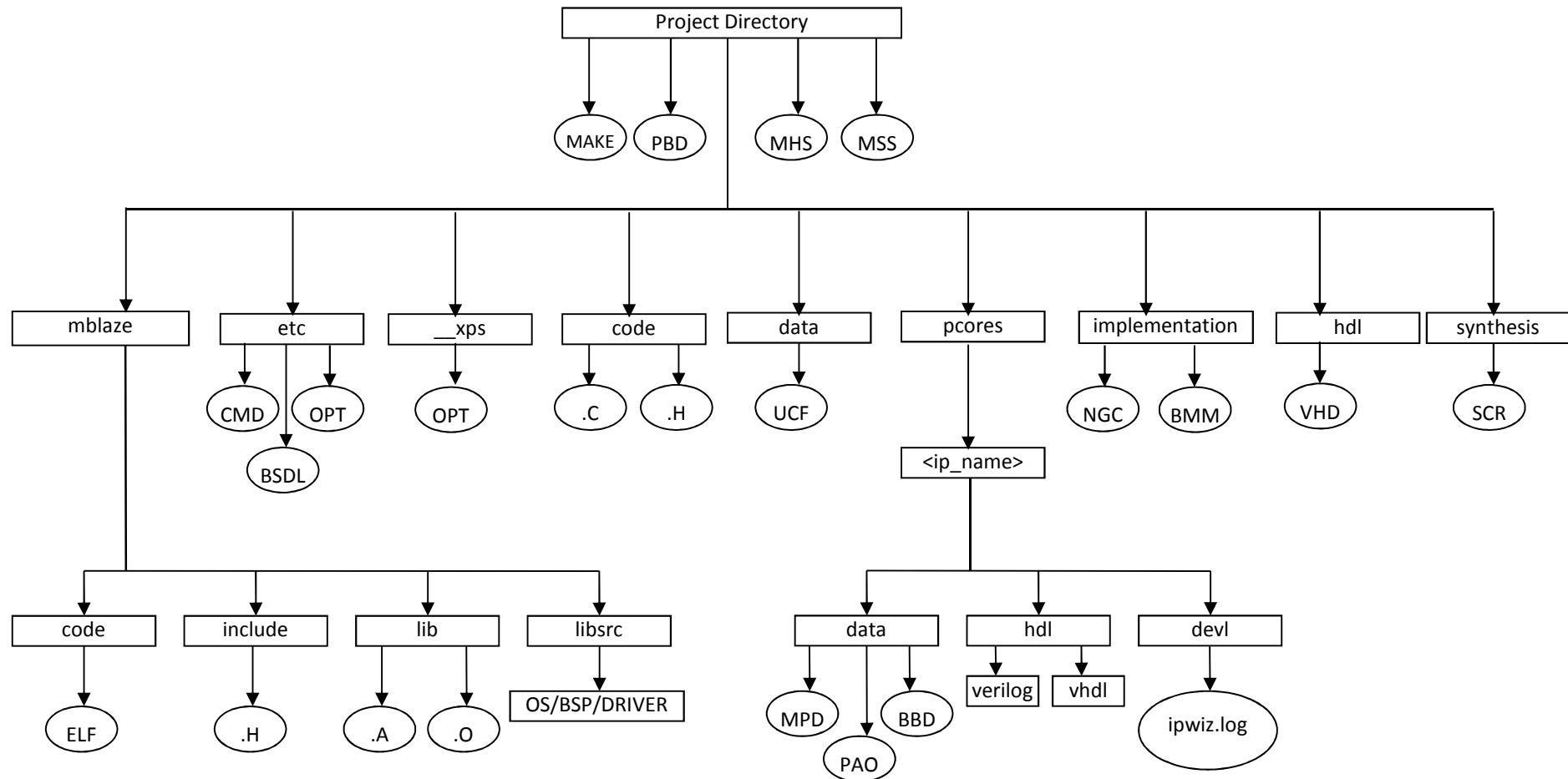


ISE ↔ XPS





DISEÑO DE UN SISTEMA EMPOTRADO: ESTRUCTURA DEL PROYECTO





FICHEROS GENERADOS

■ SW

- MDD (Microprocessor Driver Definition). Contiene las directivas necesarias para seleccionar los drivers de la aplicación.
- MSS (Microprocessor SW Specification). Especificación del SW del sistema empotrado.
- MLD (Microprocessor Library Definition). Contiene directivas para seleccionarlas librerías SW y el sistema operativo.

■ HW

- BDD (Black Box Definition)
- MHS (Microprocessor HW Specification). Define los componentes HW del sistema.
- MPD (Microprocessor Peripheral Definition). Define la interfaz de los periféricos.
- PAO (Peripheral Analyze Order). Contiene la lista de ficheros HDE necesarios para la síntesis y define el orden de compilación de los mismos.
- XDB (Xilinx Board Definition). Contiene la definición de las interfaces lógicas presentes en una placa determinada y cómo se conectan a la FPGA



BIBLIOGRAFÍA:

- “EDK Concepts, Tools, and Techniques. *Guide to Effective Embedded System Design*”
Xilinx → Manual del entorno de desarrollo
- “Platform Specification Format Reference Manual”, Xilinx → Formatos de los distintos ficheros y descripción de su contenido