

UNIVERSIDAD CARLOS III DE MADRID

# Tema 1. Jerarquía de Memoria

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Departamento de Ingeniería de Sistemas y Automática

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Universidad  
Carlos III de Madrid



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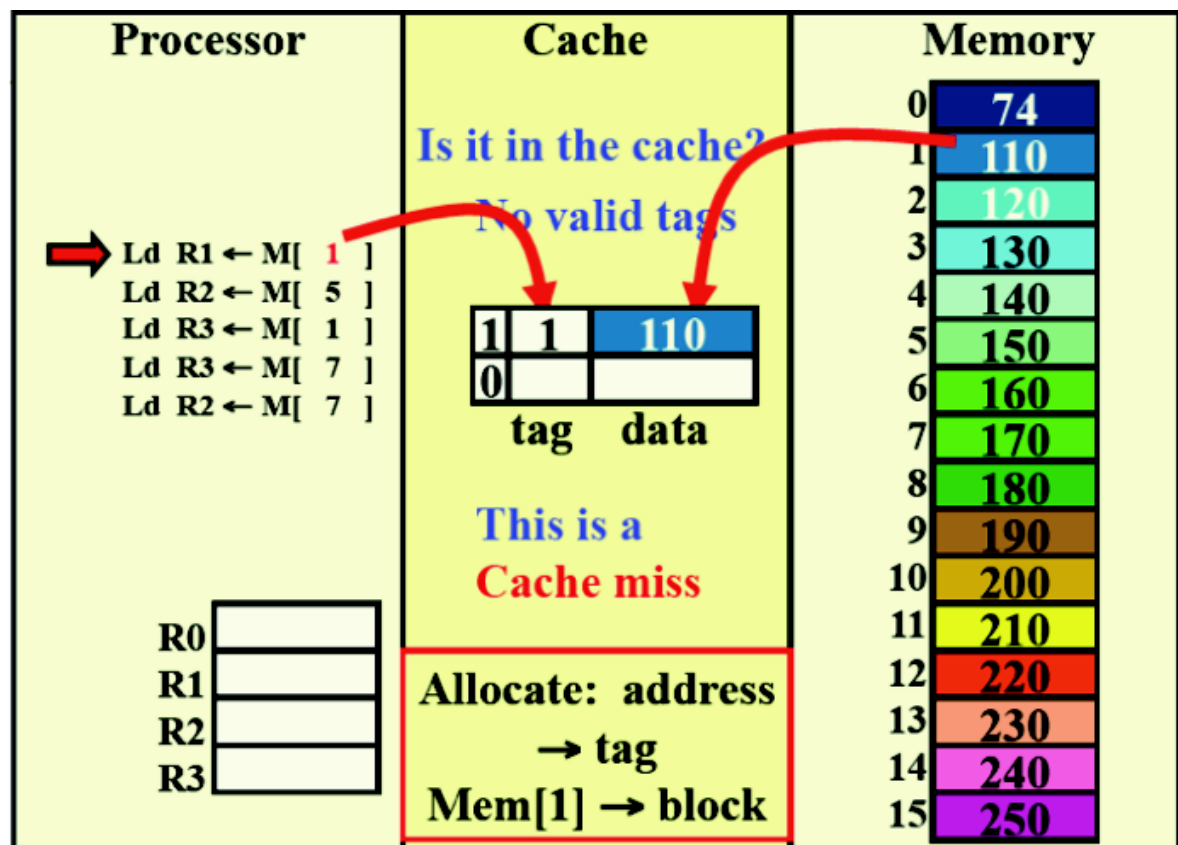
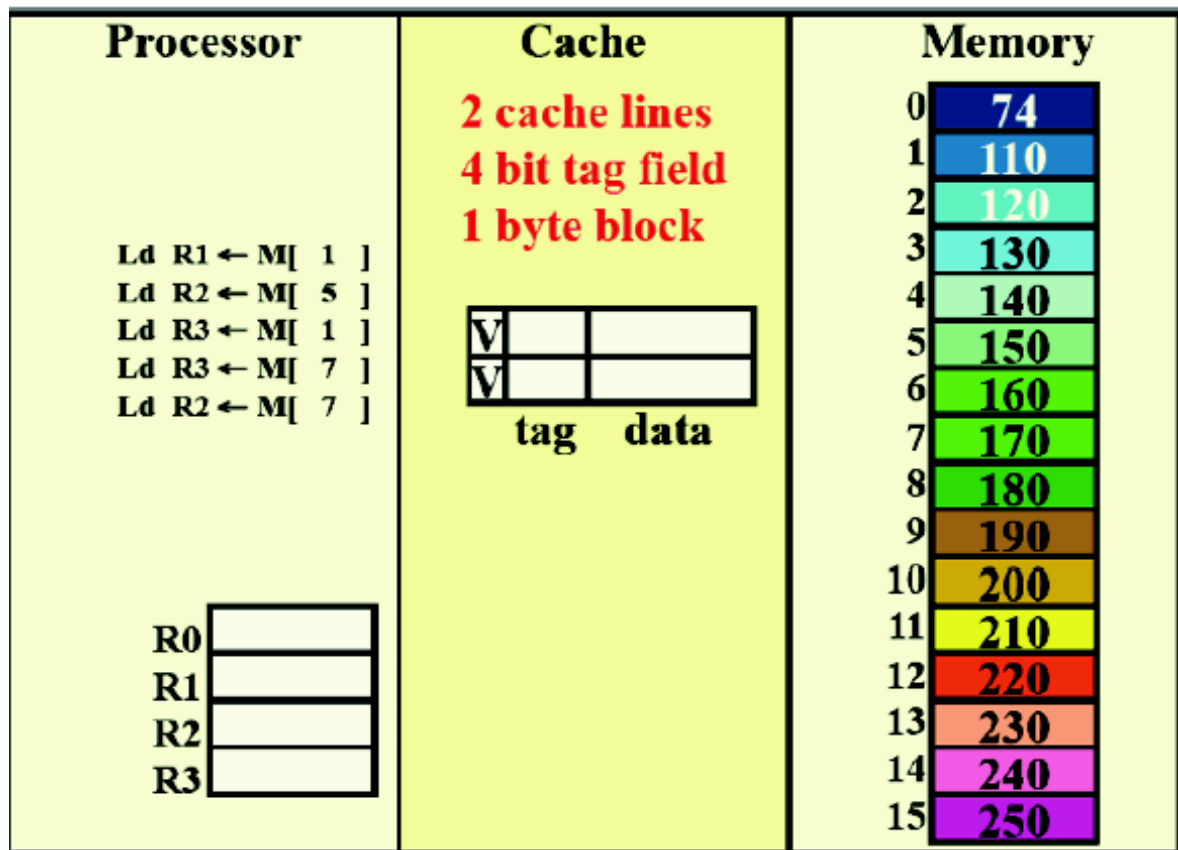
## Ejercicio 1

Sistema simple de memoria

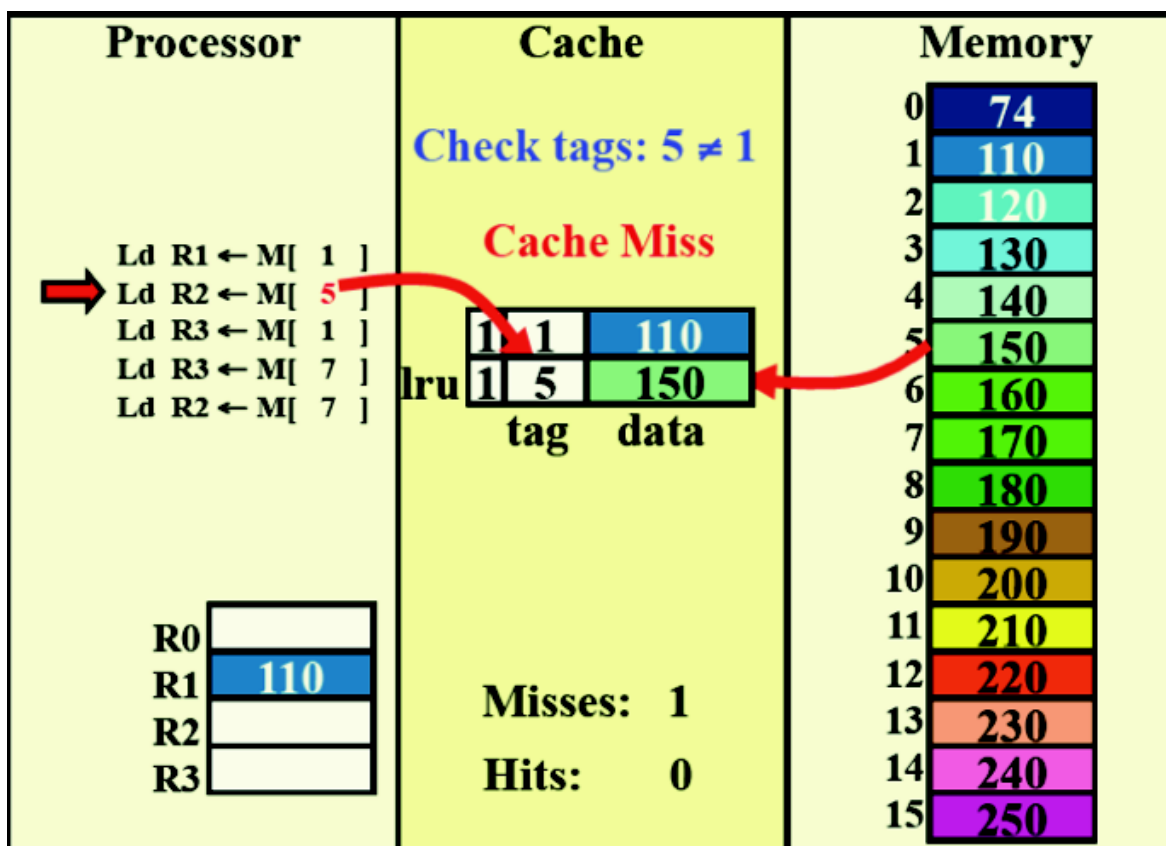
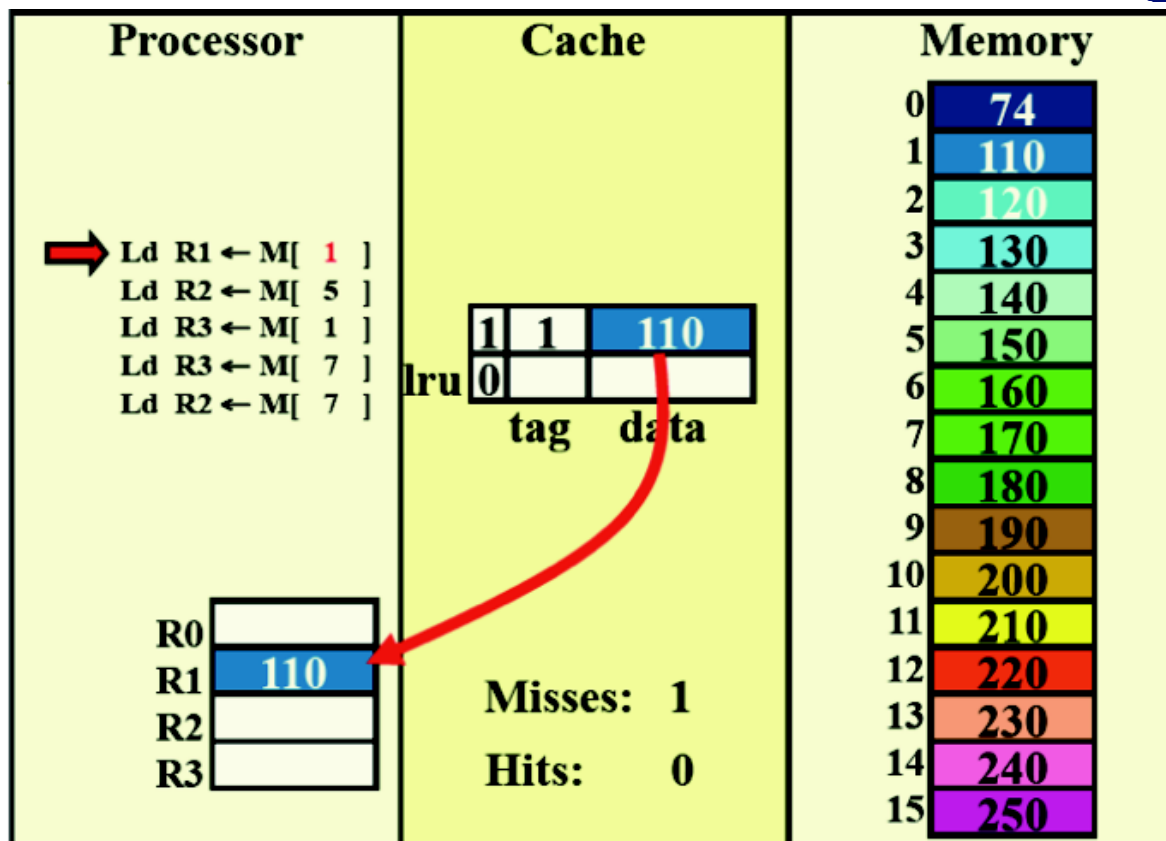
- Registros CPU.
- Caché asociativa de 2 líneas (entradas), con campo de etiqueta de 4 bits y campo de datos de 1 Byte, política de reemplazo LRU (Least Recently Used).
- Memoria física con palabra de memoria de 1 Byte.



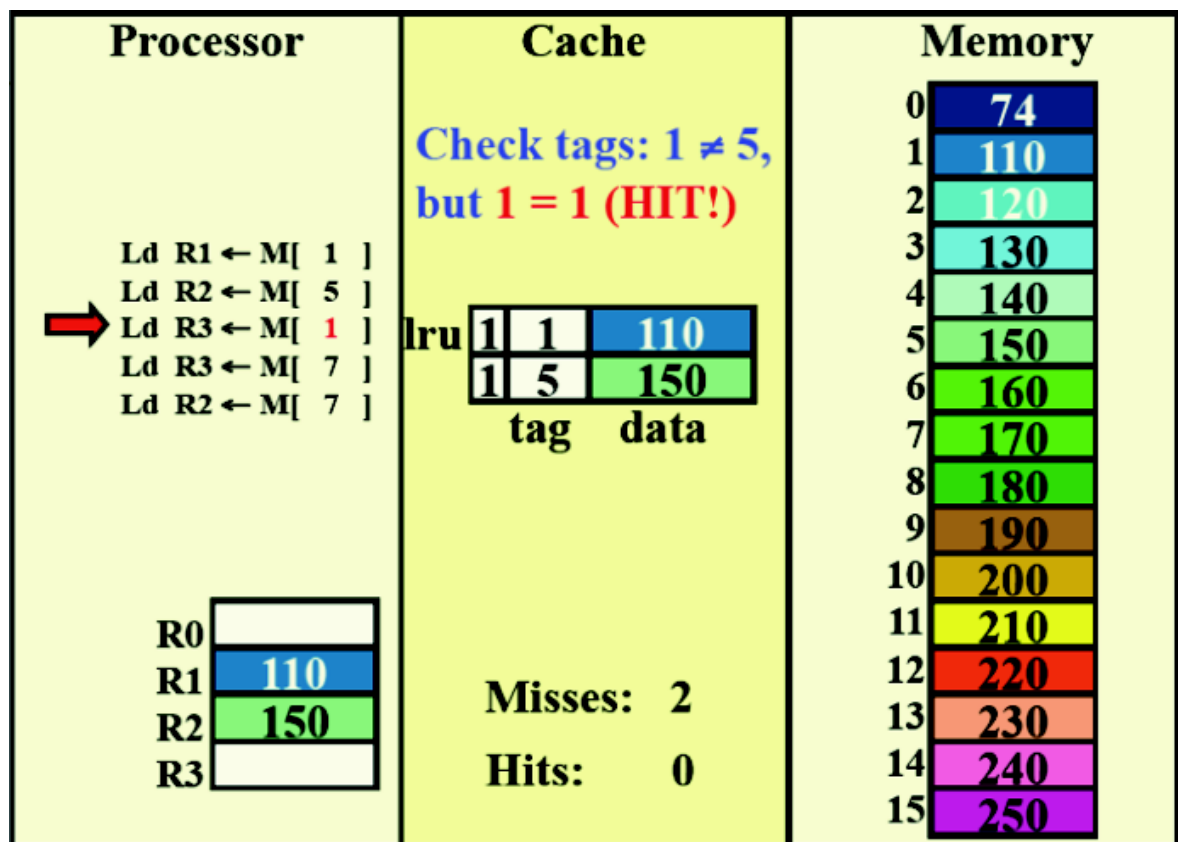
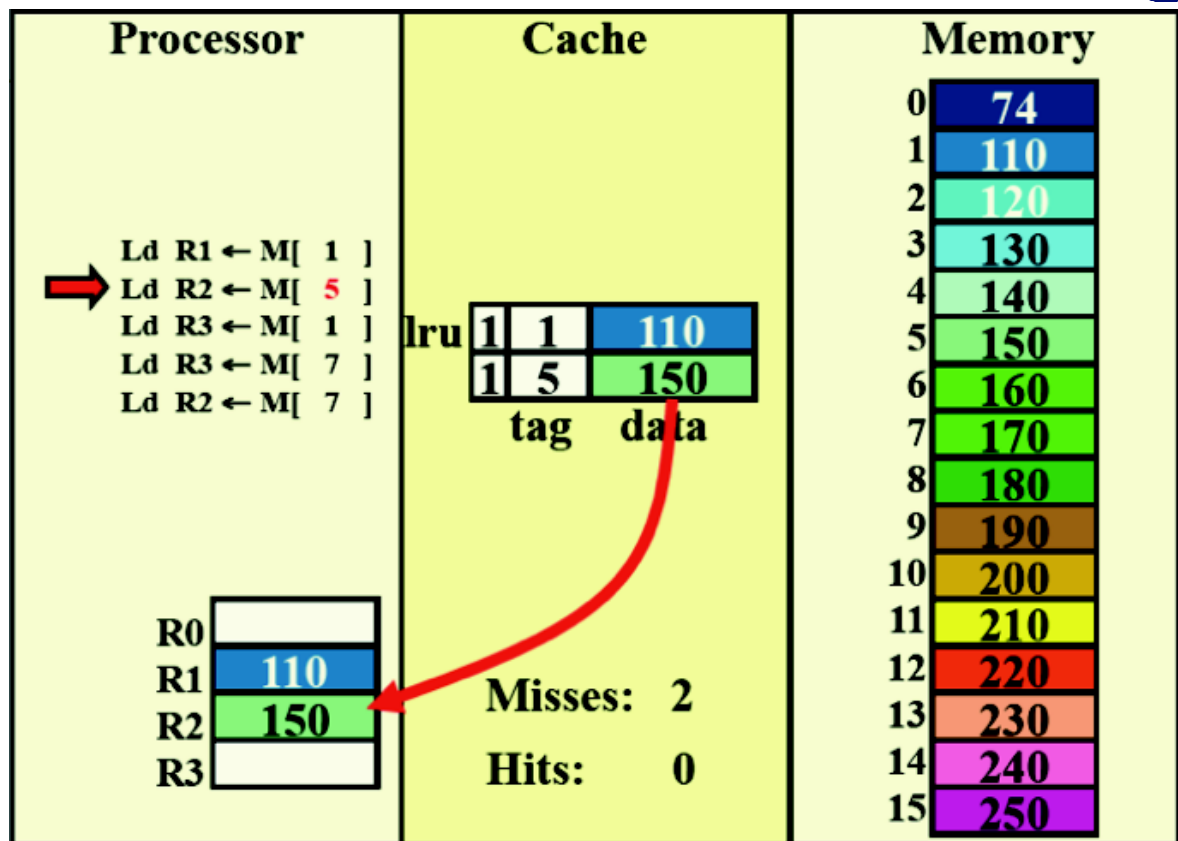
Solución



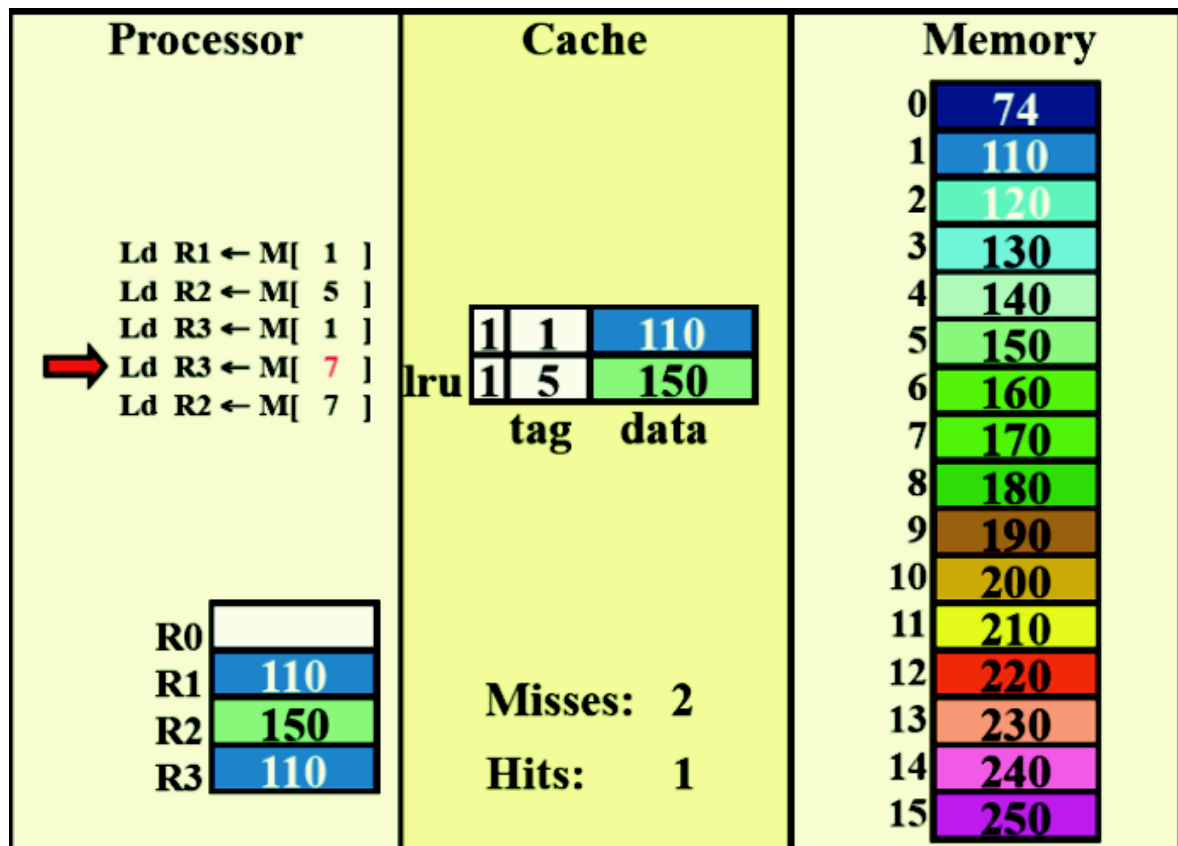
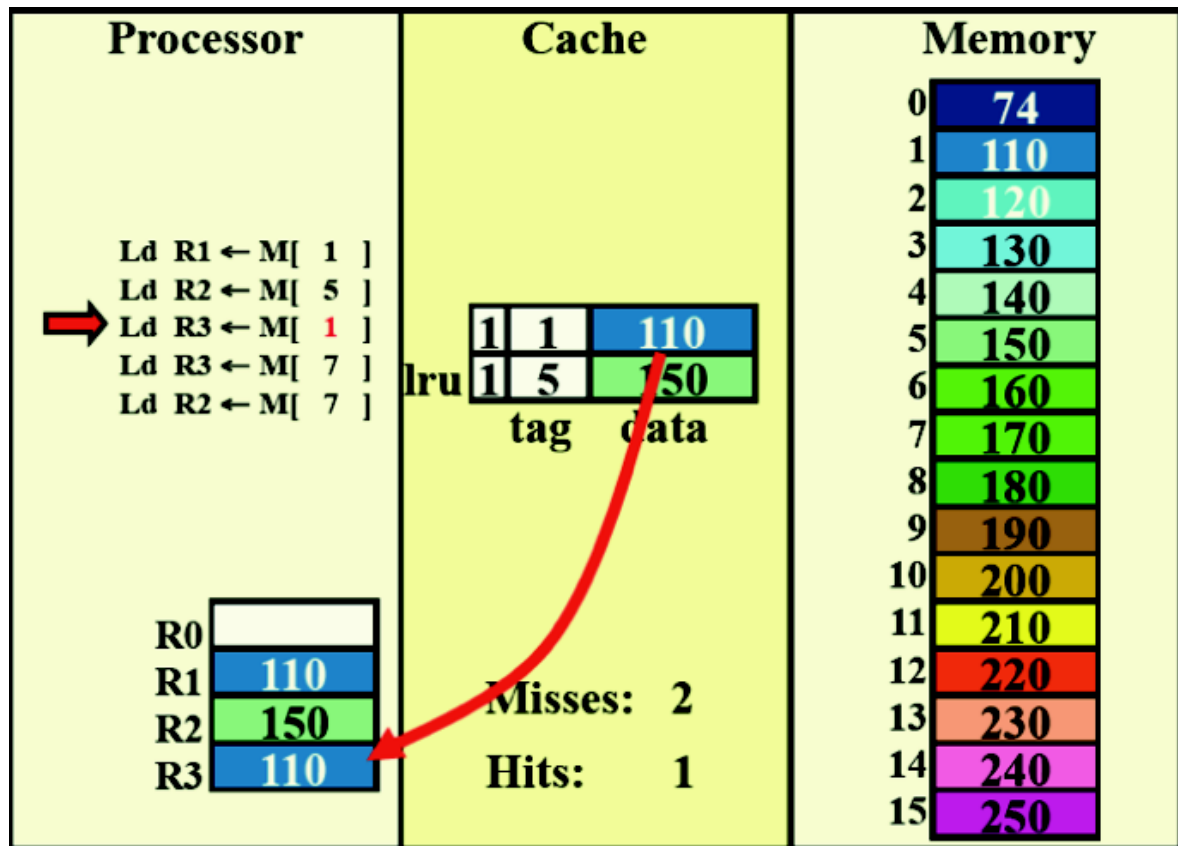




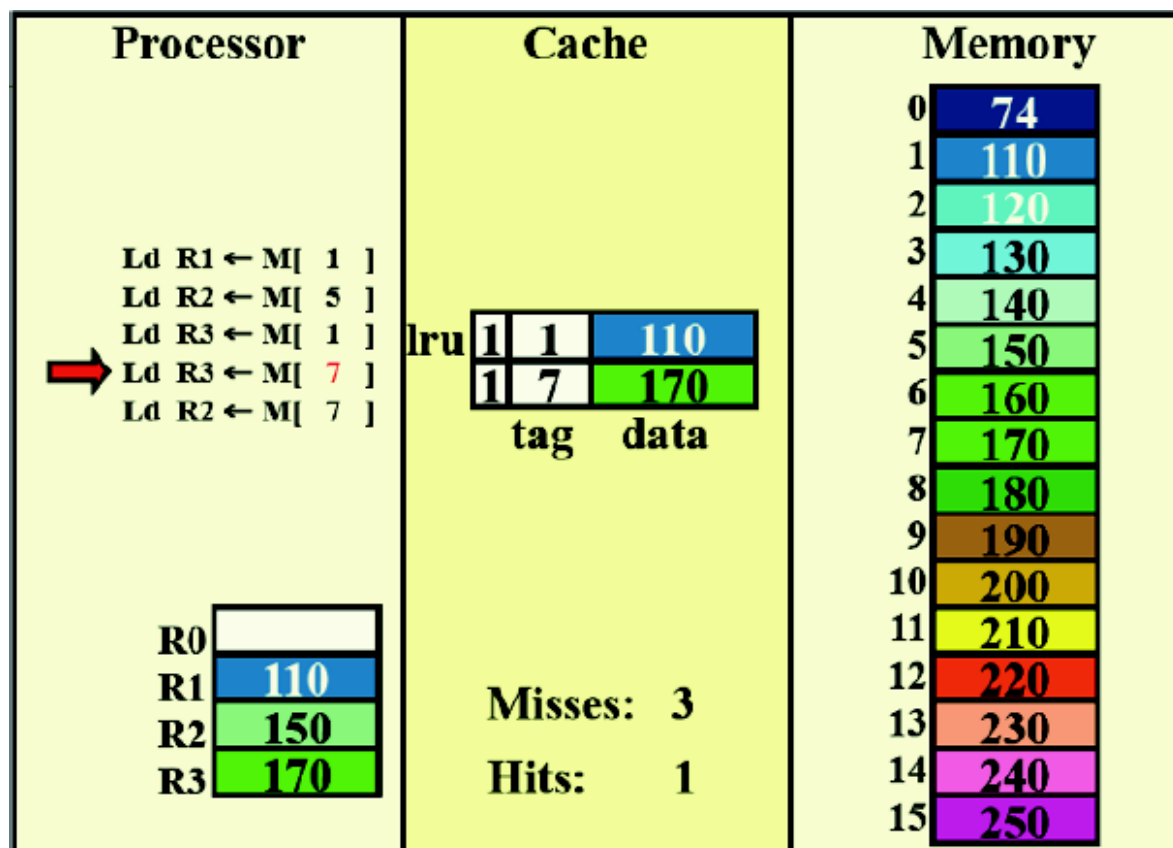
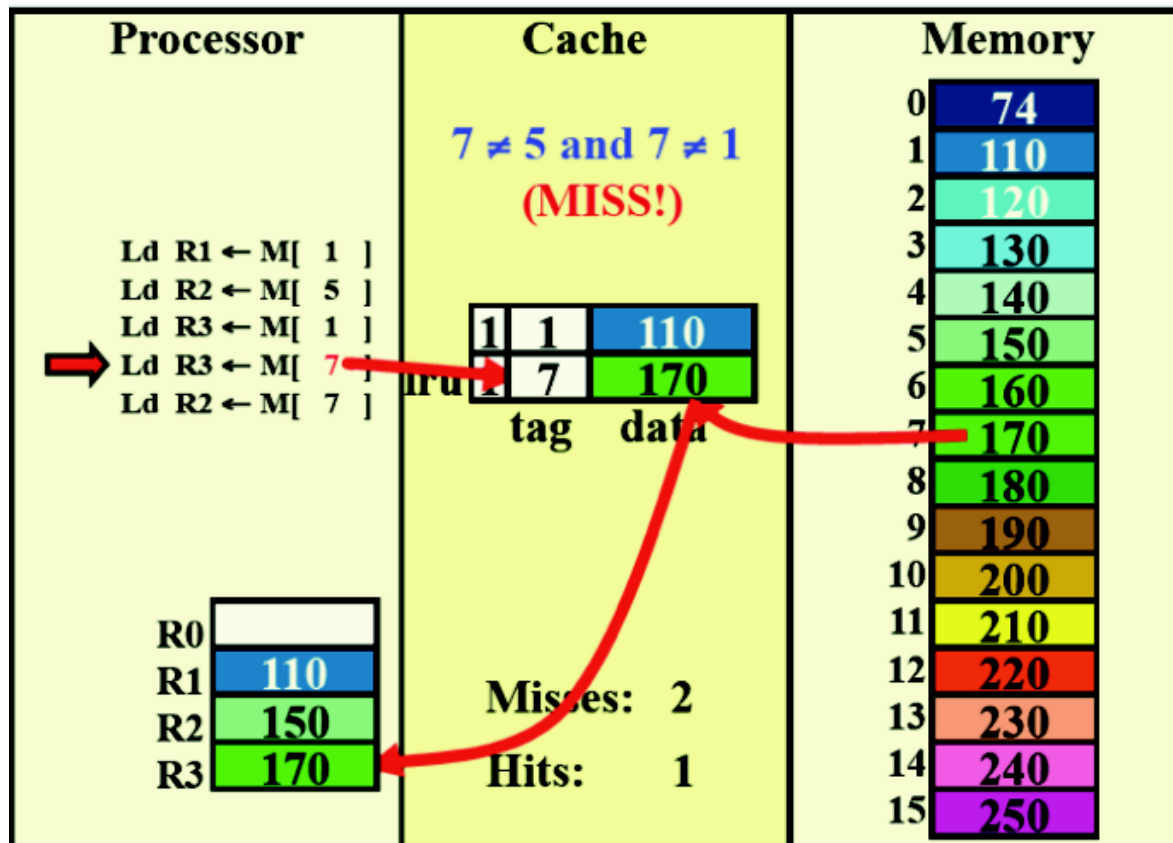




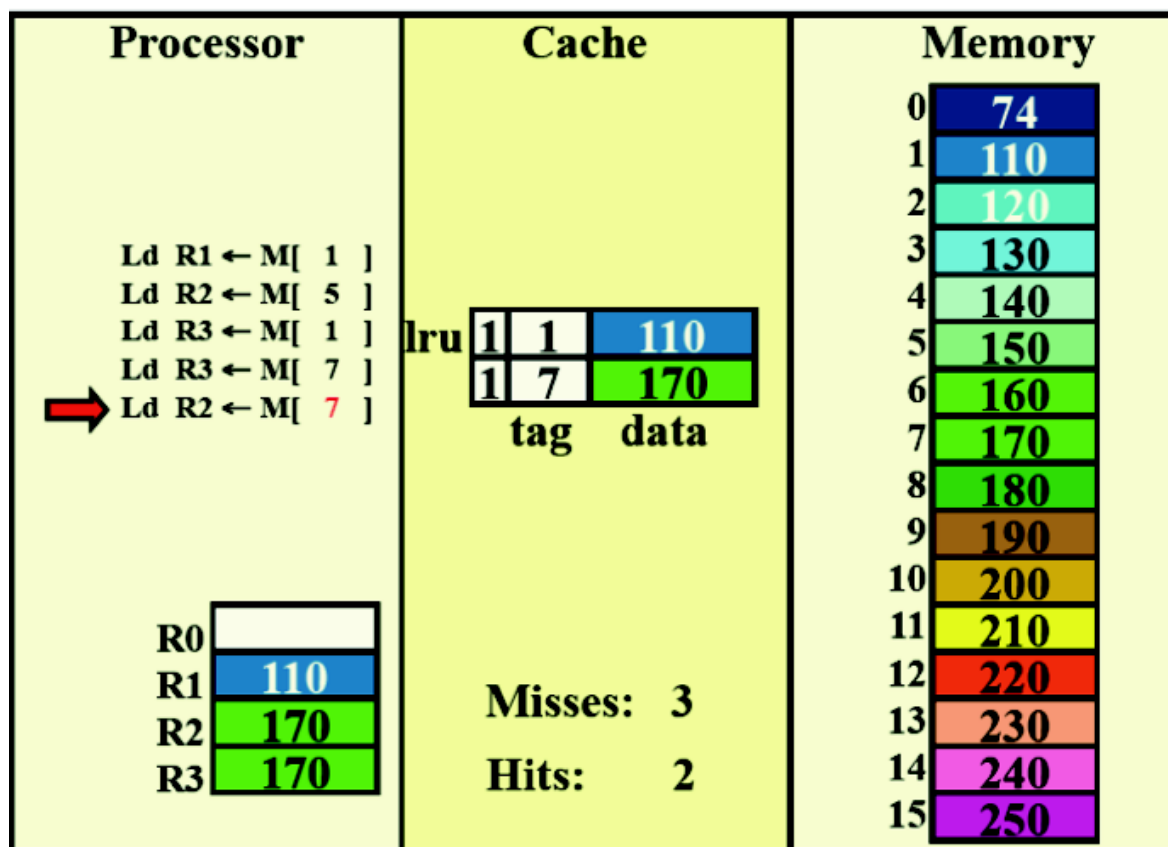
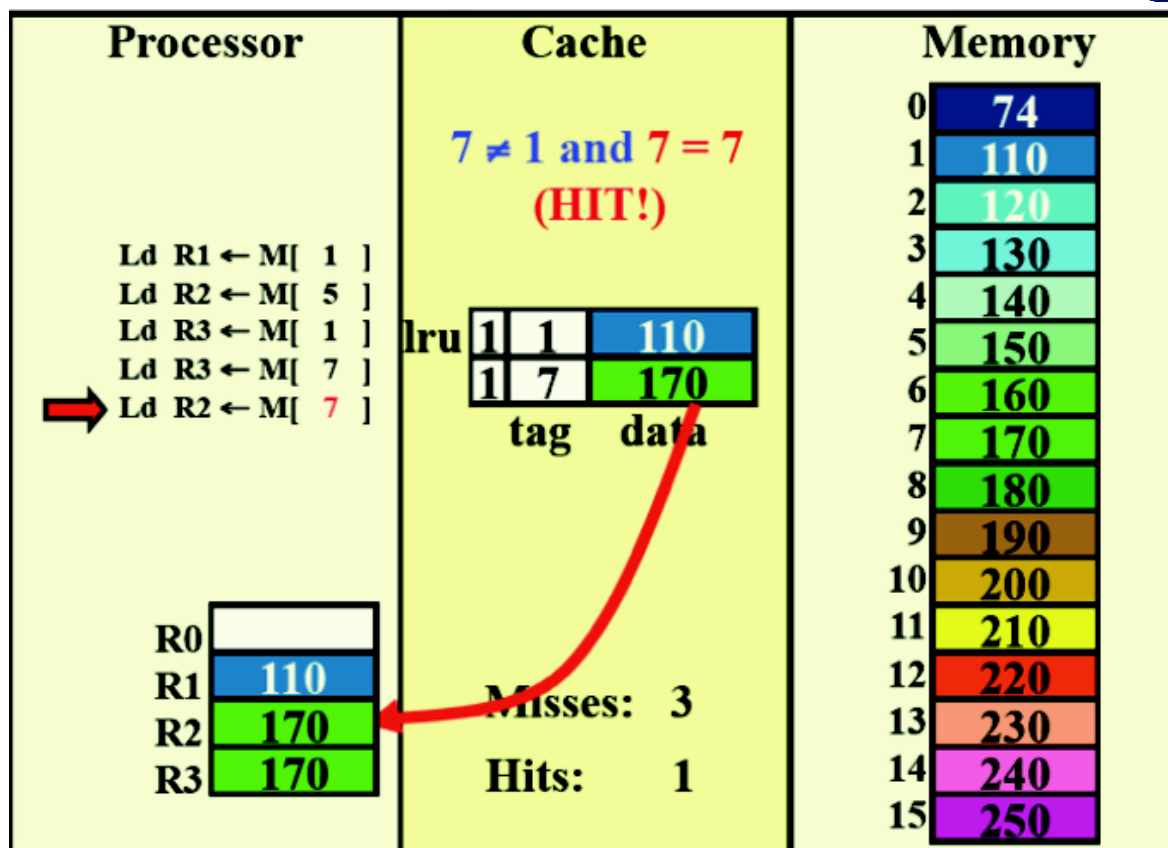
















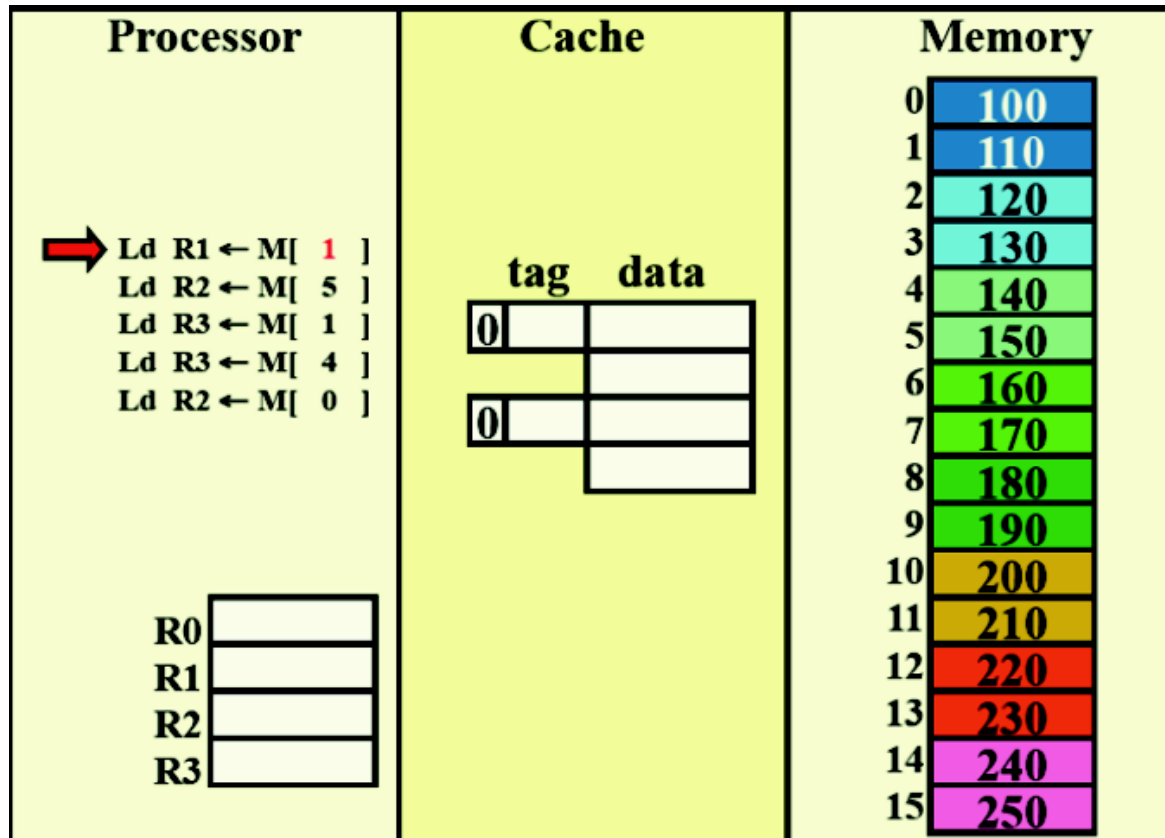
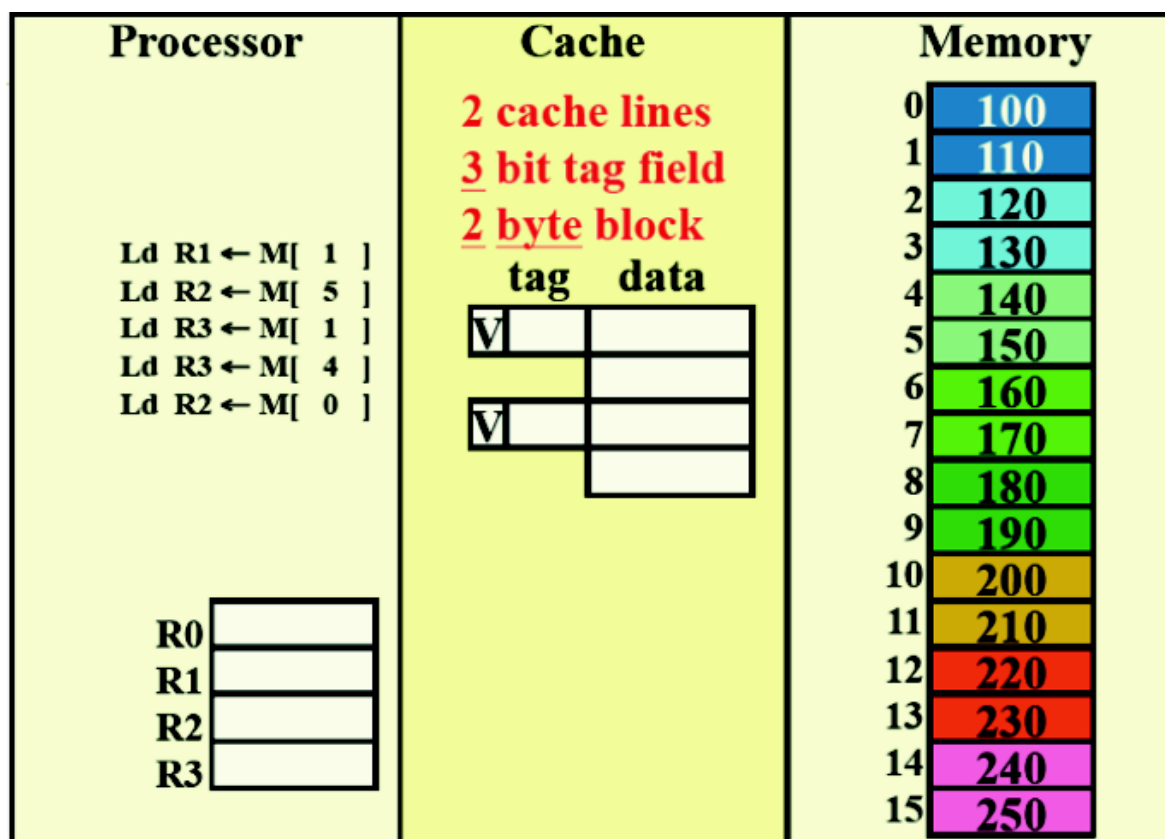
## Ejercicio 2

Aumento del tamaño de bloque

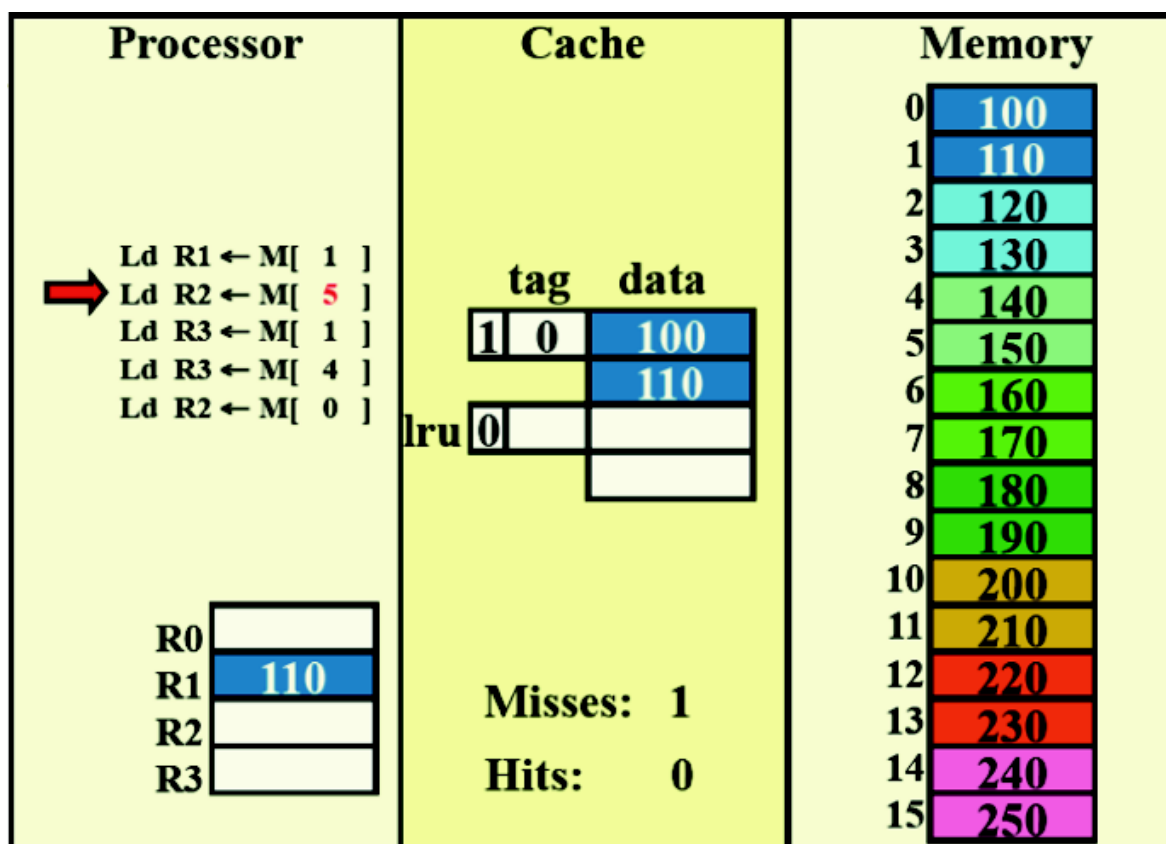
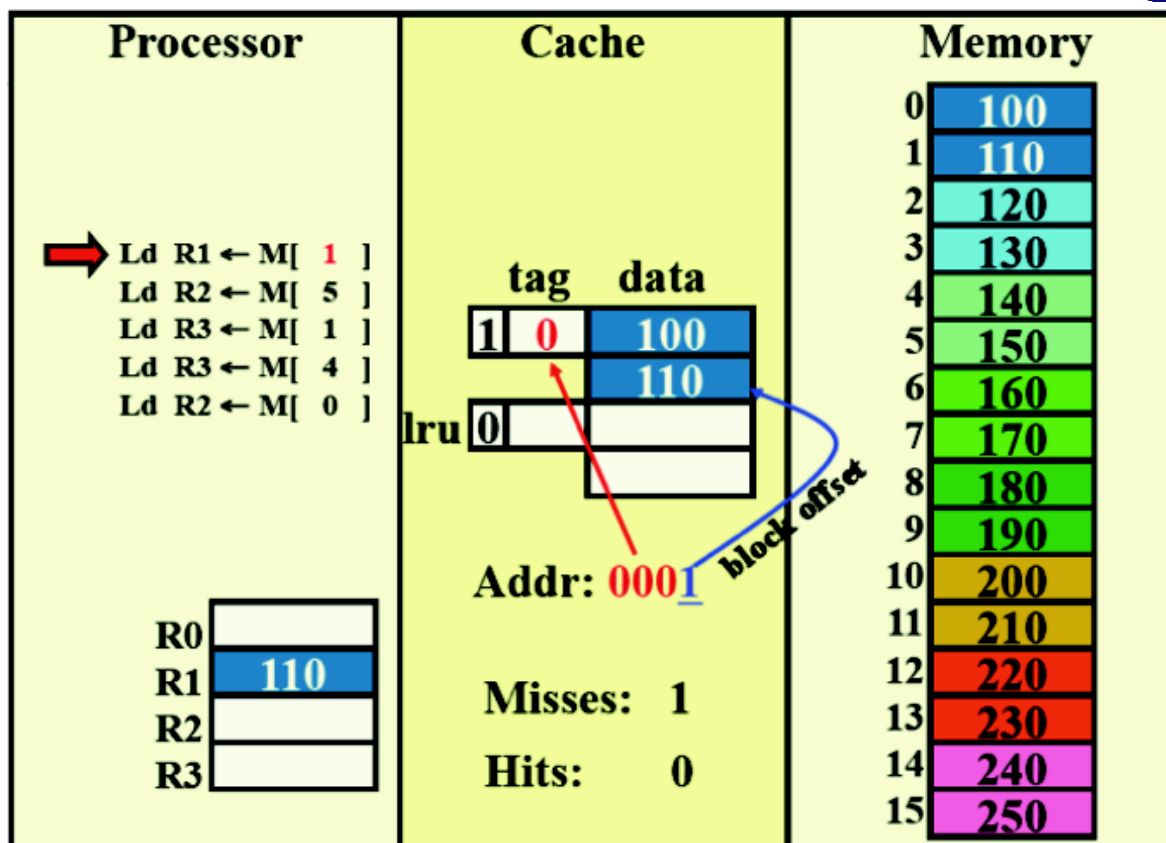
- Registros CPU.
- Caché asociativa de 2 líneas (entrada), con campo de etiqueta de 3 bits y campo de datos de 2 Bytes, política de reemplazo LRU (Least Recently Used).
- Memoria física con palabra de memoria de 1 Byte.



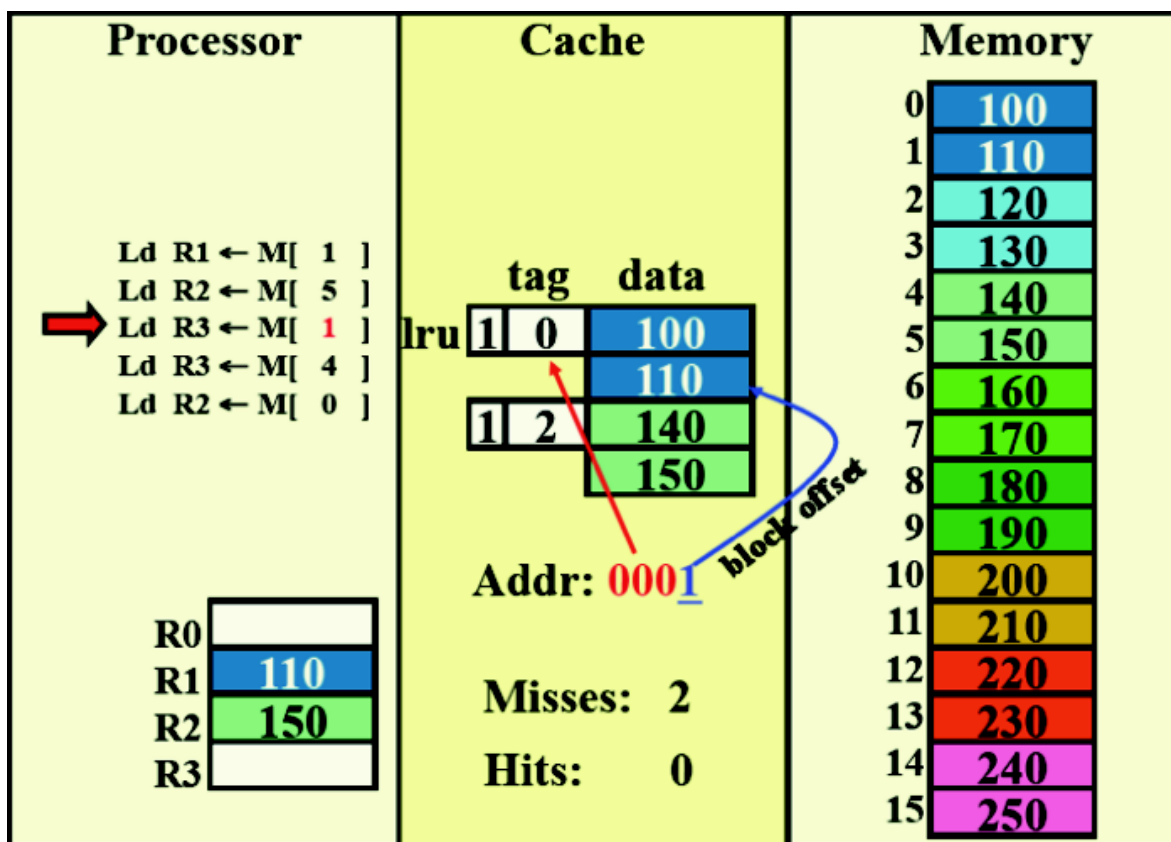
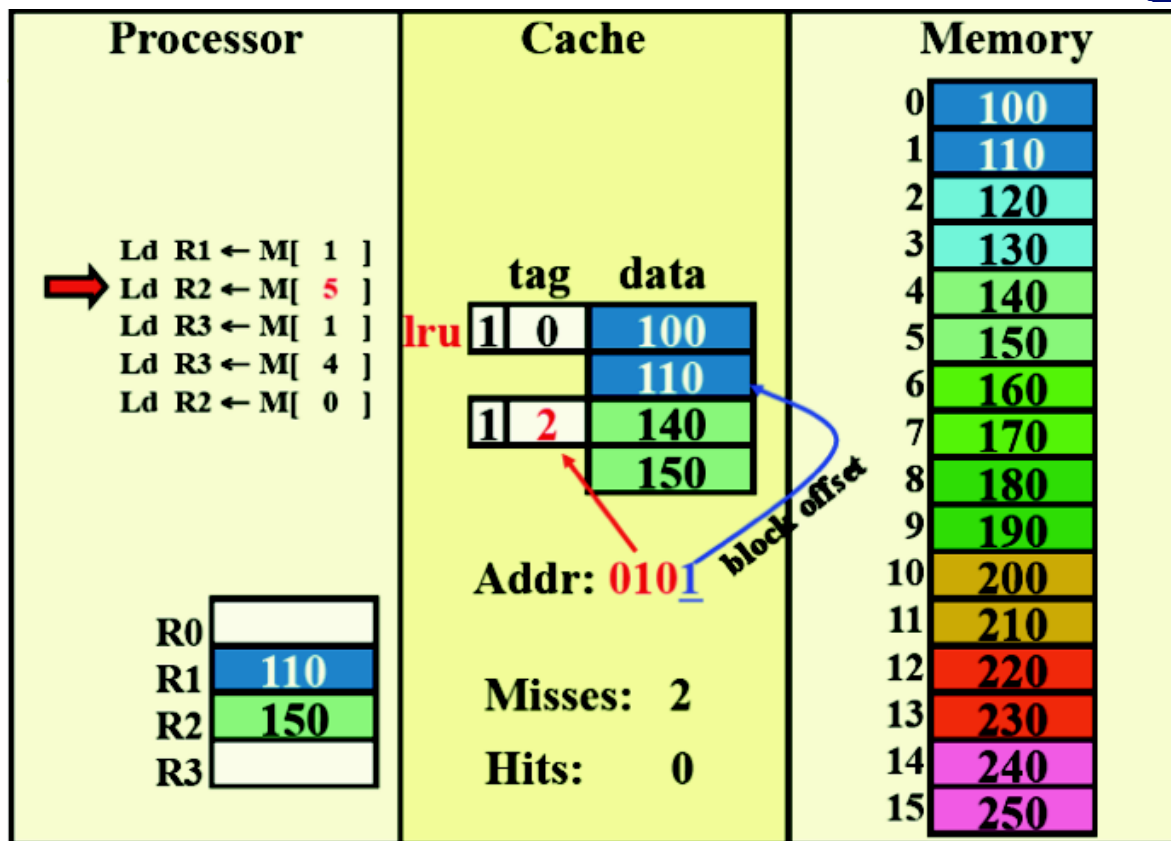
Solución



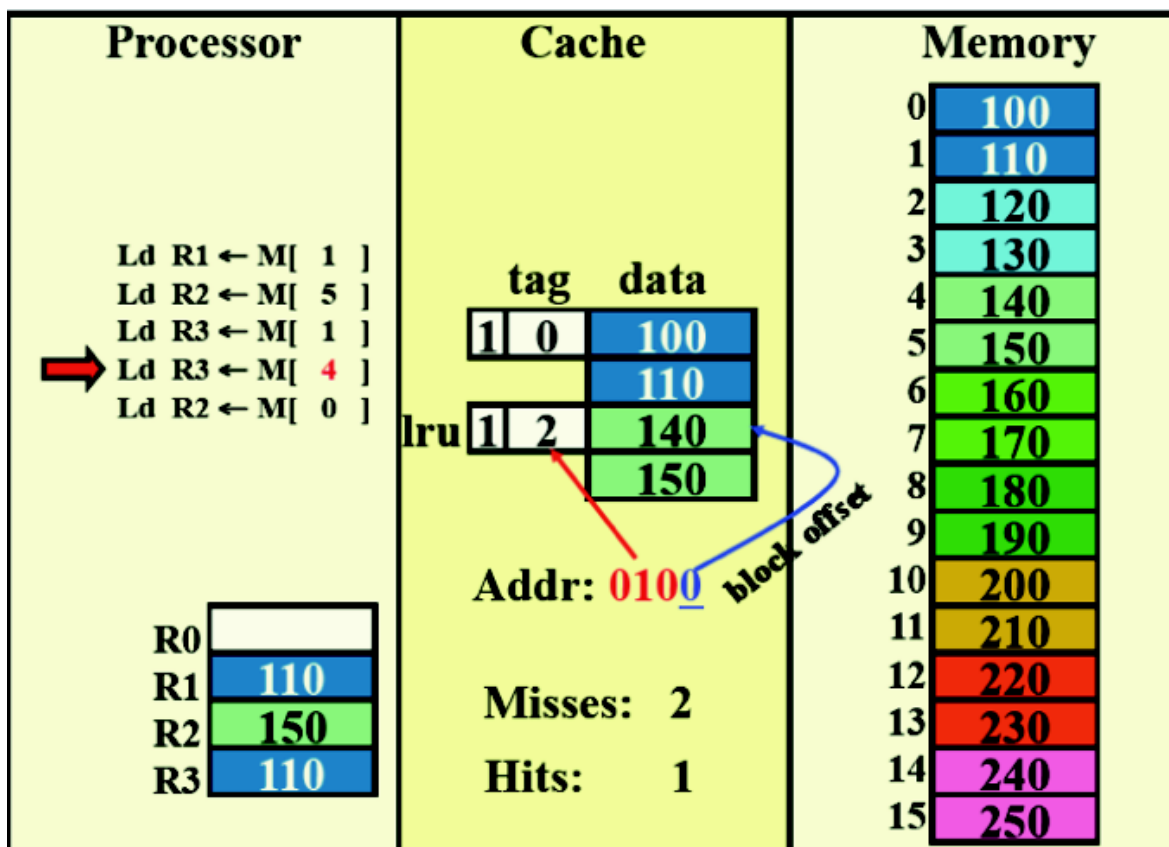
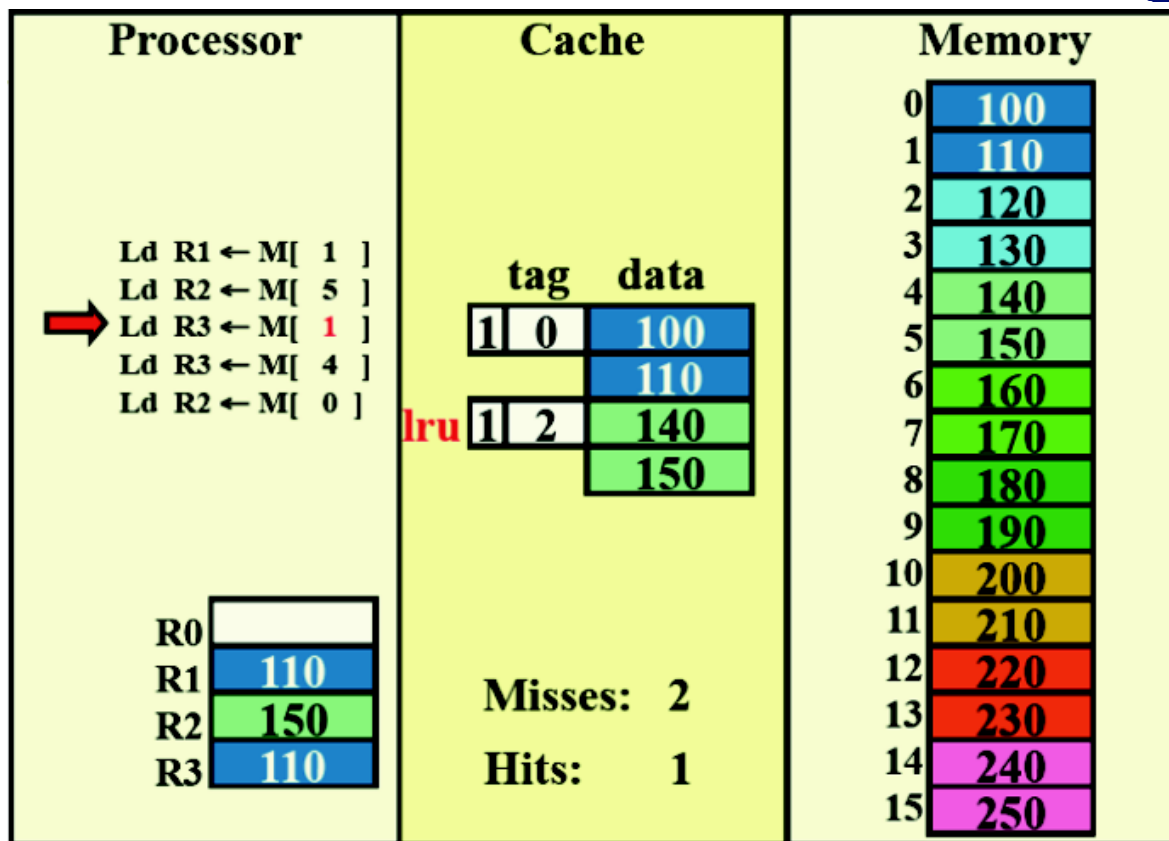




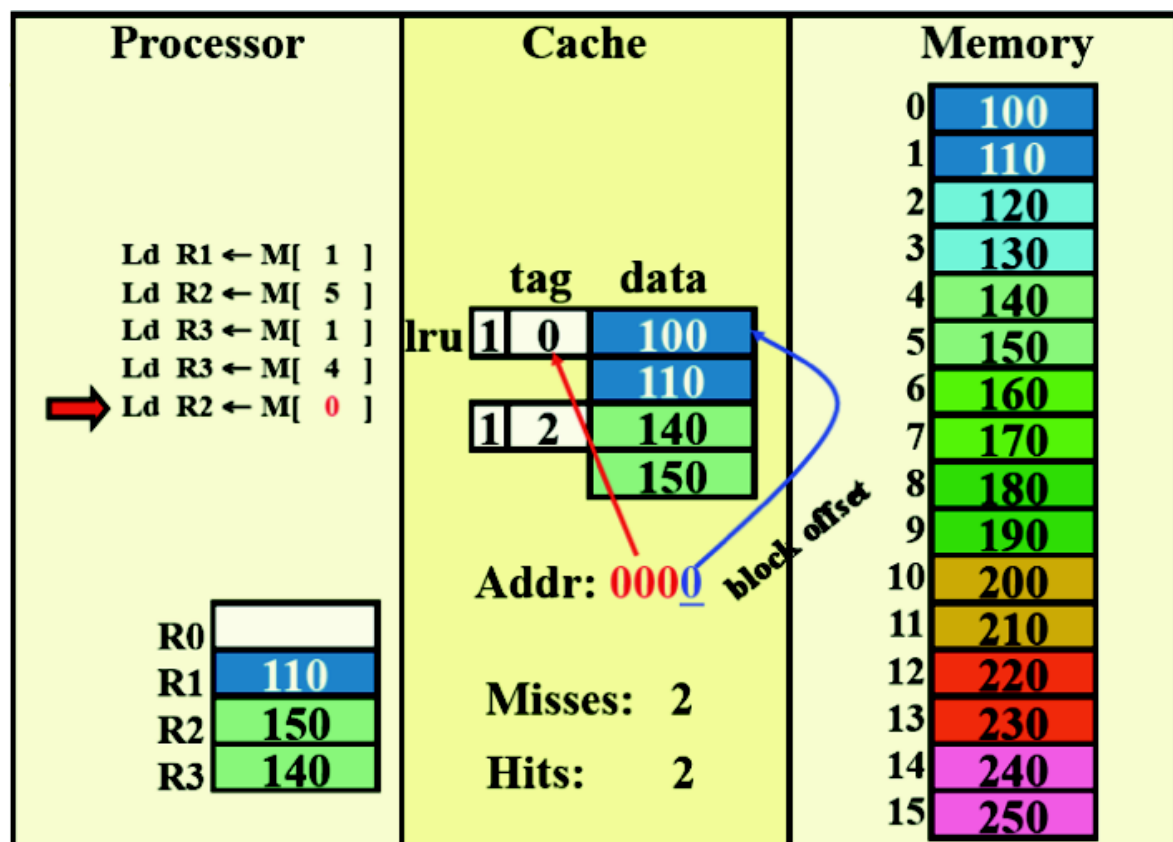
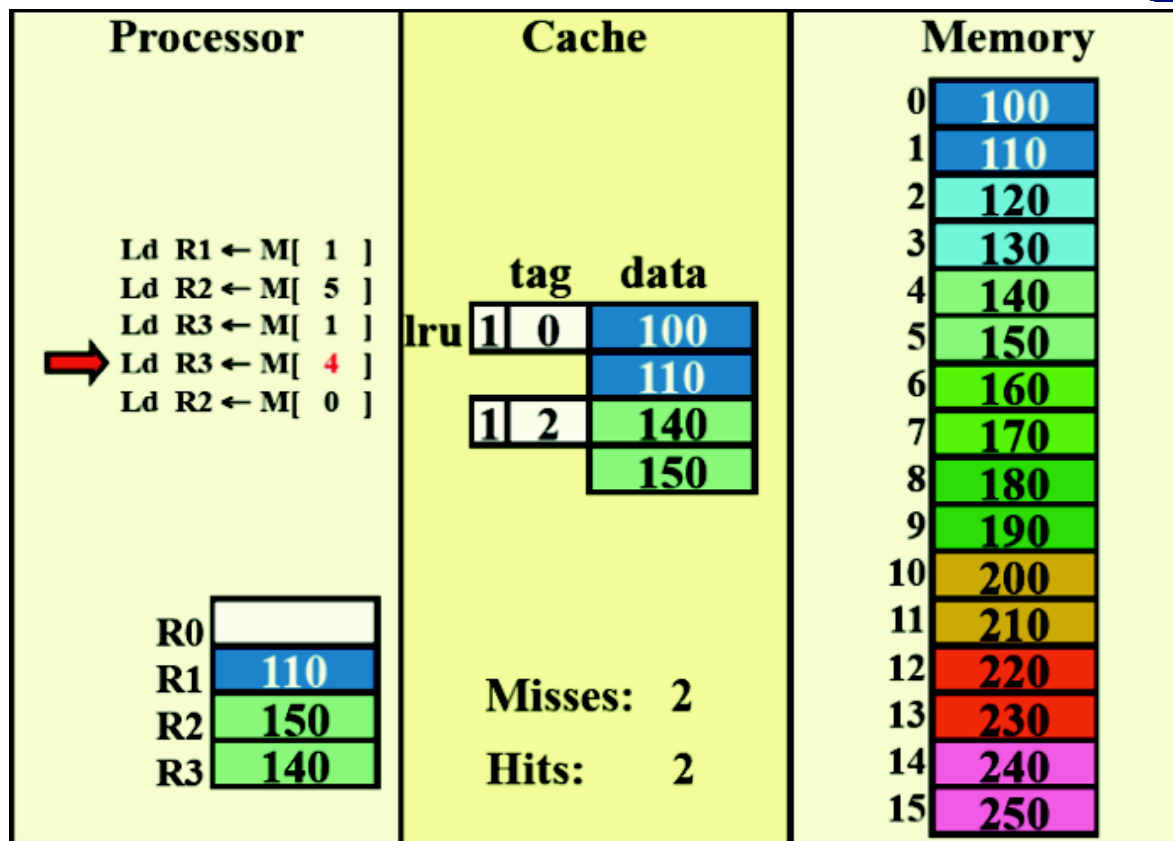




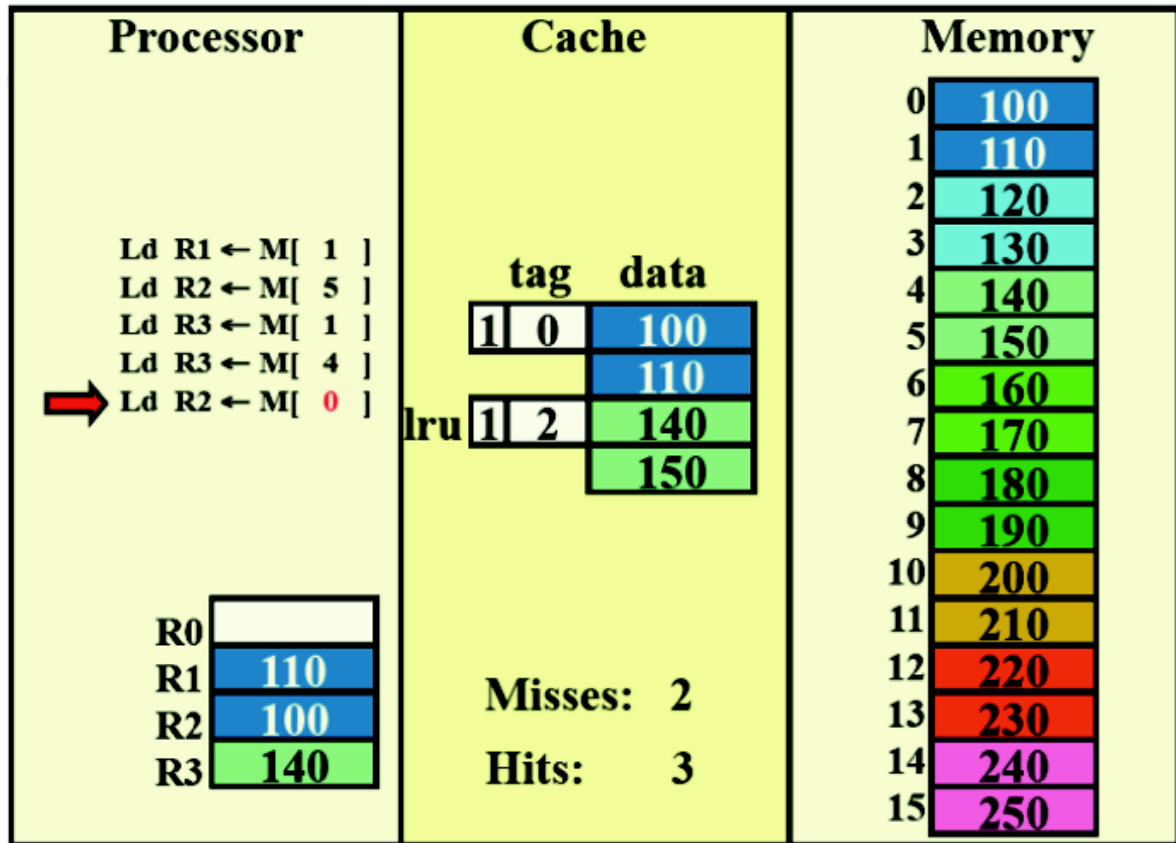














### Ejercicio 3

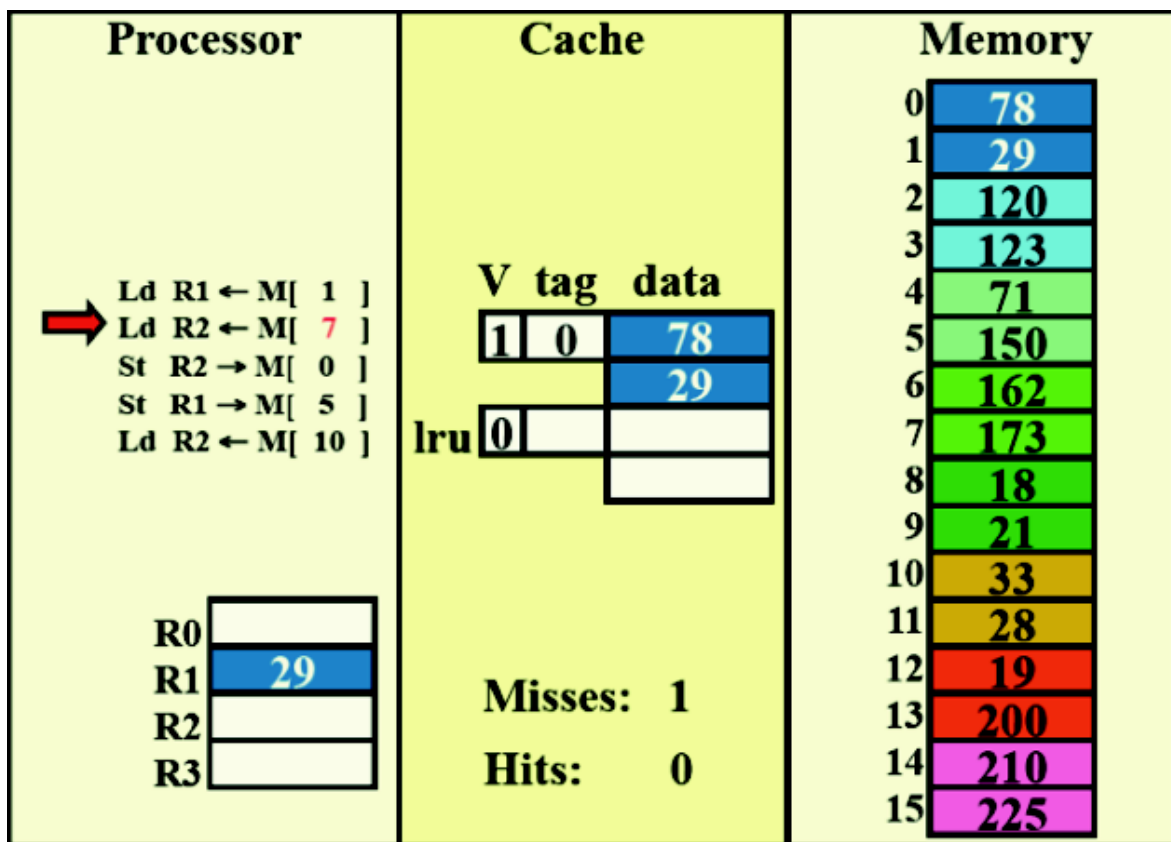
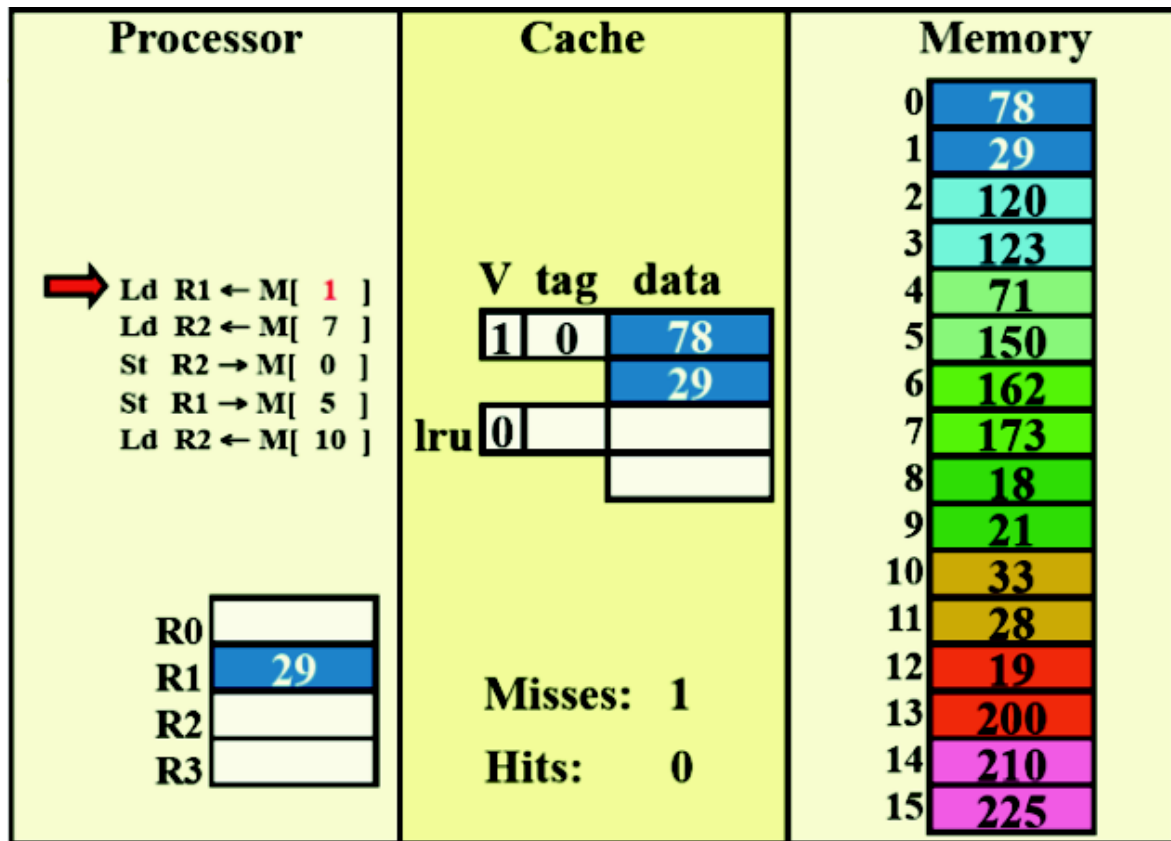
Escritura en memoria (write-through)

#### Solución

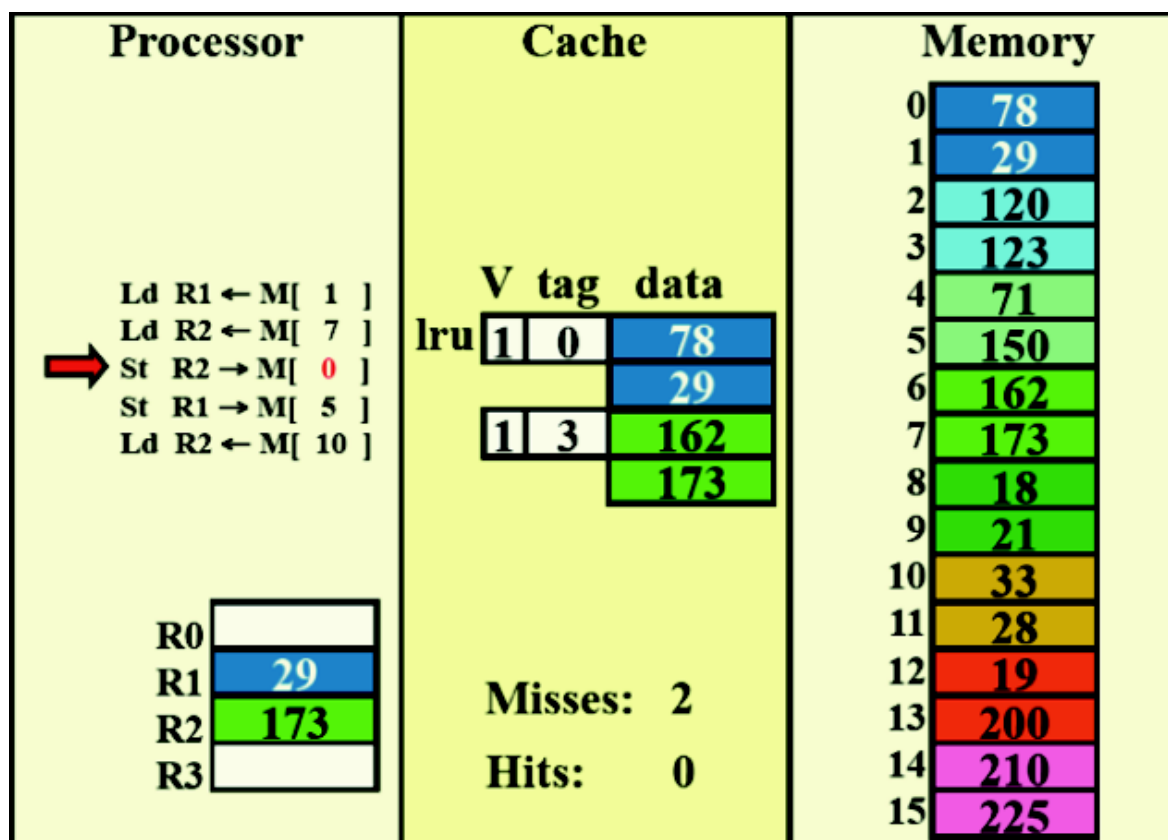
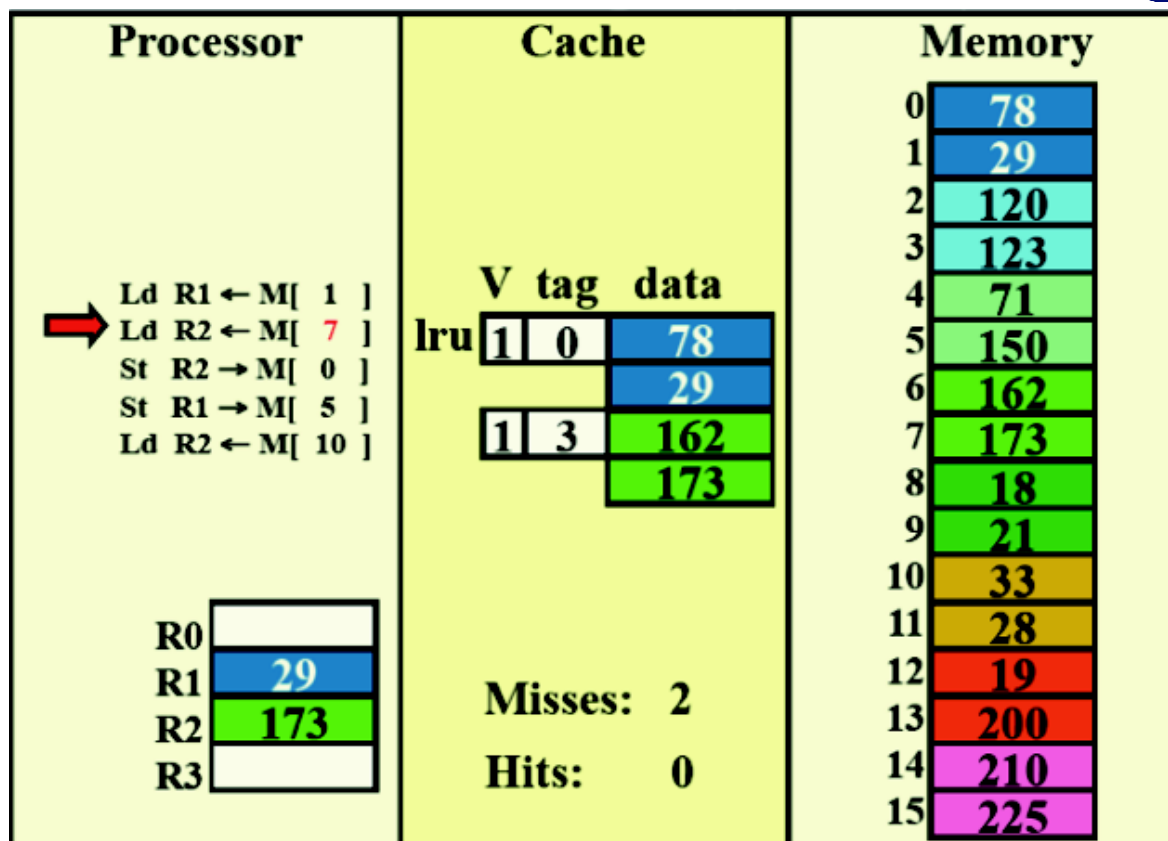
Processor	Cache	Memory
<p>Assume write-allocate policy</p> <p>Ld R1 ← M[ 1 ] Ld R2 ← M[ 7 ] St R2 → M[ 0 ] St R1 → M[ 5 ] Ld R2 ← M[ 10 ]</p> <p>R0 R1 R2 R3</p>	<p>V tag data</p> <p>0 0</p> <p>Misses: 0 Hits: 0</p>	<p>0 78 1 29 2 120 3 123 4 71 5 150 6 162 7 173 8 18 9 21 10 33 11 28 12 19 13 200 14 210 15 225</p>

Processor	Cache	Memory
<p>→ Ld R1 ← M[ 1 ] Ld R2 ← M[ 7 ] St R2 → M[ 0 ] St R1 → M[ 5 ] Ld R2 ← M[ 10 ]</p> <p>R0 R1 R2 R3</p>	<p>V tag data</p> <p>0 0</p> <p>Misses: 0 Hits: 0</p>	<p>0 78 1 29 2 120 3 123 4 71 5 150 6 162 7 173 8 18 9 21 10 33 11 28 12 19 13 200 14 210 15 225</p>

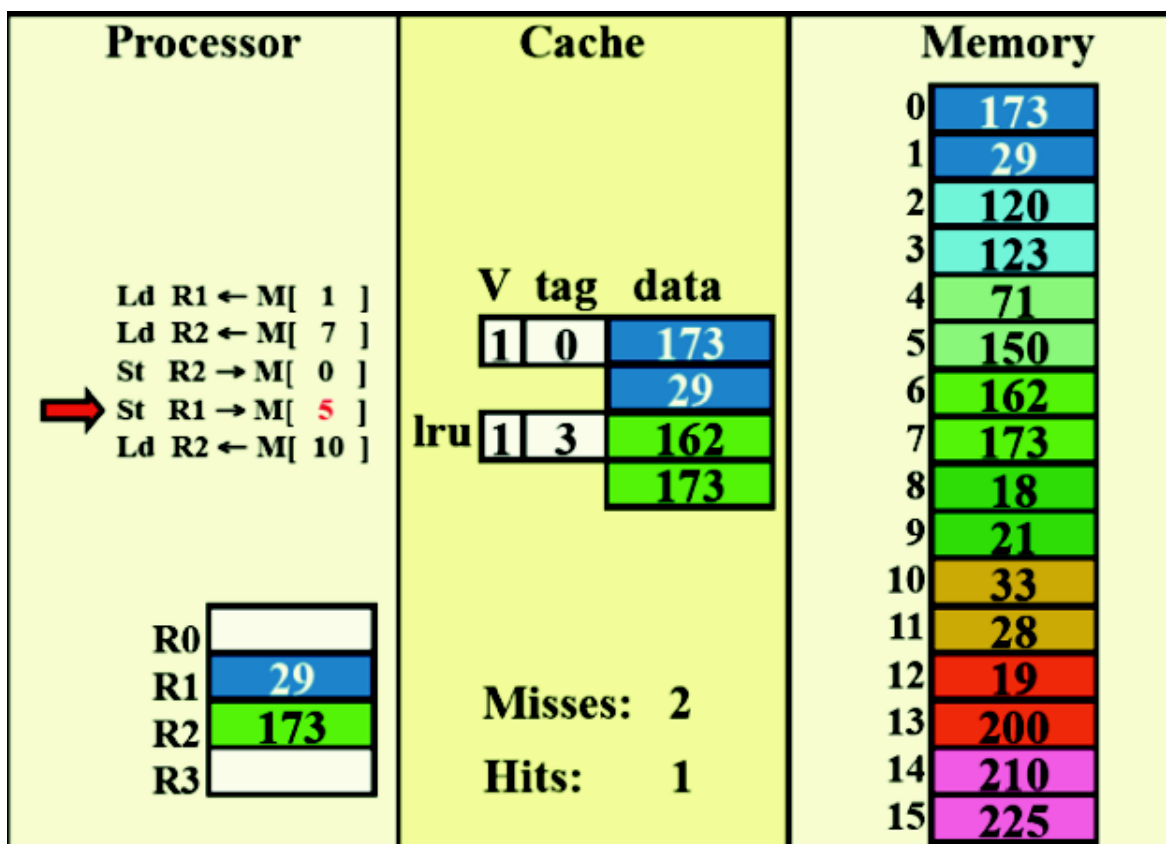
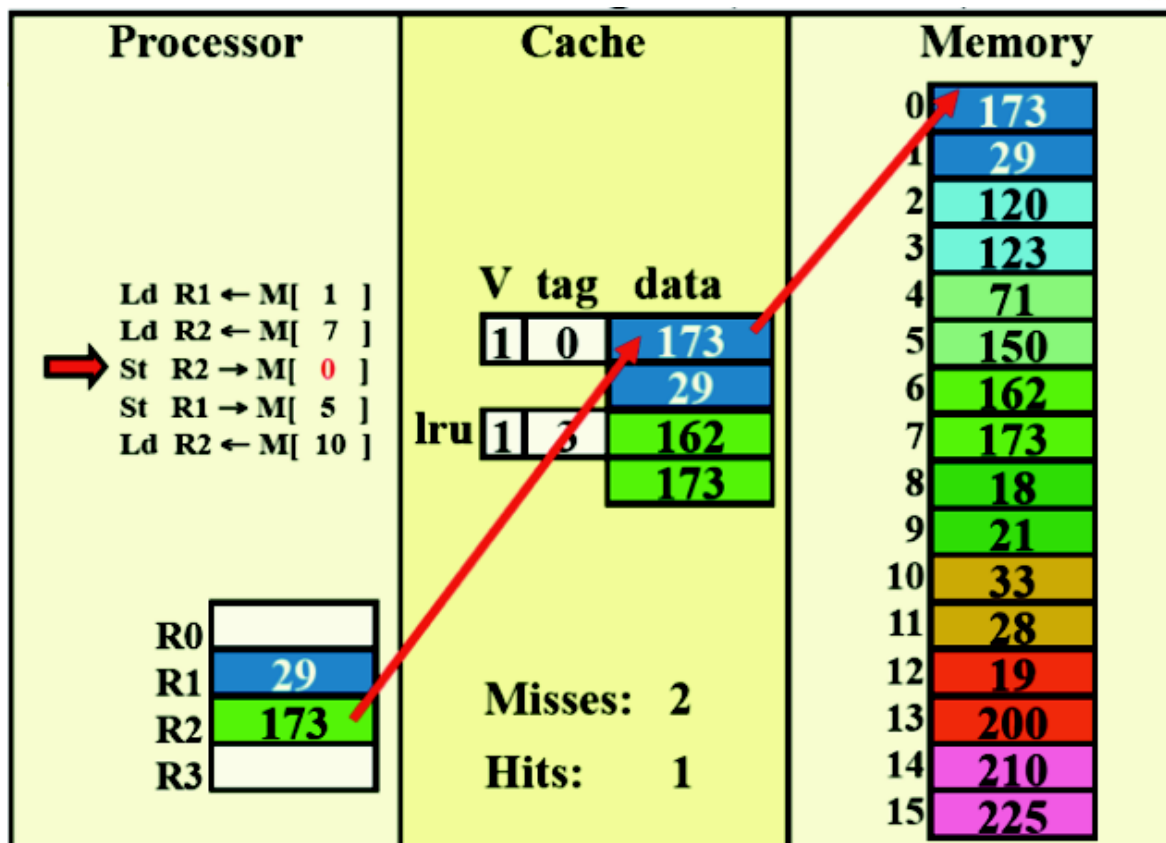




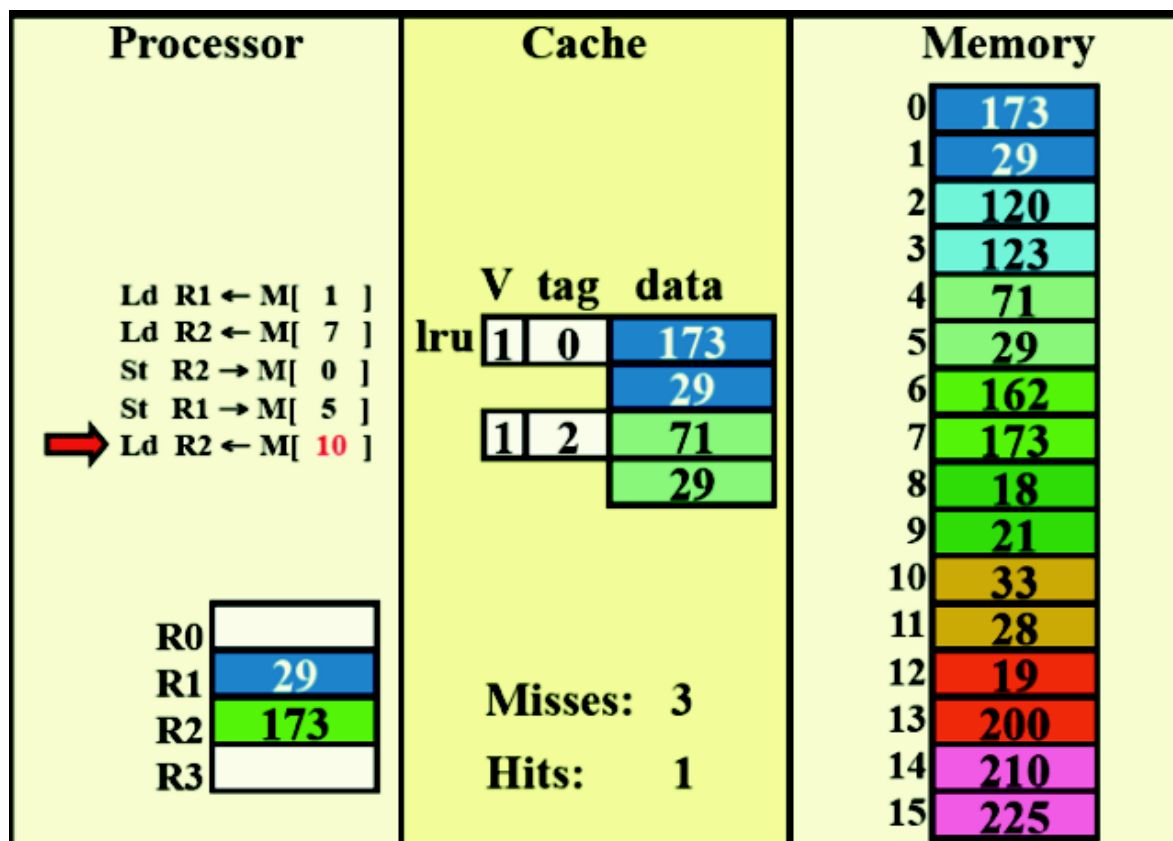
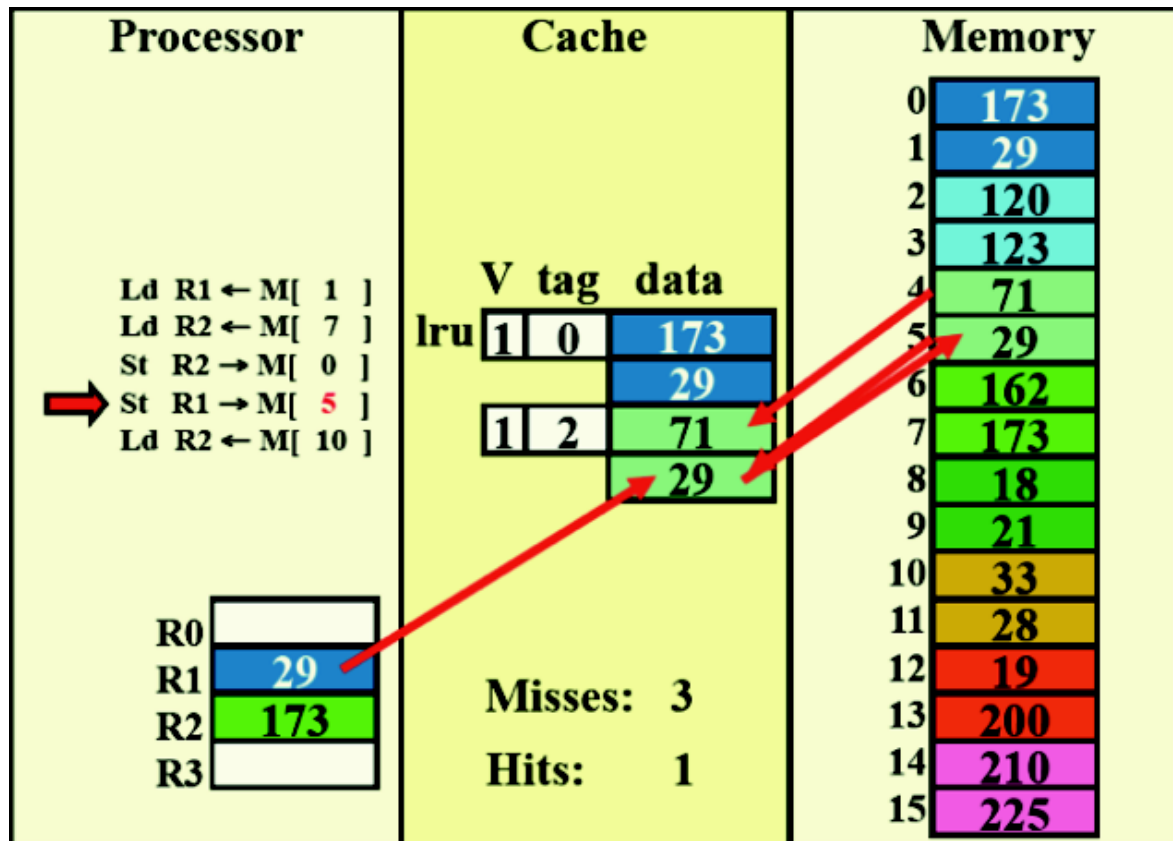




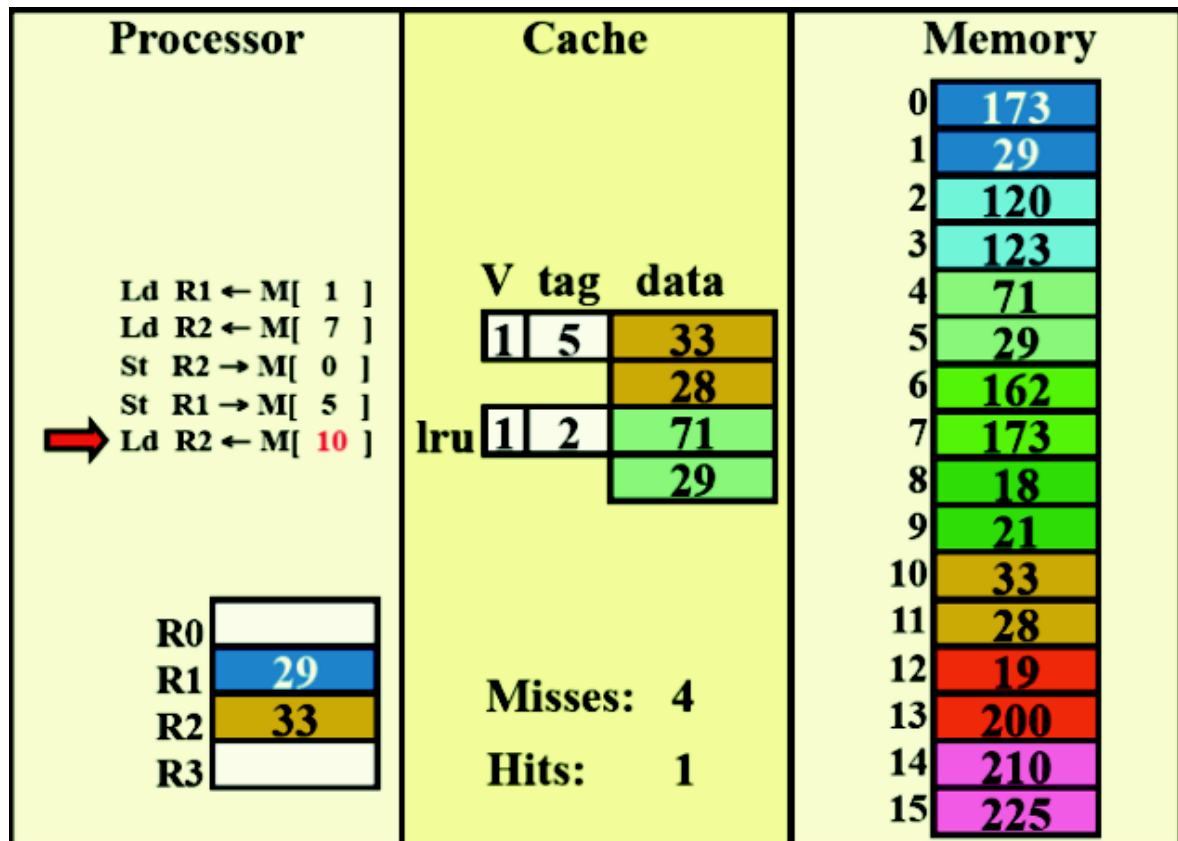














## Ejercicio 4

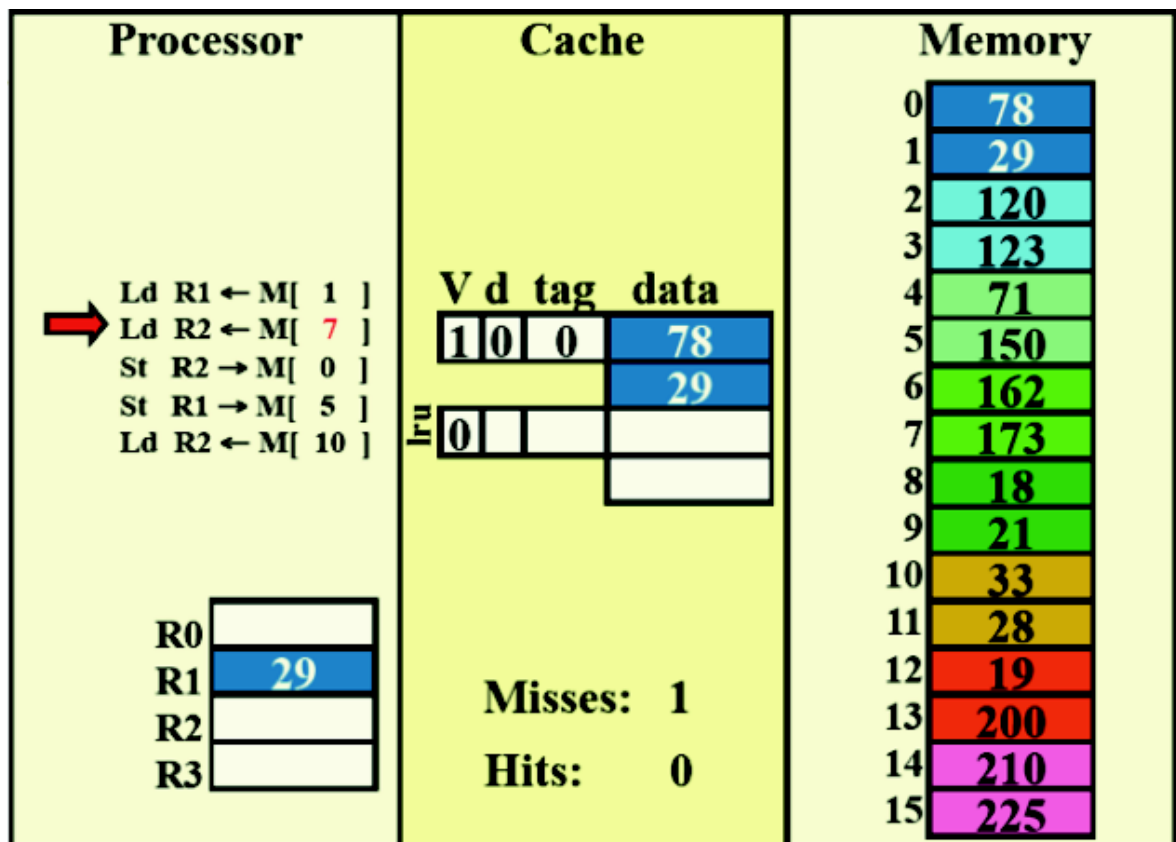
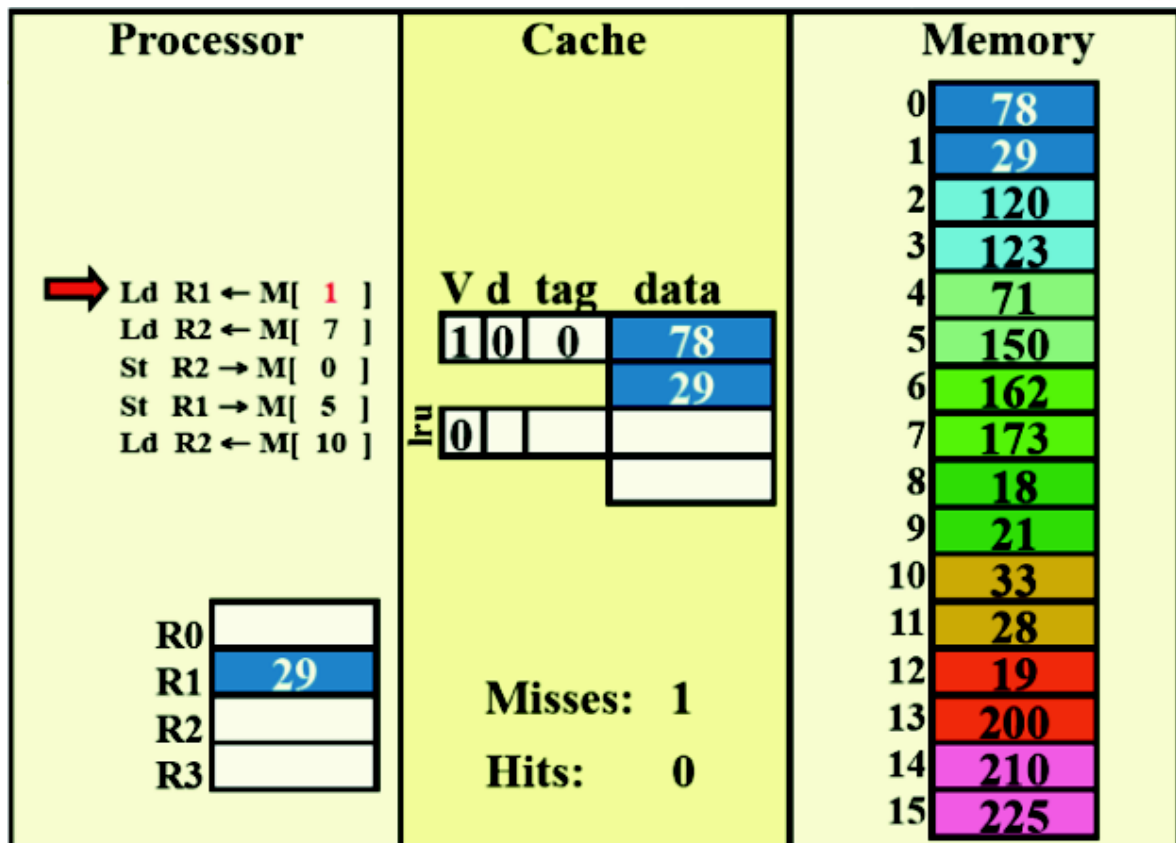
Escritura en memoria (write-back)

### Solución

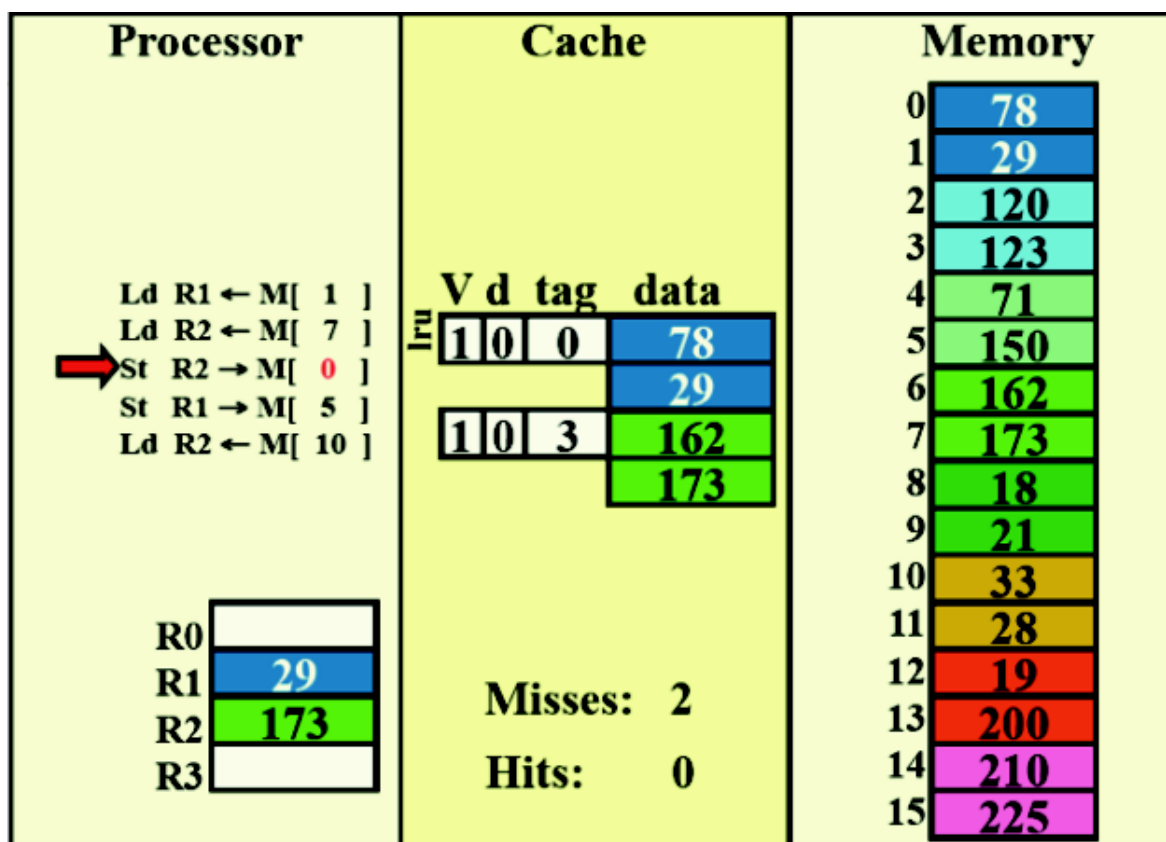
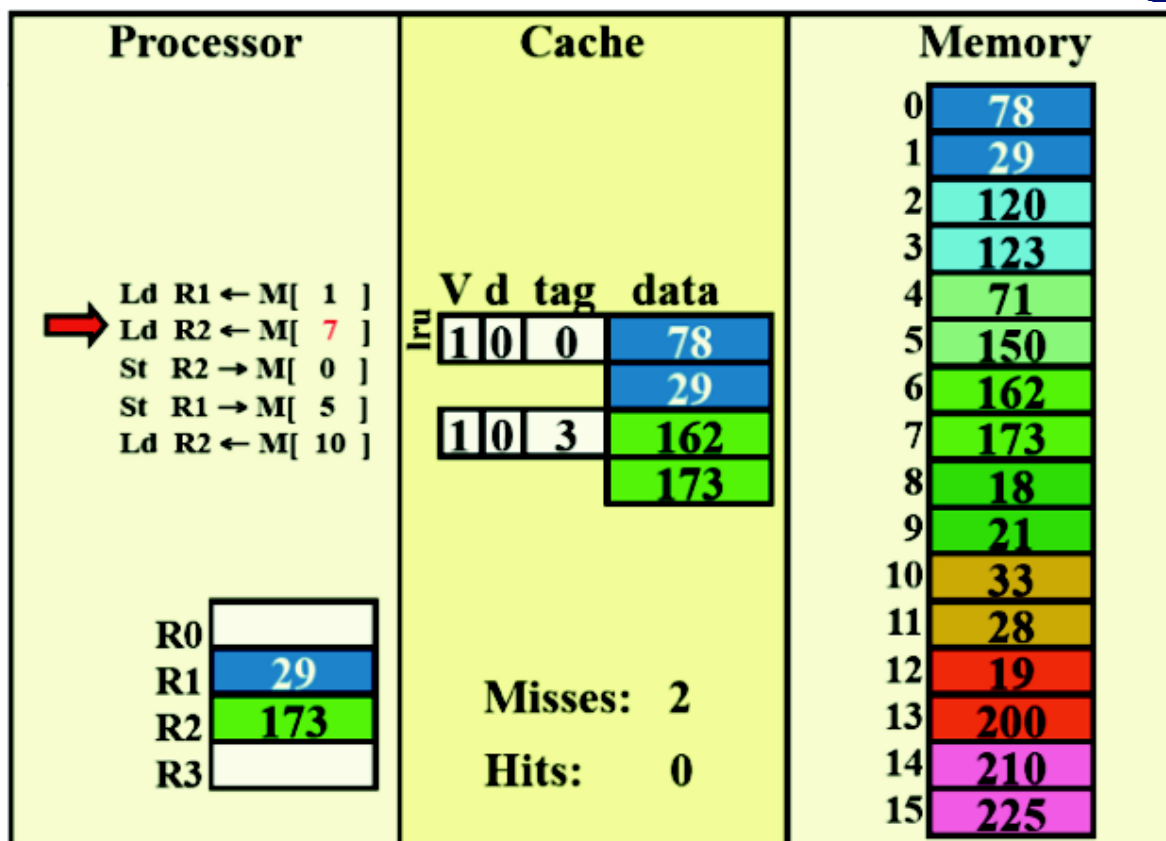
Processor	Cache	Memory
<p>Ld R1 ← M[ 1 ]</p> <p>Ld R2 ← M[ 7 ]</p> <p>St R2 → M[ 0 ]</p> <p>St R1 → M[ 5 ]</p> <p>Ld R2 ← M[ 10 ]</p>	<p><b>V d tag data</b></p> <p>0 0</p> <p>0 0</p>	<p>0 78</p> <p>1 29</p> <p>2 120</p> <p>3 123</p> <p>4 71</p> <p>5 150</p> <p>6 162</p> <p>7 173</p> <p>8 18</p> <p>9 21</p> <p>10 33</p> <p>11 28</p> <p>12 19</p> <p>13 200</p> <p>14 210</p> <p>15 225</p>
<p>R0</p> <p>R1</p> <p>R2</p> <p>R3</p>	<p>Misses: 0</p> <p>Hits: 0</p>	

Processor	Cache	Memory
<p>→ Ld R1 ← M[ 1 ]</p> <p>Ld R2 ← M[ 7 ]</p> <p>St R2 → M[ 0 ]</p> <p>St R1 → M[ 5 ]</p> <p>Ld R2 ← M[ 10 ]</p>	<p><b>V d tag data</b></p> <p>0 0</p> <p>0 0</p>	<p>0 78</p> <p>1 29</p> <p>2 120</p> <p>3 123</p> <p>4 71</p> <p>5 150</p> <p>6 162</p> <p>7 173</p> <p>8 18</p> <p>9 21</p> <p>10 33</p> <p>11 28</p> <p>12 19</p> <p>13 200</p> <p>14 210</p> <p>15 225</p>
<p>R0</p> <p>R1</p> <p>R2</p> <p>R3</p>	<p>Misses: 0</p> <p>Hits: 0</p>	

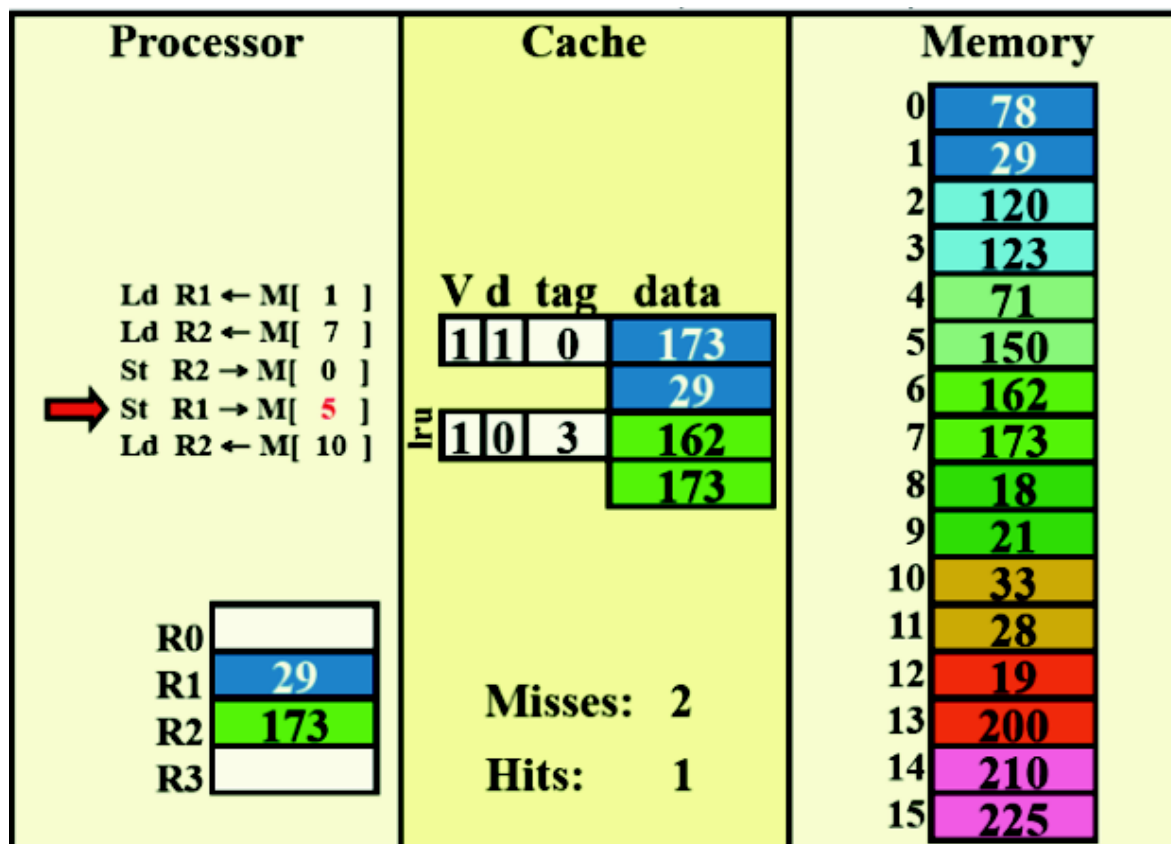
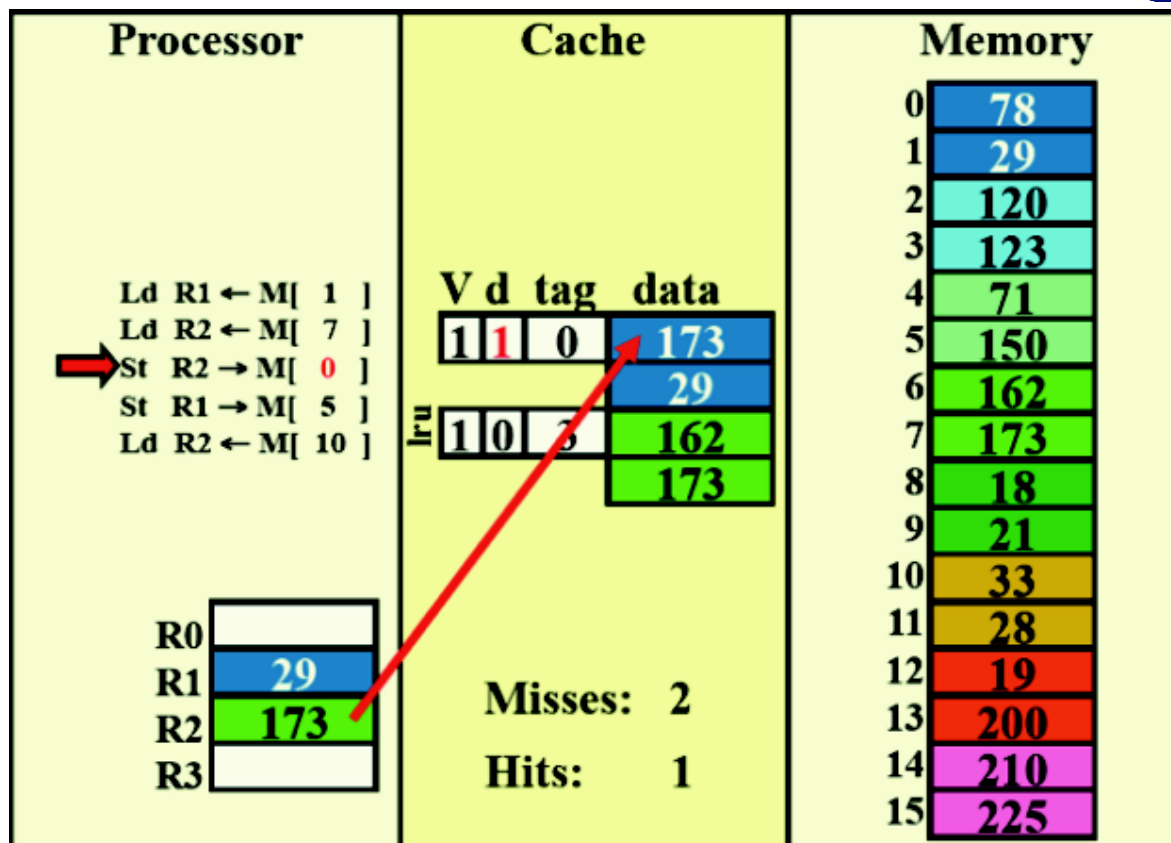




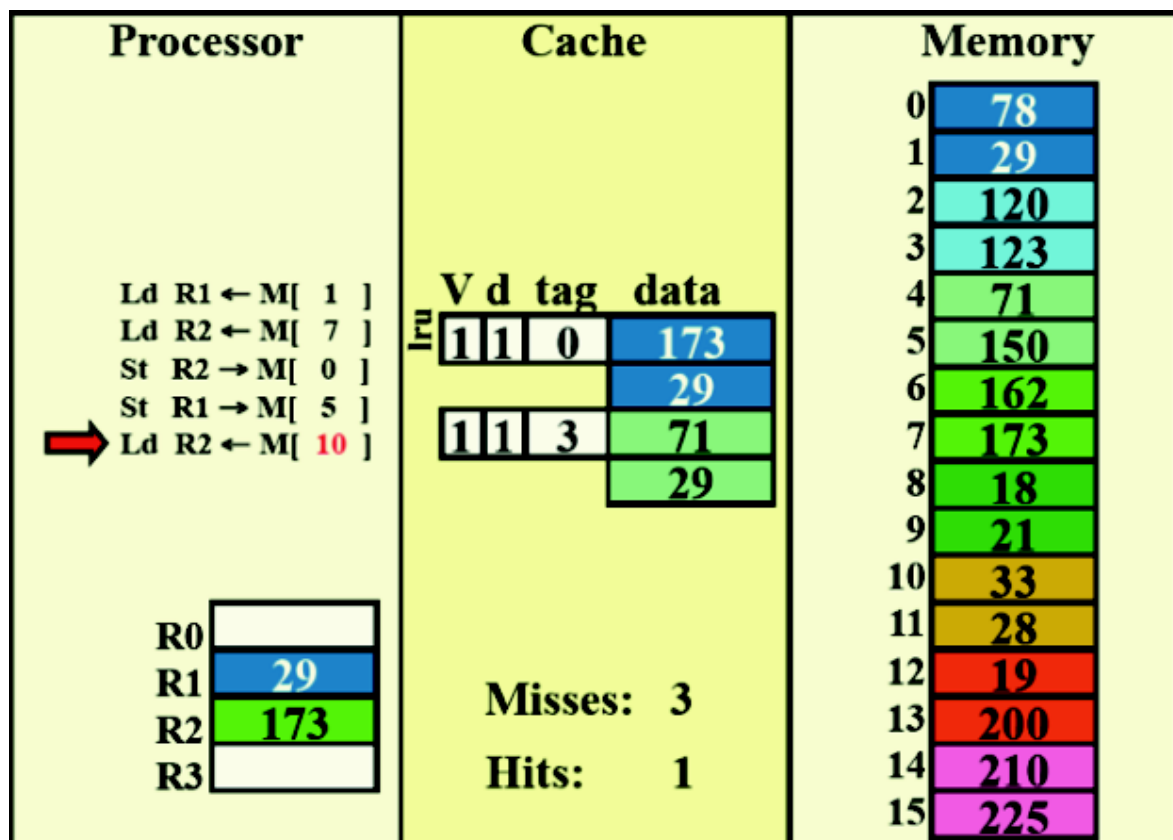
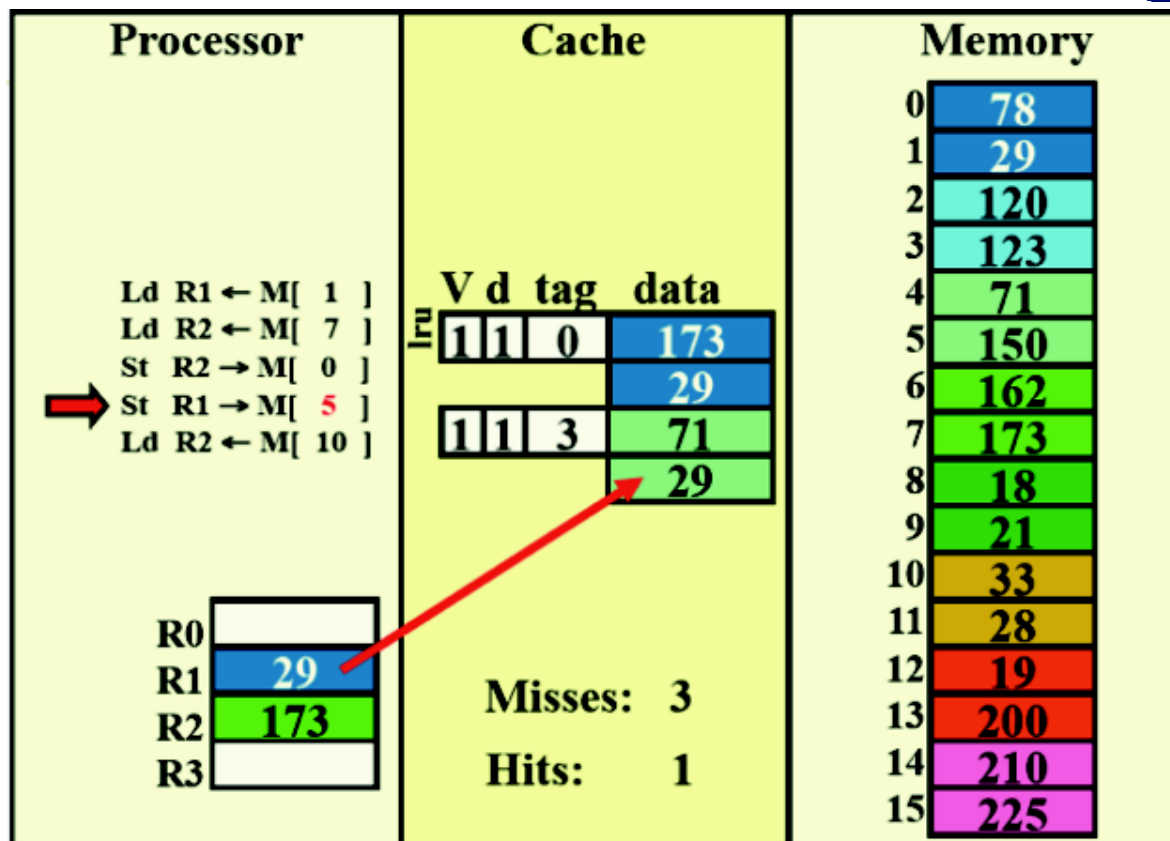




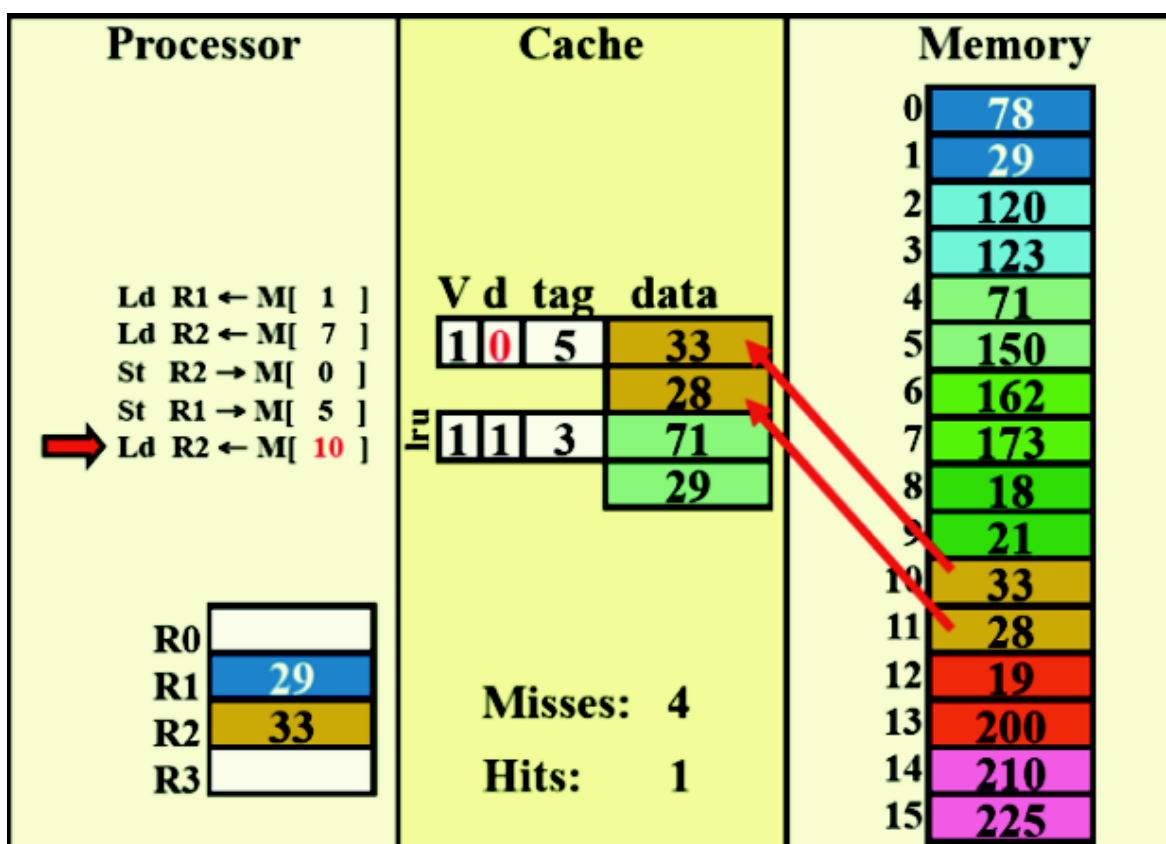
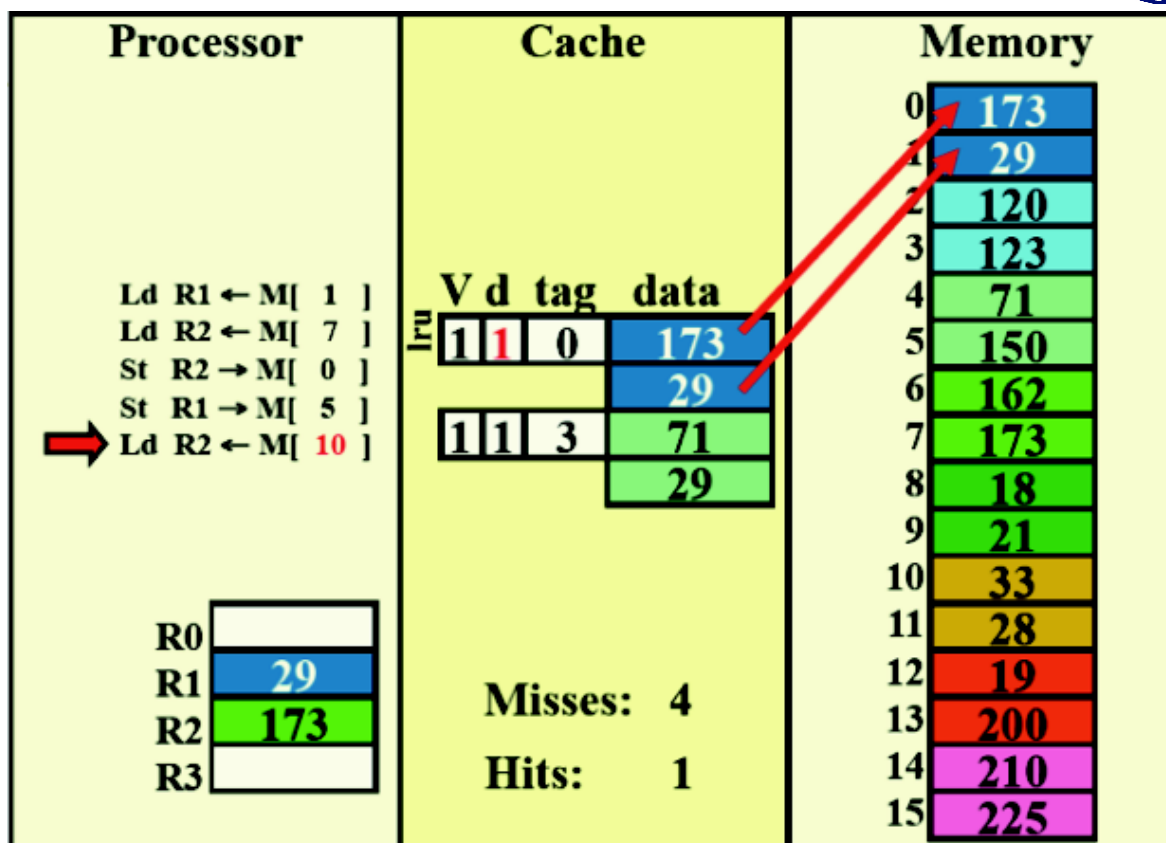










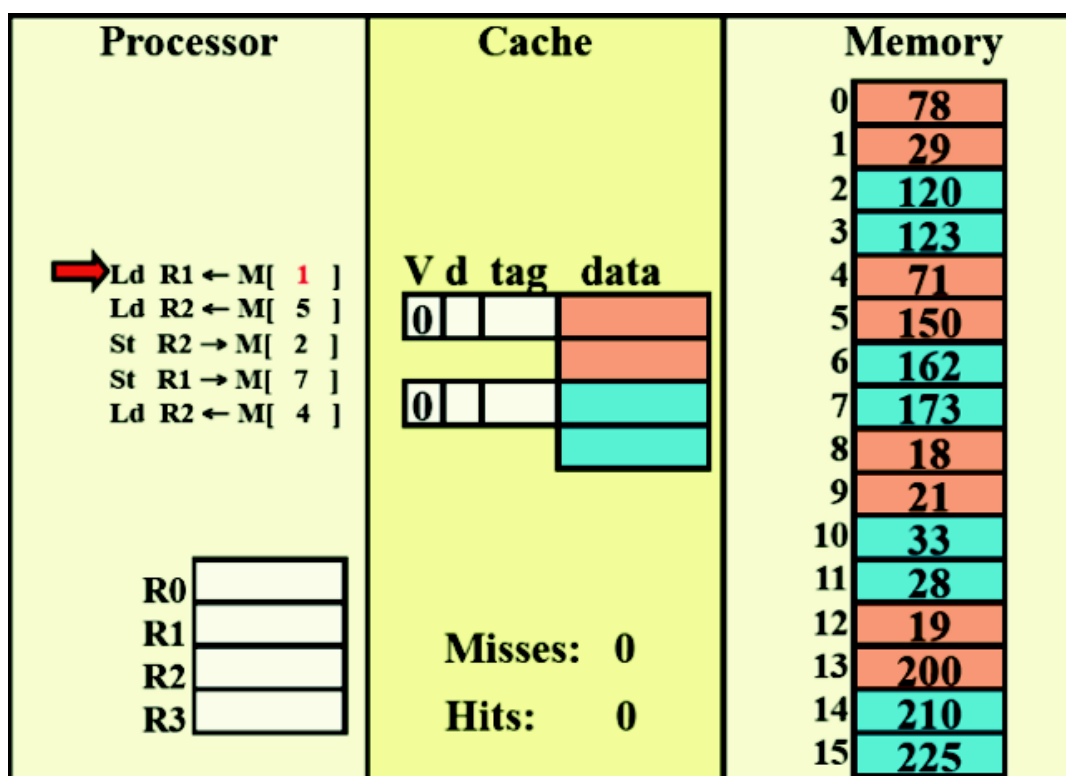
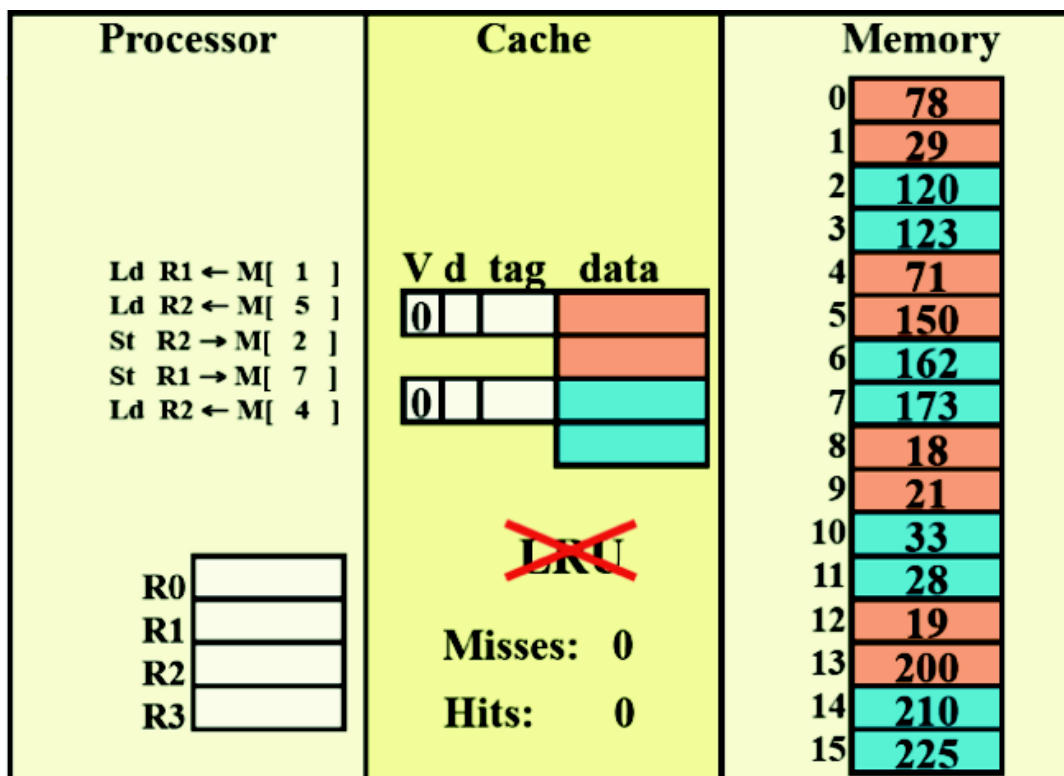




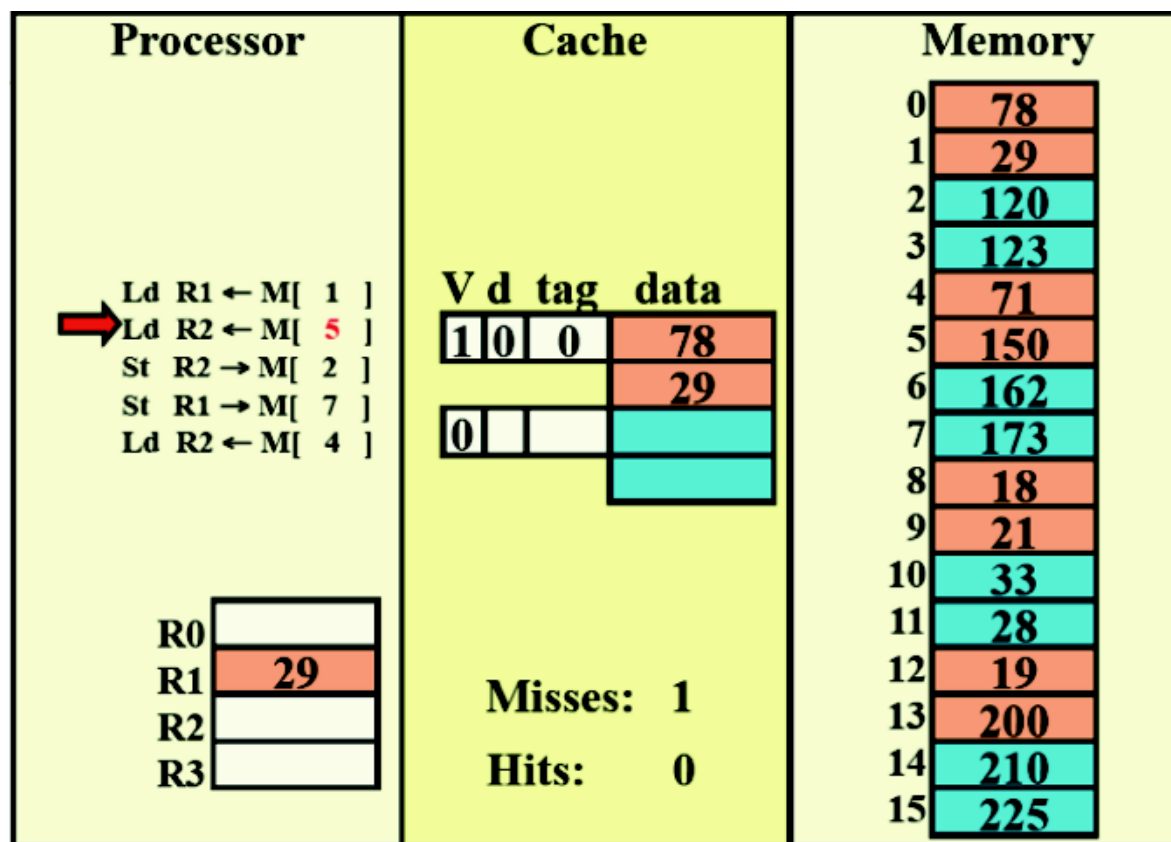
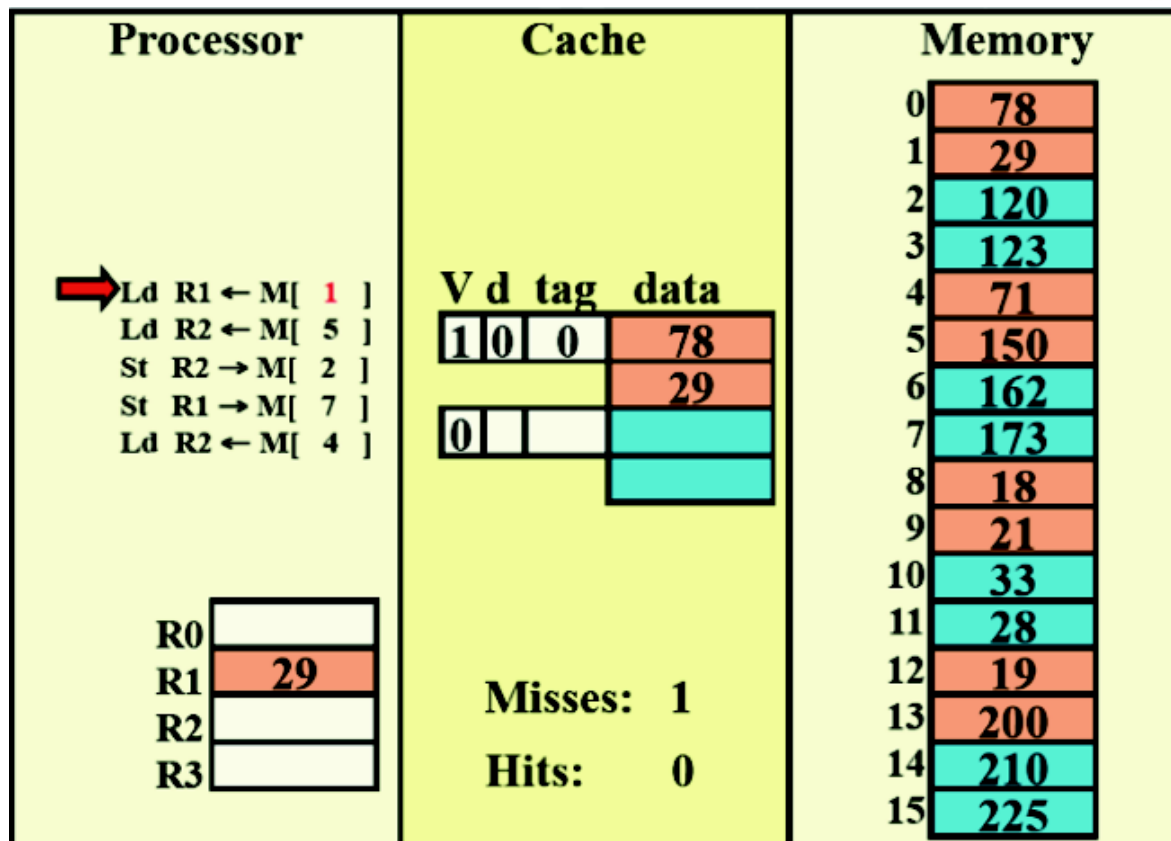
## Ejercicio 5

Mapeo directo

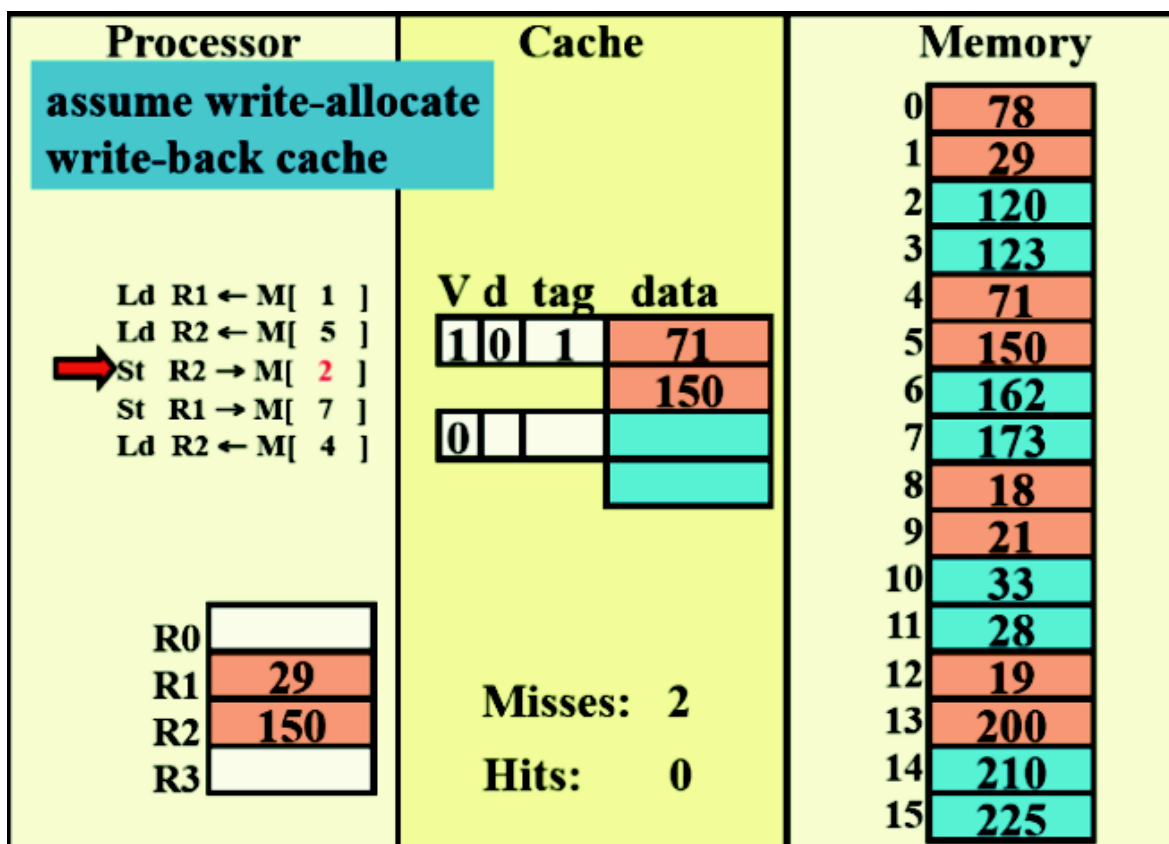
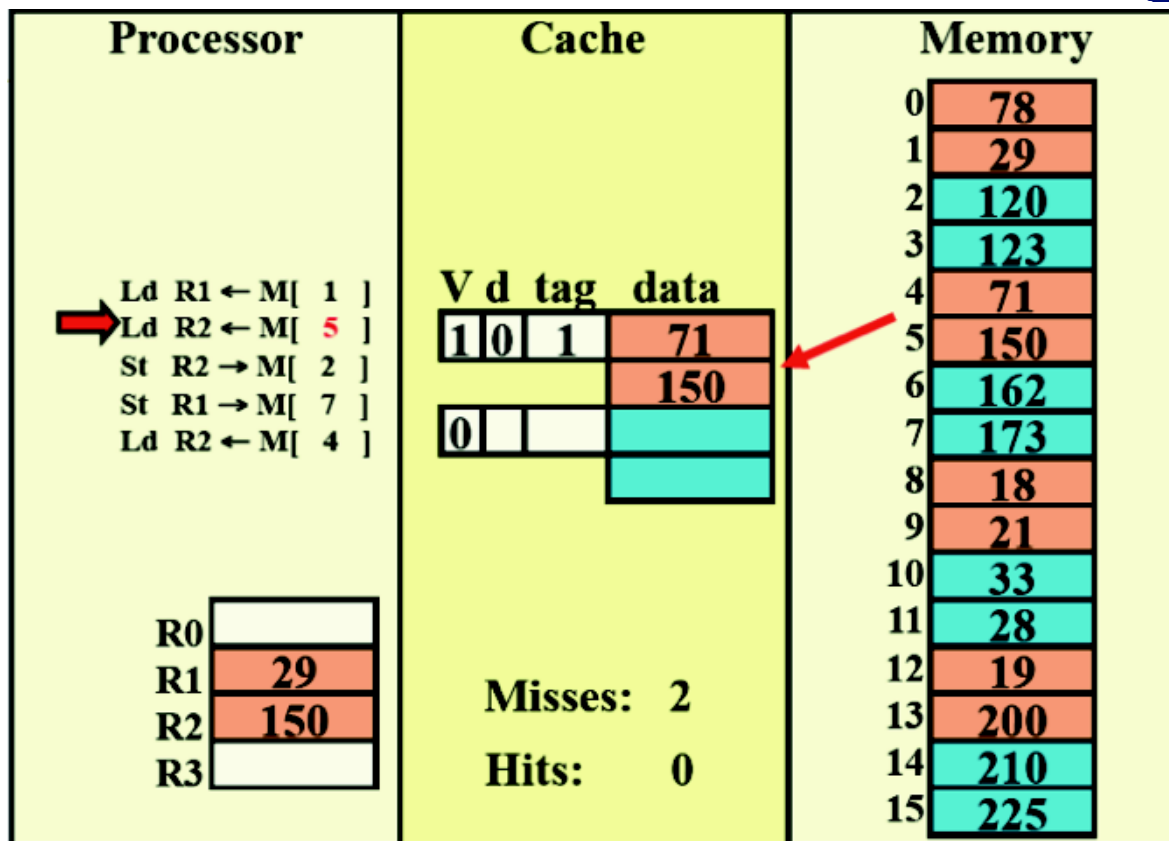
### Solución



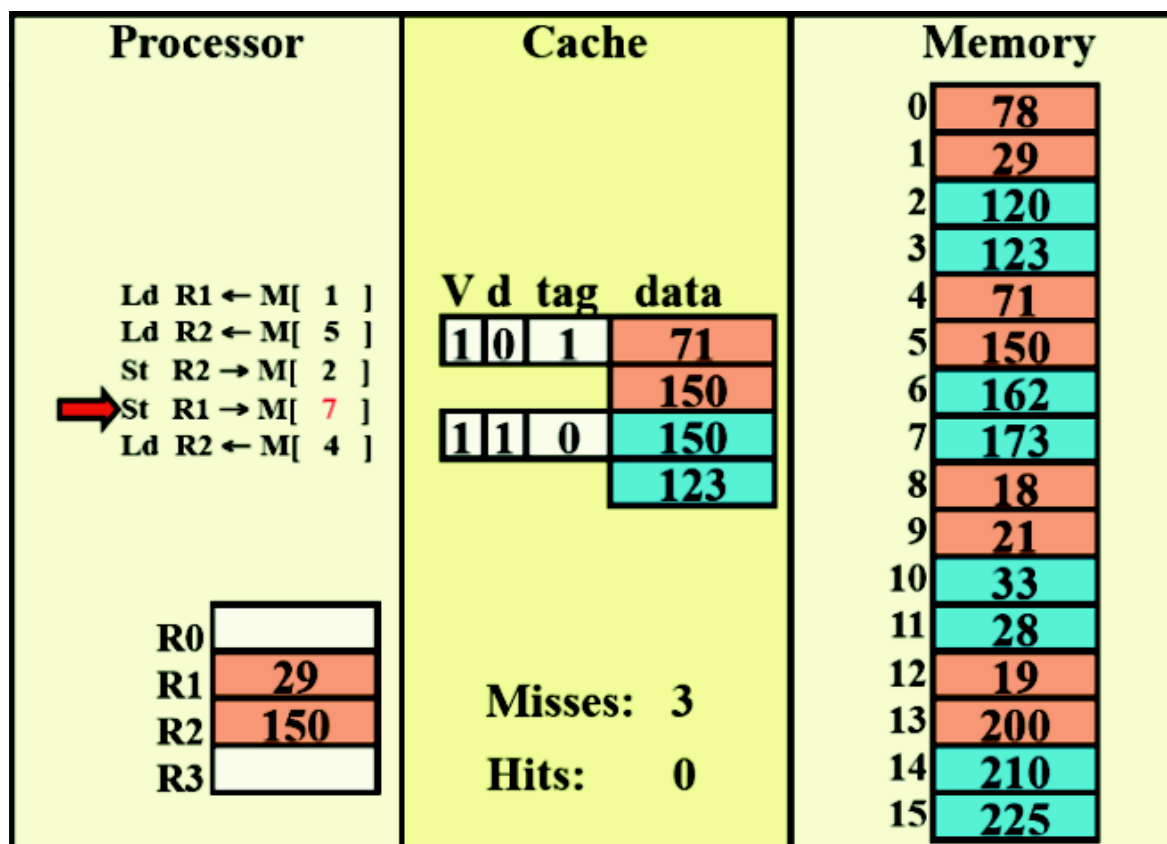
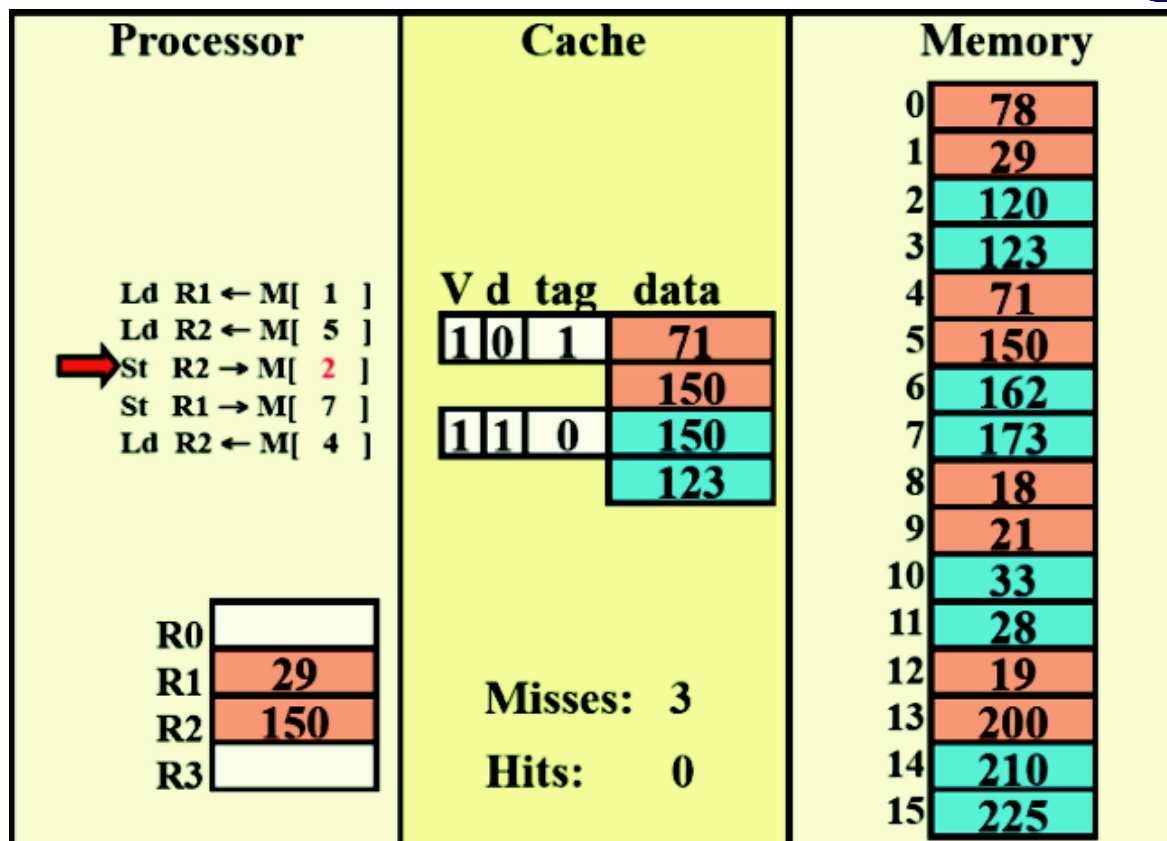




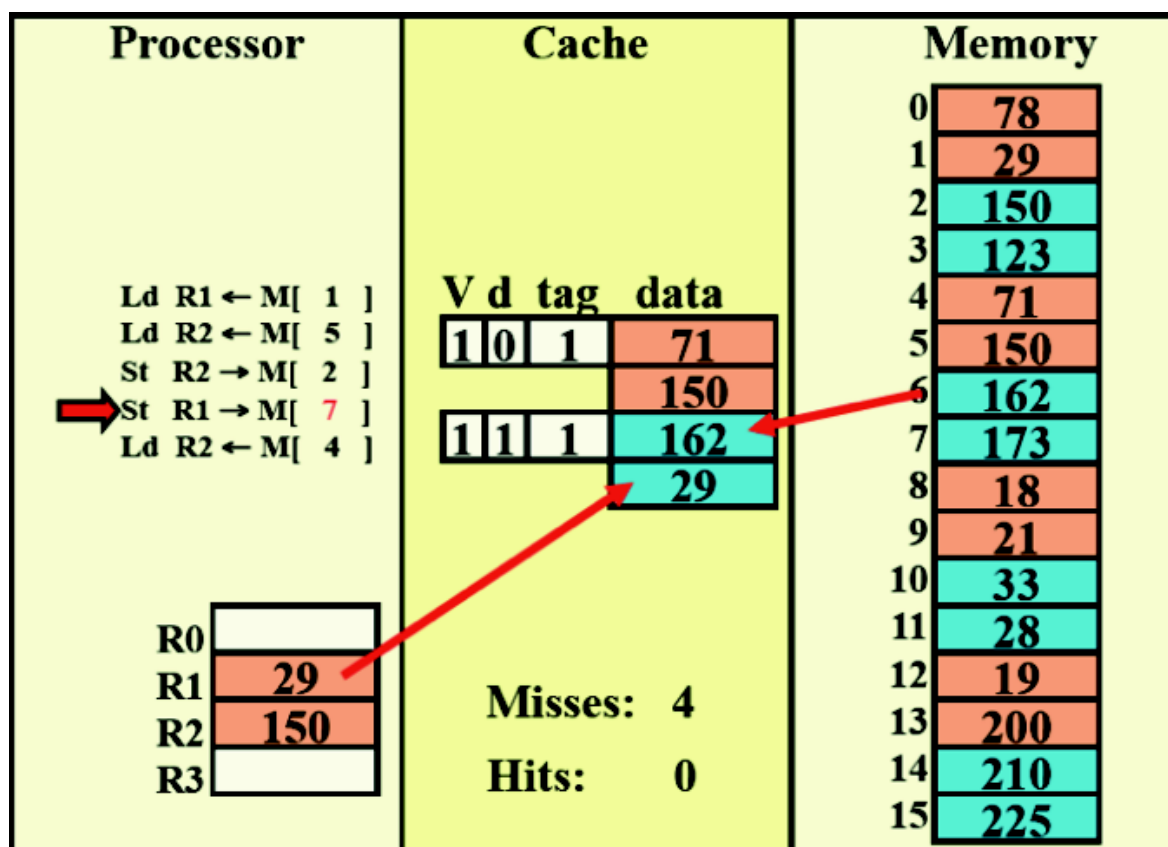
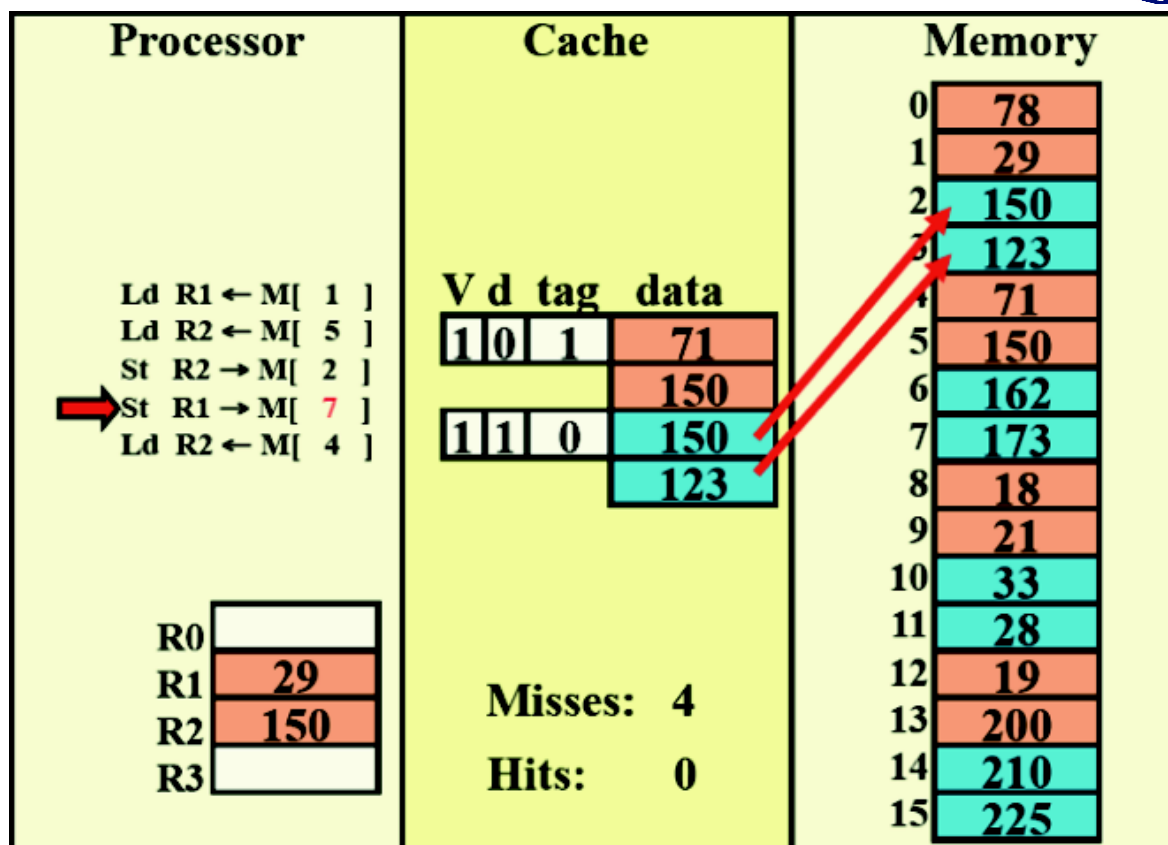














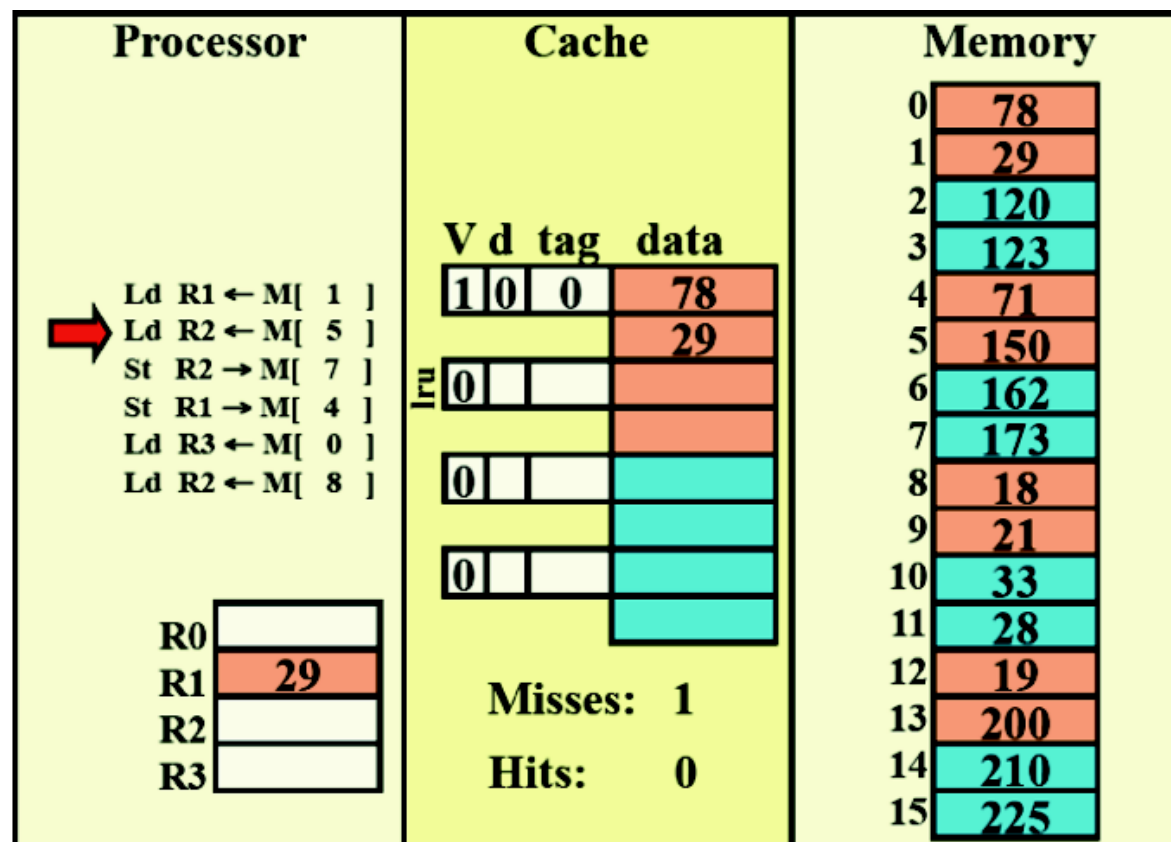
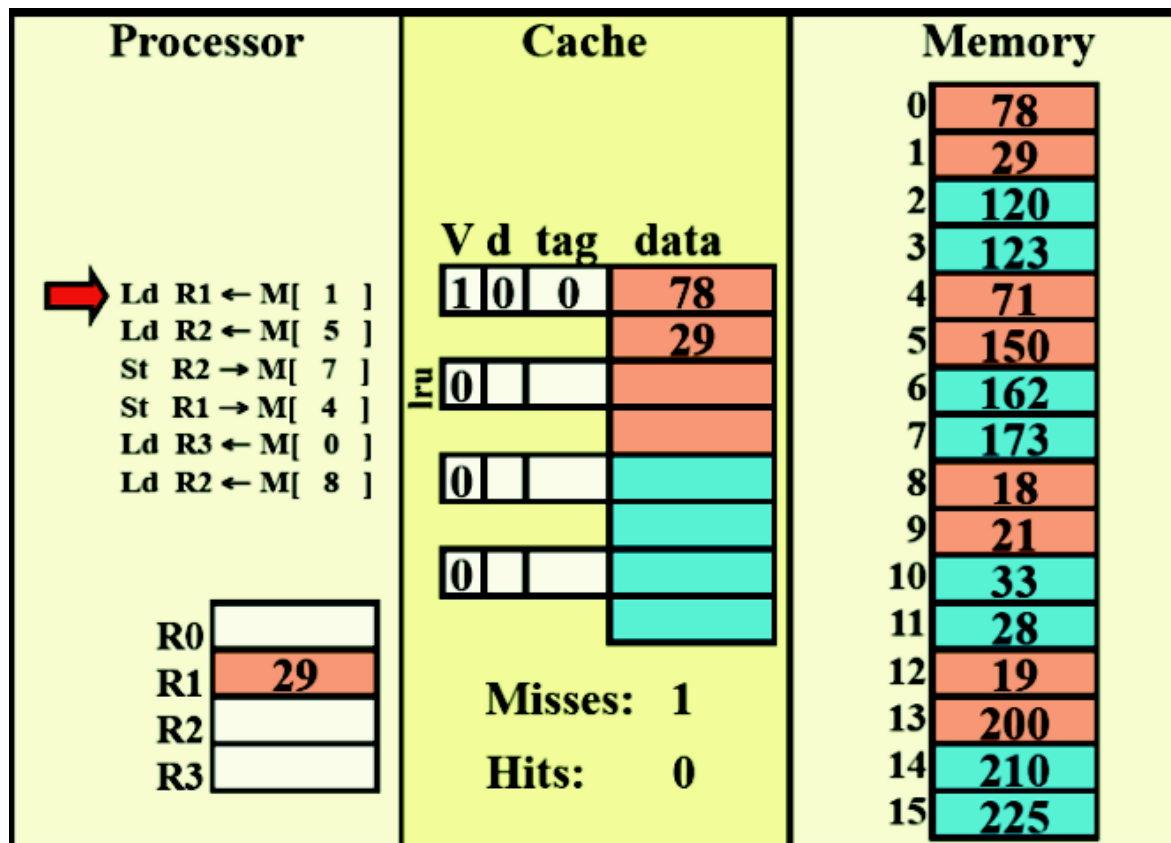
Processor	Cache	Memory																																																				
<div>Ld R1 ← M[ 1 ] Ld R2 ← M[ 5 ] St R2 → M[ 2 ] St R1 → M[ 7 ] ➔ Ld R2 ← M[ 4 ]</div>	<div><table><thead><tr><th>V</th><th>d</th><th>tag</th><th>data</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>0</td><td>71</td></tr><tr><td></td><td></td><td></td><td>150</td></tr><tr><td>1</td><td>1</td><td>1</td><td>162</td></tr><tr><td></td><td></td><td></td><td>29</td></tr></tbody></table><div>Misses: 4 Hits: 0</div></div>	V	d	tag	data	1	0	0	71				150	1	1	1	162				29	<div><table><tbody><tr><td>0</td><td>78</td></tr><tr><td>1</td><td>29</td></tr><tr><td>2</td><td>150</td></tr><tr><td>3</td><td>123</td></tr><tr><td>4</td><td>71</td></tr><tr><td>5</td><td>150</td></tr><tr><td>6</td><td>162</td></tr><tr><td>7</td><td>173</td></tr><tr><td>8</td><td>18</td></tr><tr><td>9</td><td>21</td></tr><tr><td>10</td><td>33</td></tr><tr><td>11</td><td>28</td></tr><tr><td>12</td><td>19</td></tr><tr><td>13</td><td>200</td></tr><tr><td>14</td><td>210</td></tr><tr><td>15</td><td>225</td></tr></tbody></table></div>	0	78	1	29	2	150	3	123	4	71	5	150	6	162	7	173	8	18	9	21	10	33	11	28	12	19	13	200	14	210	15	225
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Processor	Cache	Memory
<div><div><div></div><div></div><div></div><div></div></div><div><div>Ld R1 ← M[ 1 ]</div><div>Ld R2 ← M[ 5 ]</div><div>St R2 → M[ 7 ]</div><div>St R1 → M[ 4 ]</div><div>Ld R3 ← M[ 0 ]</div><div>Ld R2 ← M[ 8 ]</div></div></div> <div><div>R0</div><div>R129</div><div>R2150</div><div>R3</div></div>	<div><div>Vdtagdata</div><div><div>10078</div><div></div><div>10171</div><div></div><div>0</div><div></div><div>0</div><div></div></div><div><div>Misses: 2</div><div>Hits: 0</div></div></div>	<div><div>078</div><div>129</div><div>2120</div><div>3123</div><div>471</div><div>5150</div><div>6162</div><div>7173</div><div>818</div><div>921</div><div>1033</div><div>1128</div><div>1219</div><div>13200</div><div>14210</div><div>15225</div></div>


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