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Unit 1. Introduction and overview of SoCs

System-on-Chip and efficient electronic circuit integration techniques

Carlos III University of Madrid, Spain

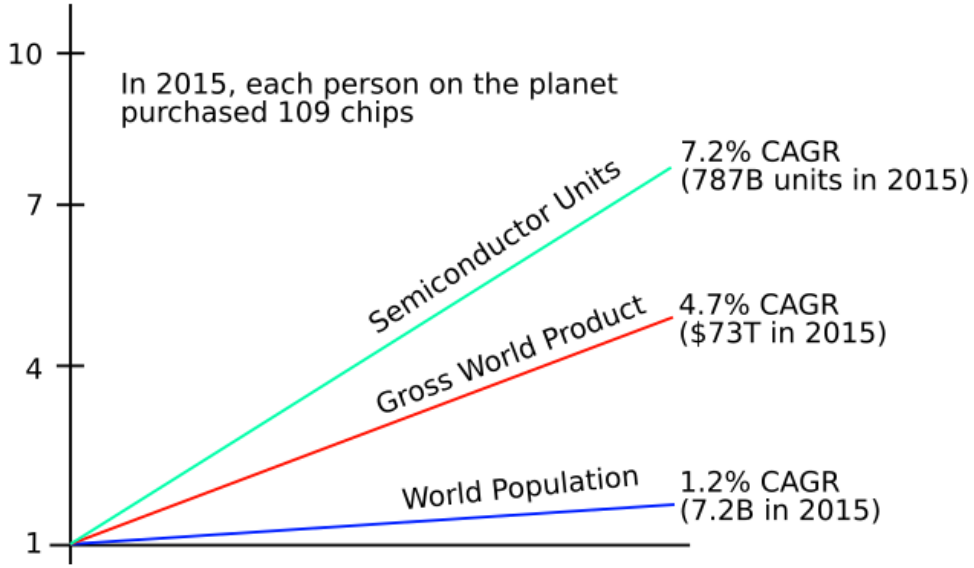
Electronics Technology Department

Outline

1. Introduction and overview of SoCs
2. Scaling problems
3. State-of-the-art SoC
4. CMOS main features

1. Introduction and overview of SoCs

- Semiconductor market growth:



CAGR: Compound Annual Growth Rate

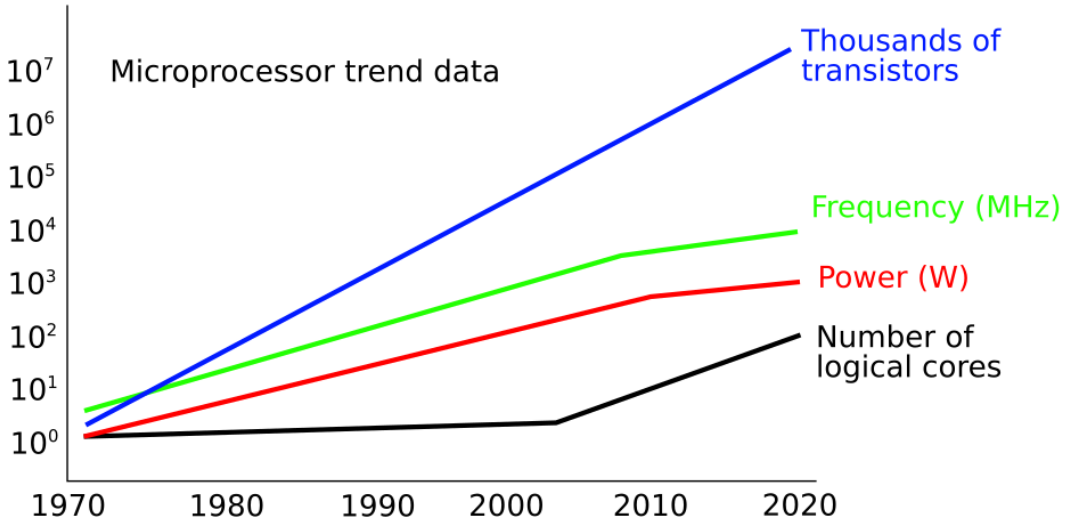
Ubiquitous electronics

- More and more intelligent and connected devices are around us.
- Computing Revolution: CPUs are incredibly powerful, with “machine learning” based HW accelerators, and assisted sensors and microcontrollers to keep performance at the best level.

Original data from I. Fujimori, P. Hanumolu and I. Fujimori, "EE4: Semiconductor economics: How business decisions are engineered," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 523-523

1. Introduction and overview of SoCs

- Moore's law:
  - **Chip Area** ↓
  - **Chip Cost** ↑
    - If analog area cannot be scaled along with digital → chip cost will increase.
    - Analog circuits must be scaled. Otherwise they cannot be integrated.
    - Digital calibration realized drastic power and area savings.
    - But, does it always make sense?

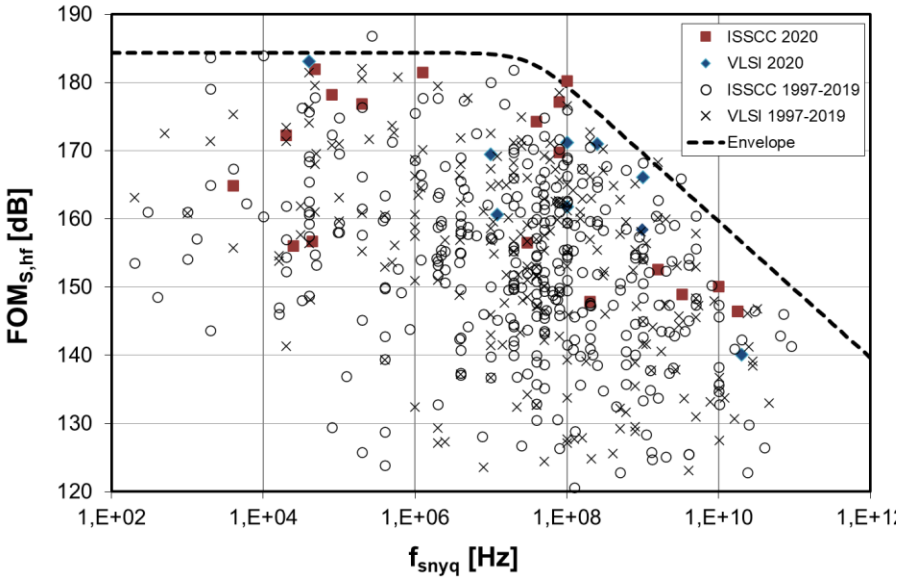


Original data up to the year 2010 collected by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten.
Data from 2010 up to 2017 collected and plotted by K. Rupp

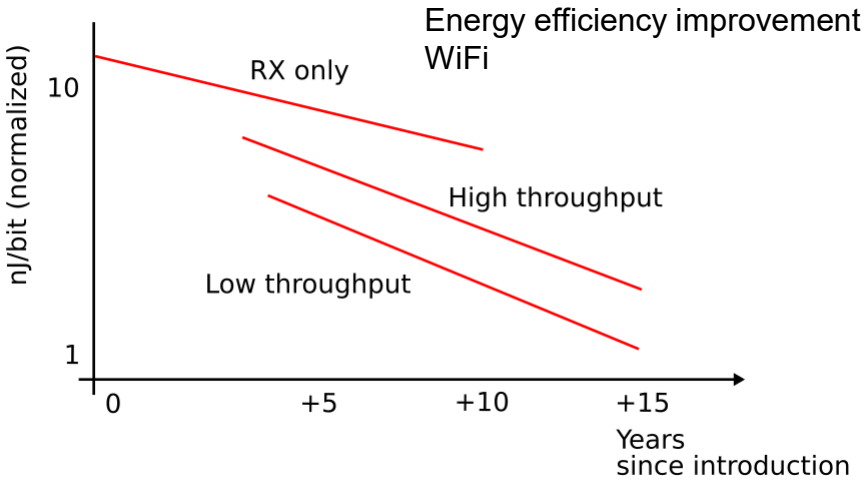
- More architectural innovations are needed for the same node.
- New fabrication and/or integration methods are required

1. Introduction and overview of SoCs

- Bandwidth and energy efficiency have improved over the last years:
  - New coding schemes
  - Architectural improvements



Original data from B. Murmann, "ADC Performance Survey 1997-2020," [Online] Available: http://web.stanford.edu/~murmann/adcsurvey.html.



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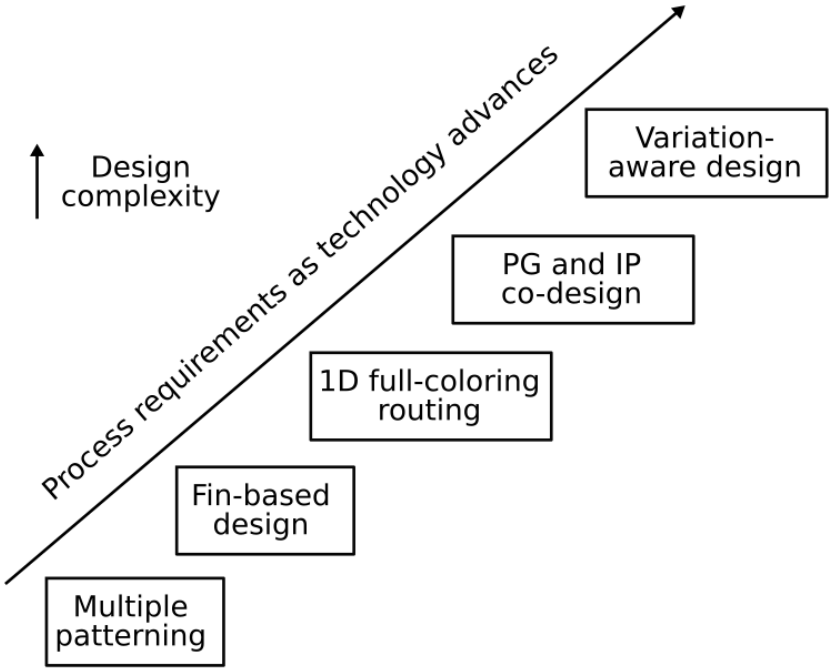
1. Introduction and overview of SoCs

- Dealing with narrow technology nodes implies a higher complexity in the design:



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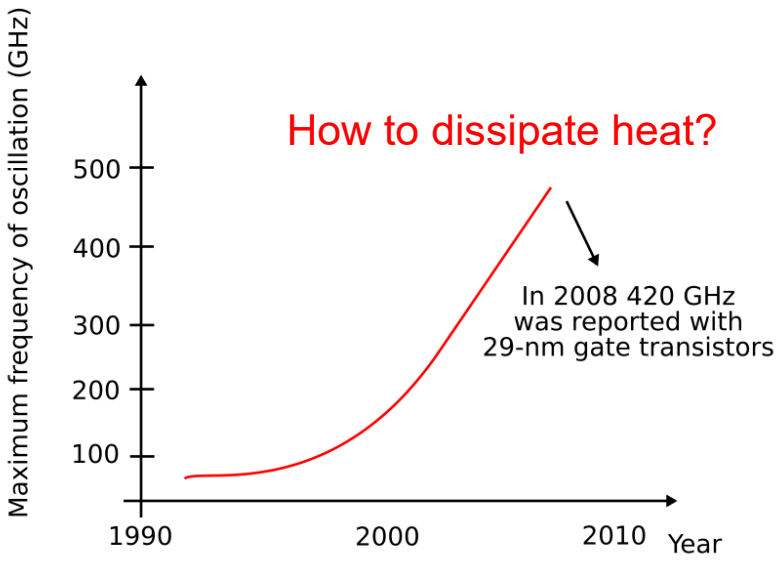

Original data Frank Schwierz, Hei Wong, and Juin J. Liou. 2008. Nanometer CMOS. World Scientific Publishing Co., Inc., USA.

Original data Post, I. et al. "A 65nm CMOS SOC Technology Featuring Strained Silicon Transistors for RF Applications." 2006 International Electron Devices Meeting (2006): 1-3.

2. Scaling problems

- Analog circuits do not scale well with the narrowest nodes, digital circuits do.
  - $g_m/I_d \approx$ constant
  - Cut-off frequency ⇧ (digital)
  - V_{DD} ⇩ (digital, analog)
  - Speed ⇧ (digital)
  - Area ⇩ (digital)
  - Signal-to-Noise Ratio (SNR) ⇩ (analog)
  - g_m/g_{ds} ⇩ (analog)
  - Scaling (digital, analog)

3. State-of-the-art SoC

- All the systems can be integrated in the same device.
  - Fully-integrated DVD player application

    K. Okamoto et al., "A fully-integrated 0.13 um CMOS mixed-signal SoC for DVD player applications," 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., San Francisco, CA, USA, 2003, pp. 38-476 vol.1

  - Wearables

    J. Kwong and A. P. Chandrakasan, "An Energy-Efficient Biomedical Signal Processing Platform," in IEEE Journal of Solid-State Circuits, vol. 46, no. 7, pp. 1742-1753, July 2011

  - Radio receiver

    F. Opteynde, "A maximally-digital radio receiver front-end," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, 2010, pp. 450-451

  - Energy harvesting IoT system-on-chip

    A. Klinefelter et al., "21.3 A 6.45μW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3

3. State-of-the-art SoC

- New smart tasks can be also performed on a single chip.
  - Cognitive computing

    C. Gonzalez et al., "3.1 POWER9™: A processor family optimized for cognitive computing with 25Gb/s accelerator links and 16Gb/s PCIe Gen4," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 50-51

  - Keyword spotting and voice recognition

    J. S. P. Giraldo, S. Lauwereins, K. Badami and M. Verhelst, "Vocell: A 65-nm Speech-Triggered Wake-Up SoC for 10- uW Keyword Spotting and Speaker Verification," in IEEE Journal of Solid-State Circuits, vol. 55, no. 4, pp. 868-878, April 2020

  - Neuromorphic computing

    F. Akopyan et al., "TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 10, pp. 1537-1557, Oct. 2015

  - EEG monitoring device to control epyleptic seizures

    M. A. Bin Altaf, C. Zhang and J. Yoo, "A 16-Channel Patient-Specific Seizure Onset and Termination Detection SoC With Impedance-Adaptive Transcranial Electrical Stimulator," in IEEE Journal of Solid-State Circuits, vol. 50, no. 11, pp. 2728-2740, Nov. 2015

4. CMOS main features

- Advantages:
  - Narrow nodes (<40 nm) → high cut-off frequency and high operating frequency.
  - Flexibility
  - High integration
  - Low power
  - Low area
- Disadvantages:
  - Lower intrinsic gain than BJT nodes
  - Small driving capability
  - Flicker noise
  - Threshold voltage not strongly scalable.
  - ESD, crosstalk.