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Unit 2. Advanced CMOS device modeling

System-on-Chip and efficient electronic circuit integration techniques

Carlos III University of Madrid, Spain

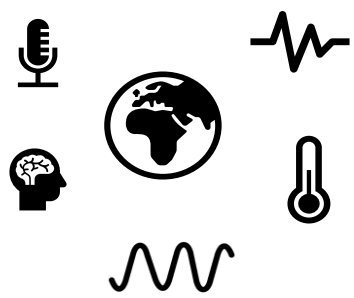
Electronics Technology Department

Outline

1. Introduction to mixed-signal microelectronics
2. MOSFET devices
3. Features extraction
4. Transistor bandwidth (BW)
5. General tips for analog design

1. Introduction to mixed-signal microelectronics

- Currently, most of the signal processing is computed with digital circuits.
- Since the 80s billions of transistors integrated on a single chip are able to perform billions of operations per second.
- Advantages of digital signal processing:
  - Design simplicity.
  - Automatic design tools available.
  - Higher noise robustness.
  - Compact circuits.
- Disadvantages of digital signal processing:
  - Limited resolution.
  - Discrete operation.
- Why do we need then mixed-signal circuits?
  - Signal processing with sensors:



Analog signals from sensors…

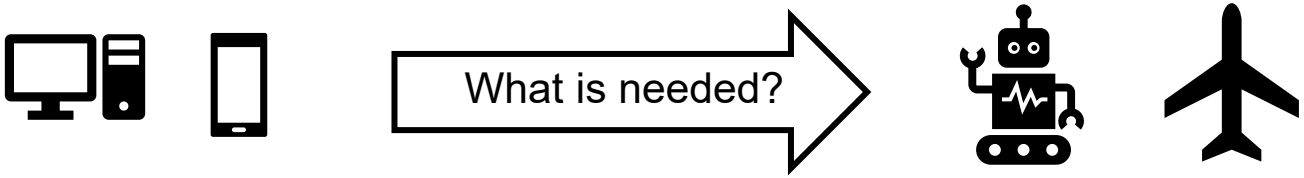
What is needed?

ADC

… and **digital signals** into processors.

1. Introduction to mixed-signal microelectronics

- Why do we need then mixed-signal circuits?
  - Digital control of actuators.

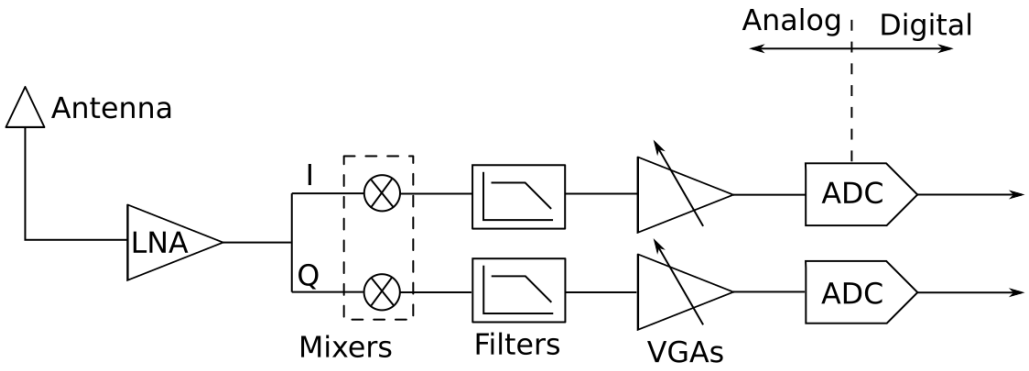


Digital signals from user…

DAC

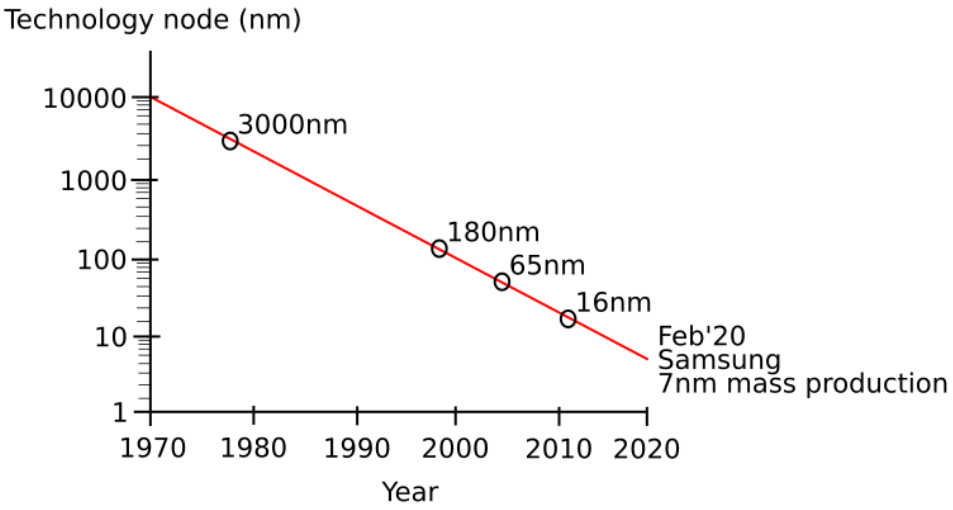
… and **analog signals** to control speed, acceleration, temperature…

  - Digital communications: DAC for transmitter and ADC for receiver.
  - Radioreceivers:



1. Introduction to mixed-signal microelectronics

- Why do we use MOSFET design nodes?
  - Patented by **Liliendeld** in the 30's.
  - They have been intensively used **since the 60's**.
  - **CMOS-based digital design**: only dynamic power consumption (logic transitions) and less area. Lower manufacturing costs and higher scalability.
  - **CMOS-based analog design**: high speed and less noisy than BJT nodes. Lower intrinsic gain, but higher input impedance. High scalability has enabled operating frequencies similar to BJT-based architectures.
  - In the narrowest nodes the parasitic resistances and capacitors become more limiting.

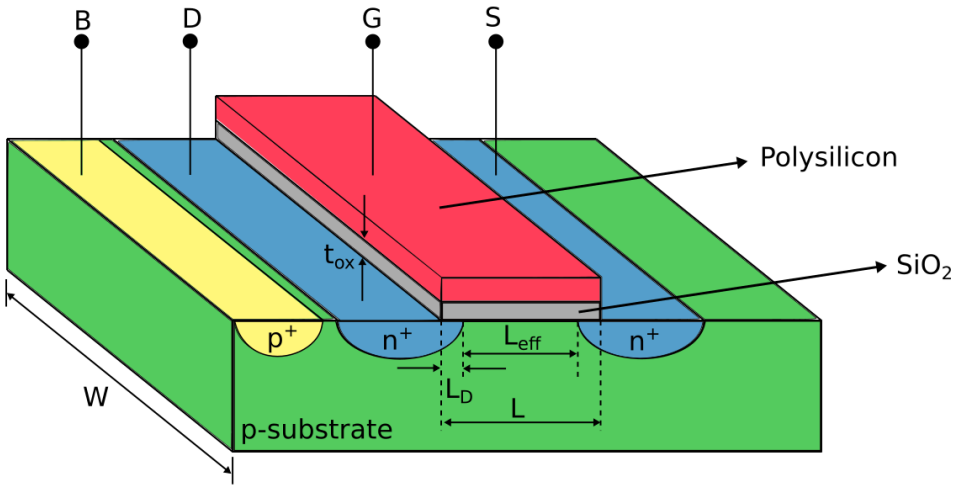


Year	1999	2001	2004	2008	2011	2014
Tech.Node (nm)	180	130	90	60	40	30
Supply (V)	1.5-1.8	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	0.3-0.6
Wiring levels	6-7	7	8	9	9-10	10
Max. Frequency (GHz)	1.2	2.1	3.5	7.1	11	14.9

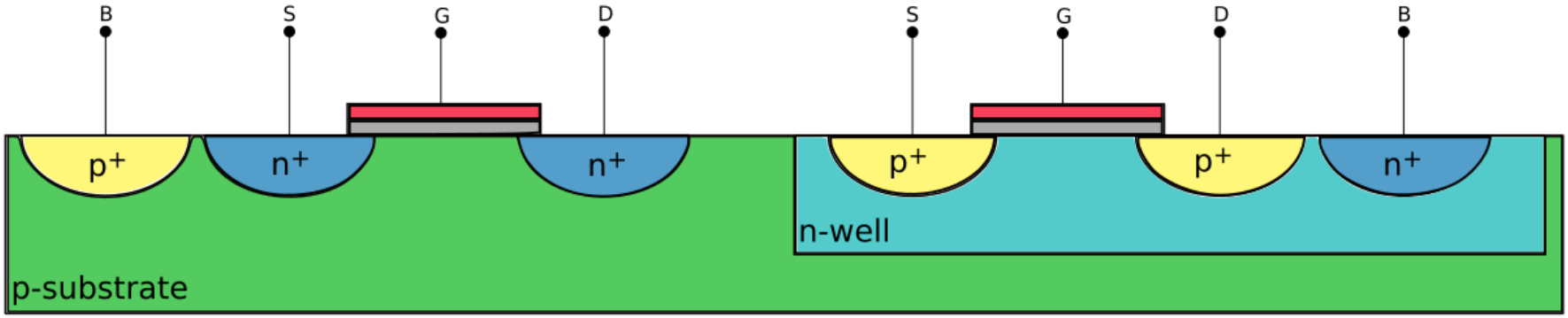
Data source:
International Technology Roadmap for Semiconductors

2. MOSFET devices

- NMOS basic structure:

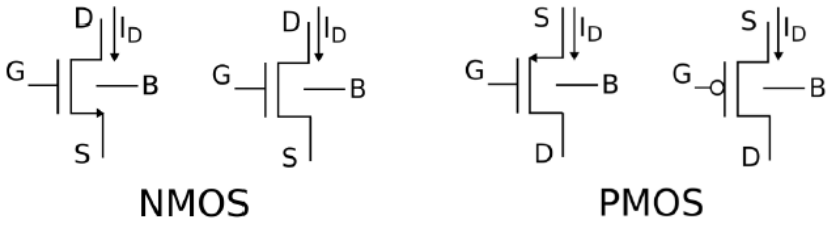


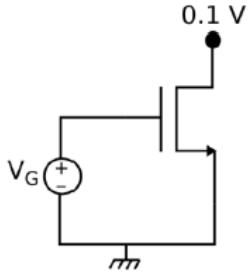
- D: drain, S: source, G: gate, and B: bulk.
- Symmetric structure.
- $L_{eff} = L - 2L_D$.
- The source provides charges and the drain collects them.
- PMOS structure is similar but sweeping the charge regions.



2. MOSFET devices

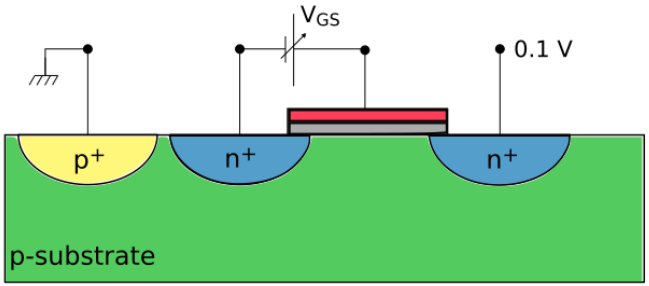
- Symbols:



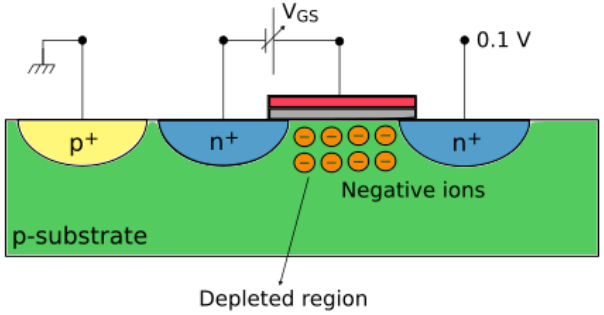


- Operating performance: starting with V_{GS} = 0V we increase it…

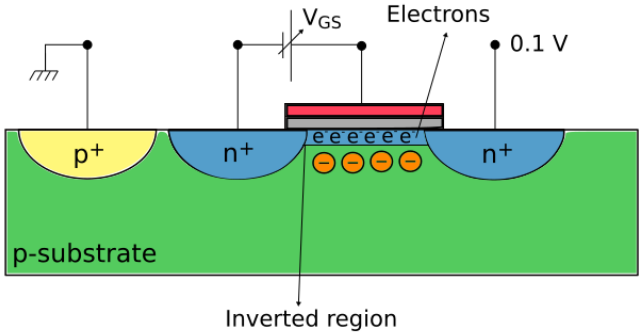
1) V_{GS} = 0V



2) 0V < V_{GS} < V_{TH}

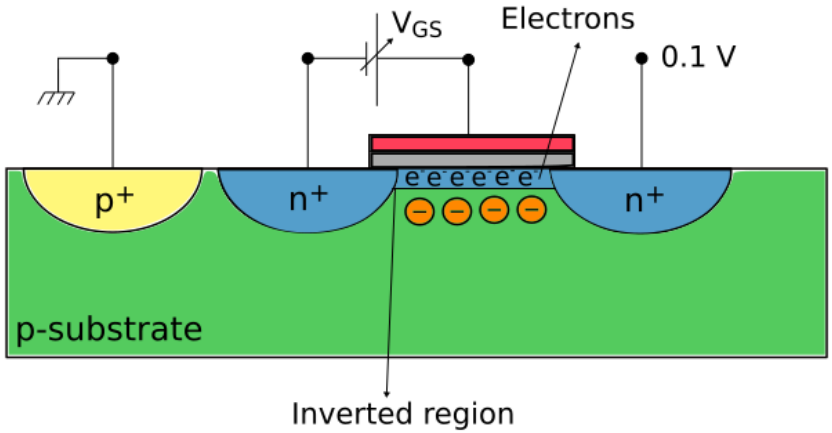


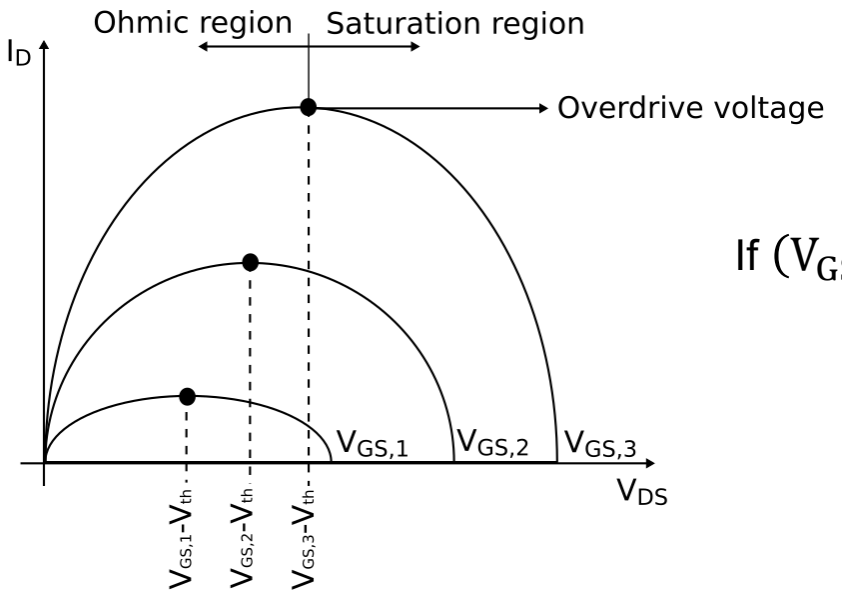
3) V_{GS} > V_{TH}



2. MOSFET devices

- Operating performance:





- Inverted region: a channel is created between D and S through the charges may flow.

$$I_D = C_{ox}\mu_n \frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\frac{\partial I_D}{\partial V_{DS}} = C_{ox}\mu_n \frac{W}{L}(V_{GS} - V_{th} - V_{DS}) = 0$$

$$V_{DS} = V_{GS} - V_{th}$$

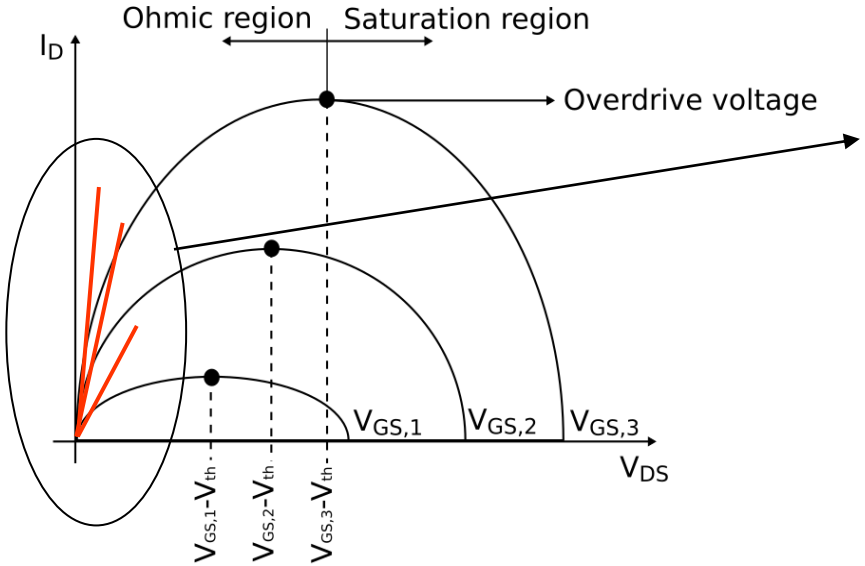
If $(V_{GS} - V_{th})V_{DS} \gg {}^1/_2\, V_{DS}^2$

$$I_D \approx C_{ox}\mu_n \frac{W}{L}(V_{GS} - V_{th})V_{DS}$$

Linear/ohmic region

2. MOSFET devices

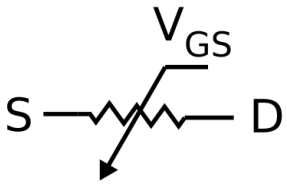
- Operating performance:



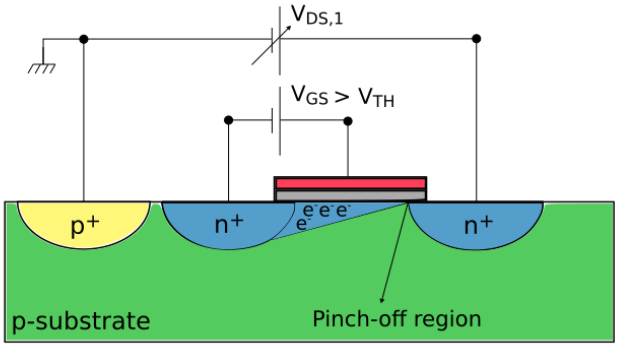
$$(V_{GS} - V_{th})V_{DS} \gg {}^1/_2\, V_{DS}^2$$

is accomplished especially for low V_{DS}.

- A transistor may work as a voltage-controlled resistor.

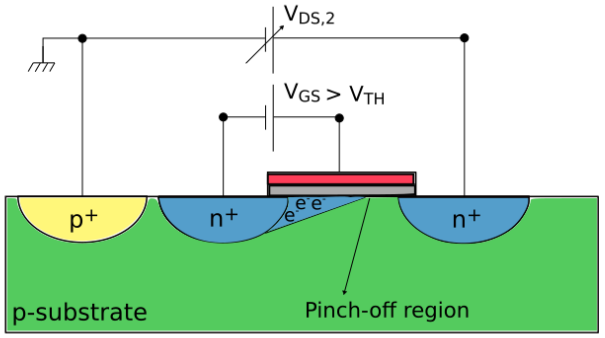


Now we keep $V_{GS}>V_{th}$ and increase V_{DS}…



Inverted region

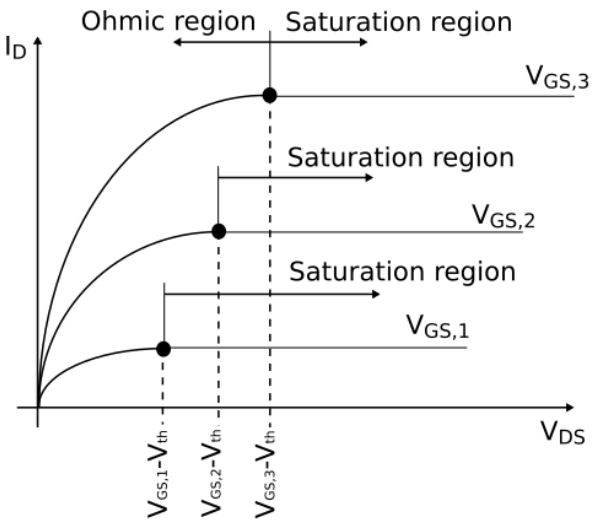
$V_{DS,2} > V_{DS,1}$



Inverted region

2. MOSFET devices

- … we get into the **saturation region**.



$$I_D = C_{ox}\mu_n \frac{W}{2L}(V_{GS} - V_{th})^2$$

- **Ideally**, the current does not depend on V_{DS}.
- The transistor operates as a voltage-controlled current source.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = C_{ox}\mu_n \frac{W}{L}(V_{GS} - V_{th}) = \sqrt{2C_{ox}\mu_n \frac{W}{L} I_D}$$

C_{ox}: oxide capacitance

$\varepsilon_o = 8{,}85\text{aF/um}$:vacuum dielectric constant

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3{,}97\varepsilon_o}{t_{ox}}$$

t_{ox} :oxide thickness (node dependent)

μ_n, μ_n :effective mobility of charge carriers

$$\mu_n = 660\ \frac{cm^2}{V \cdot s} \qquad \mu_p = 210\ \frac{cm^2}{V \cdot s}$$

⟶ **g_m in NMOS higher than in PMOS**

2. MOSFET devices

- Second order effects:
  - **Body effect:** Which should be the bulk voltage?

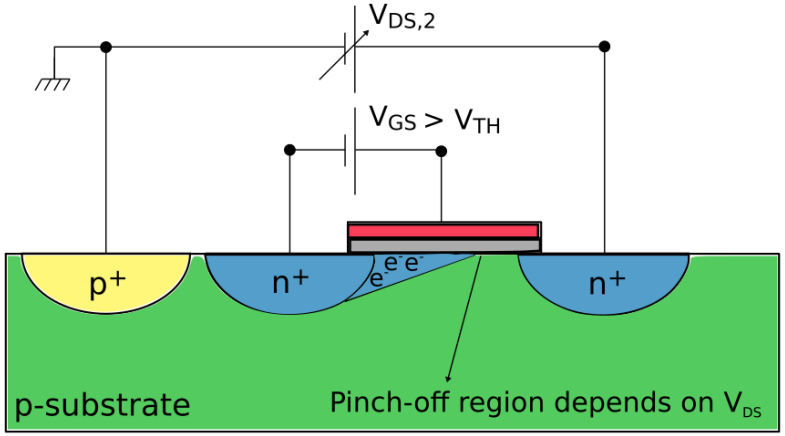
Bulk voltage modifies V_{th}.

$$V_{th} = V_{tho} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

Node dependent

γ between 0.3 y 0.4 $V^{1/2}$

  - **Channel modulation:** due to I_D-V_{DS} dependence.



Inverted region

$$I_D = C_{ox}\mu_n \frac{W}{2L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

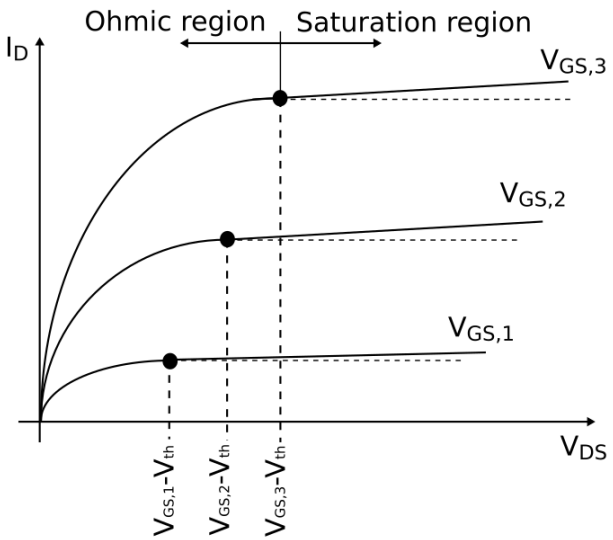
Channel modulation coefficient, it represents the relative variation of the channel length when V_{DS} increases:

- L high (250 nm) → λ high.
- L low (40nm) → λ low.

$$\lambda \propto 1/L$$

2. MOSFET devices

- Second order effects:
  - **Channel modulation:**



$$g_m = \frac{\partial I_D}{\partial V_{GS}} = C_{ox}\mu_n \frac{W}{L}(V_{GS} - V_{th})(1 + \lambda V_{DS})$$

$$= \sqrt{2C_{ox}\mu_n \frac{W}{L} I_D (1 + \lambda V_{DS})}$$

An additional term is added to g_m.

- **Subthreshold region, Weak inversion:**
  - If $V_{GS}<V_{th}$ → weak depleted region → small current proportional to V_{GS} flows.
  - If $V_{DS}>200$ mV, current follows an exponential function:

$$I_D \approx I_{D0} \frac{W}{L} e^{V_{GS}/n(kT/q)}$$

I_{D0} depends on the process

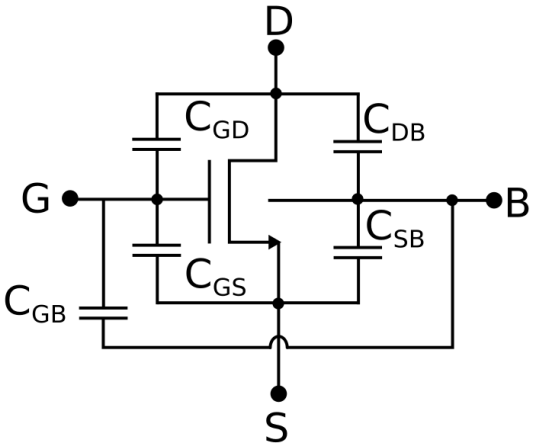
$1 < n < 3$

$$g_m = \frac{I_D}{n(kT/q)}$$

g_m higher than in saturation!!

2. MOSFET devices

- Internal capacitances:



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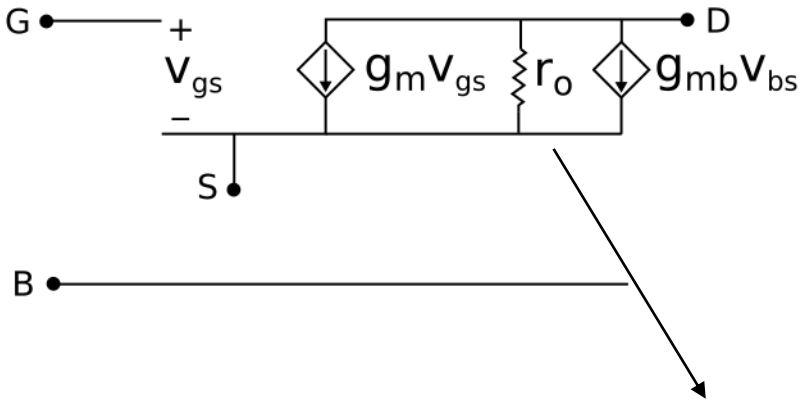
Capacitances depend on the operating region.

Capacitance	Off	Linear	Saturation
C_{GS}	C_{ov}·W	**0,5·C_{ox}·W·L**	**(2/3)·C_{ox}·W·L**
C_{GD}	C_{ov}·W	**0,5·C_{ox}·W·L**	**C_{ov}·W**
C_{GB}	C_{ox}·W·L	CGBO·L	CGBO·L
C_{DB}	C_{jd}	C_{jd}	C_{jd}
C_{SB}	C_{js}	C_{js}	C_{js}

2. MOSFET devices

- Small signal model in saturation:



Body-effect

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m$$

Increasing V_{BS} is equivalent to increasing V_{GS}.

Resistance due to channel modulation.

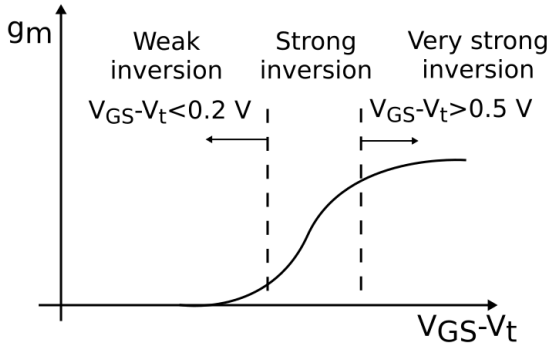
$$r_o = \frac{\partial V_{DS}}{\partial I_D} \approx \frac{1}{\lambda I_D} = \frac{2L}{\lambda C_{ox} \mu_n W V_{DS,sat}{}^2} \qquad \lambda \propto \frac{1}{L} \qquad \boxed{r_o \propto \frac{L^2}{V_{DS,sat}{}^2}}$$

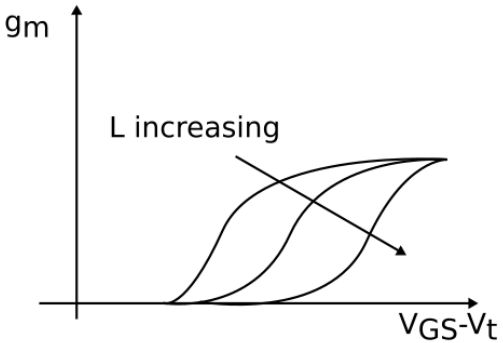
Voltage gain: $A_V = -g_m r_o = -\frac{2}{\lambda (V_{GS} - V_T)}$ (no body-effect included)

For frequency response analysis we would need to include internal capacitances.

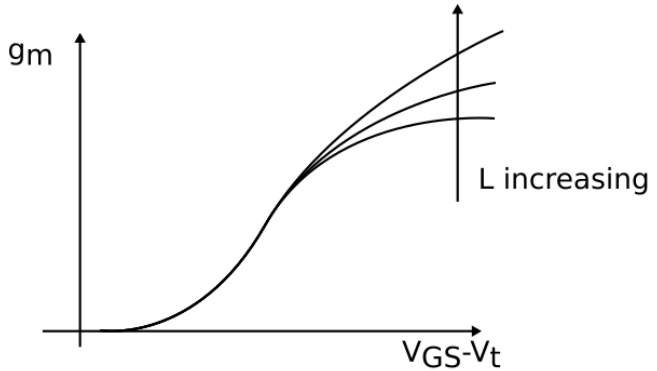
2. MOSFET devices

- Operating regions:





W kept constant



W/L kept constant

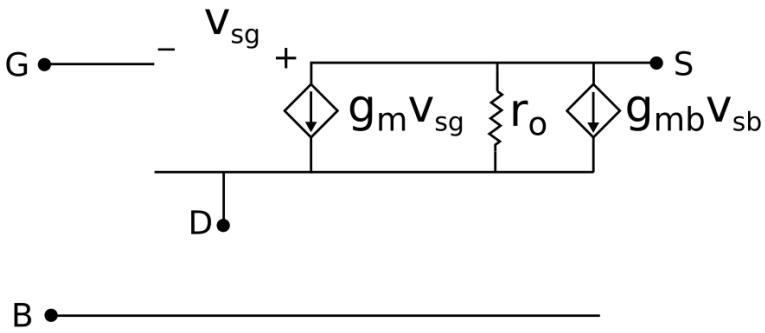
Weak inversion	$I_{DS} = I_{D0}\frac{W}{L}e^{\left(\frac{V_{GS}}{nkT/q}\right)}$	$g_m = \frac{I_{DS}}{nkT/q}$
Strong inversion	$I_{DS} = k'_x\frac{W}{L}(V_{GS} - V_T)^2$	$g_m = \frac{2 \cdot I_{DS}}{V_{GS} - V_T}$
Very strong inversion	$I_{DS} = WC_{OX}V_{SAT}(V_{GS} - V_T)$	$g_m = \frac{I_{DS}}{V_{GS} - V_T}$

2. MOSFET devices

- PMOS:
  - All the phenomena previously described apply similar in PMOS.
  - All the equations remain modifying the polarity of the voltages/currents and considering that the current is due to positive charges.

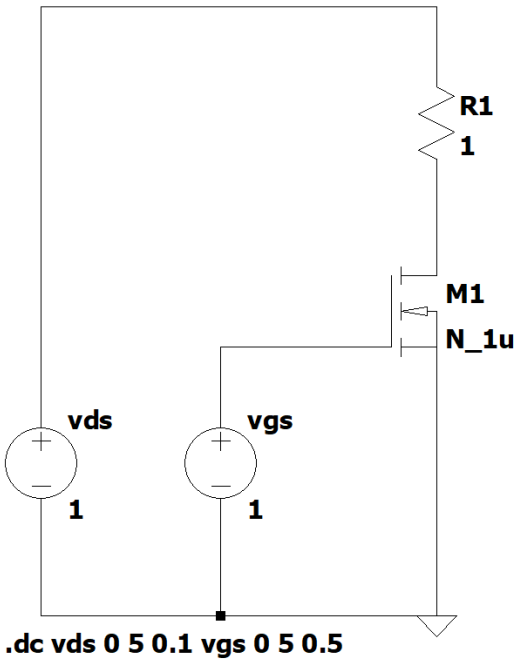
$$I_D = C_{ox}\mu_p \frac{W}{2L}(V_{SG} - |V_{th}|)^2(1 + \lambda V_{SD})$$

$$I_D \approx I_{D0}\frac{W}{L}e^{V_{SG}/n(kT/q)}$$

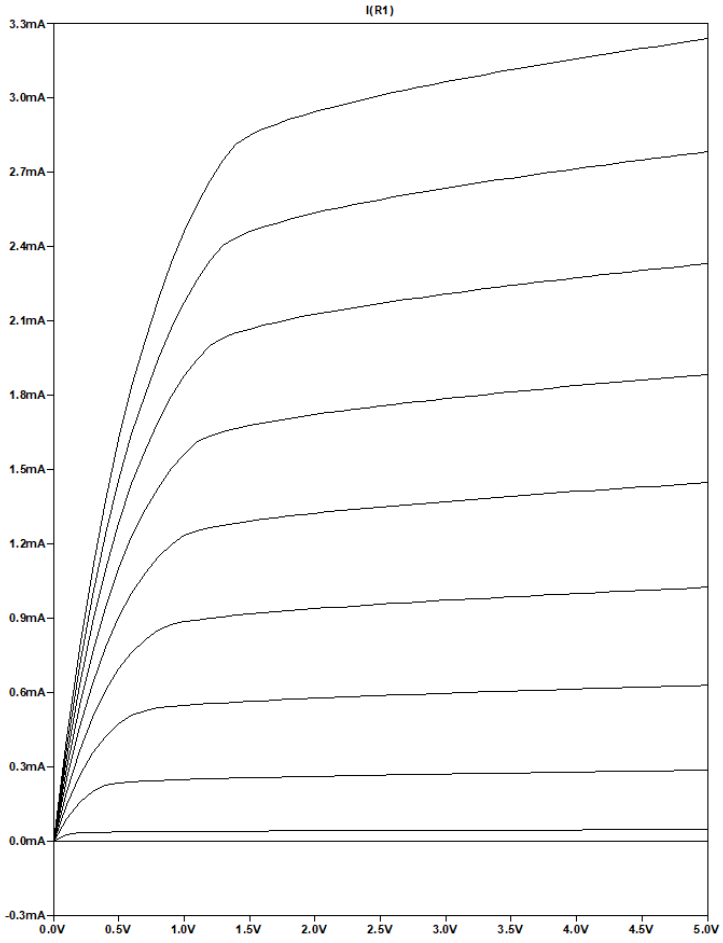


3. Features extraction

- Simulations performed in LTSpice: 1um node.



W = 10 u
L = 1 u

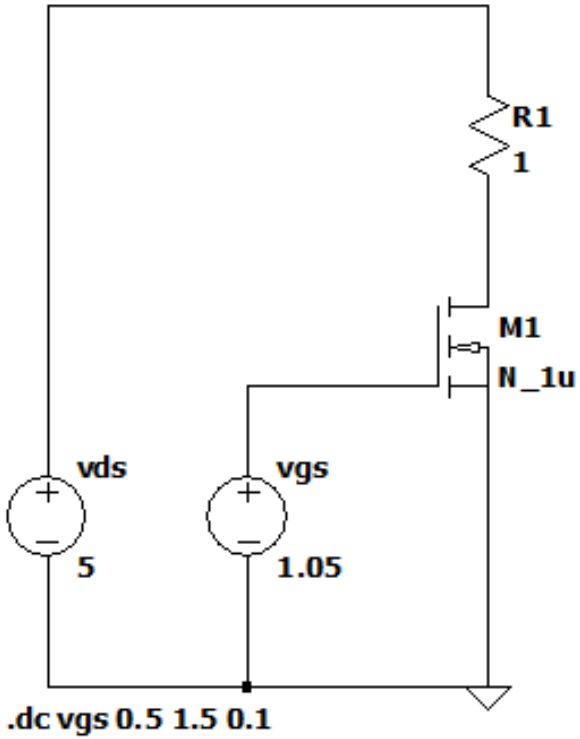


Low channel modulation

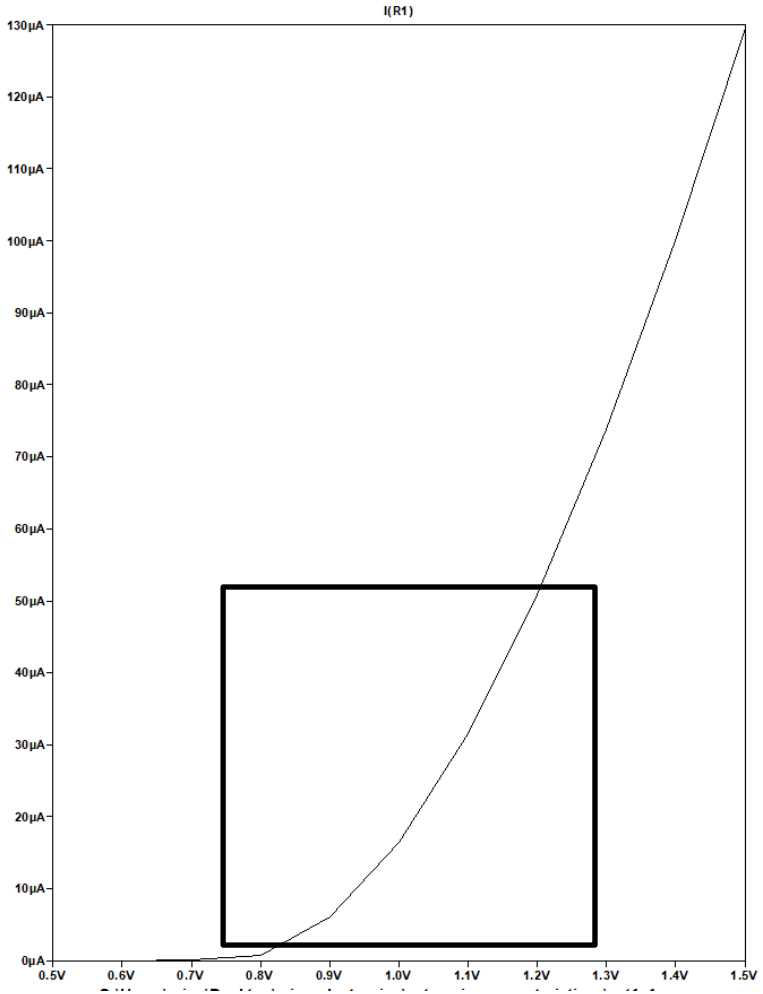
$\lambda_n = 0.01\ V^{-1}$

3. Features extraction

- Simulations performed in LTSpice: 1um node.



W = 10 u
L = 2 u



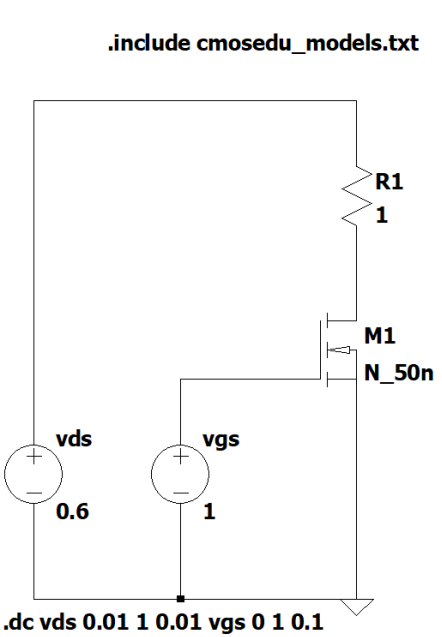
$$I_D = C_{ox}\mu_n \frac{W}{2L}(V_{GS} - V_{th})^2$$

$V_{th} = 0.75\ V$ $C_{ox}\mu_n = 100\ uA/V^2$

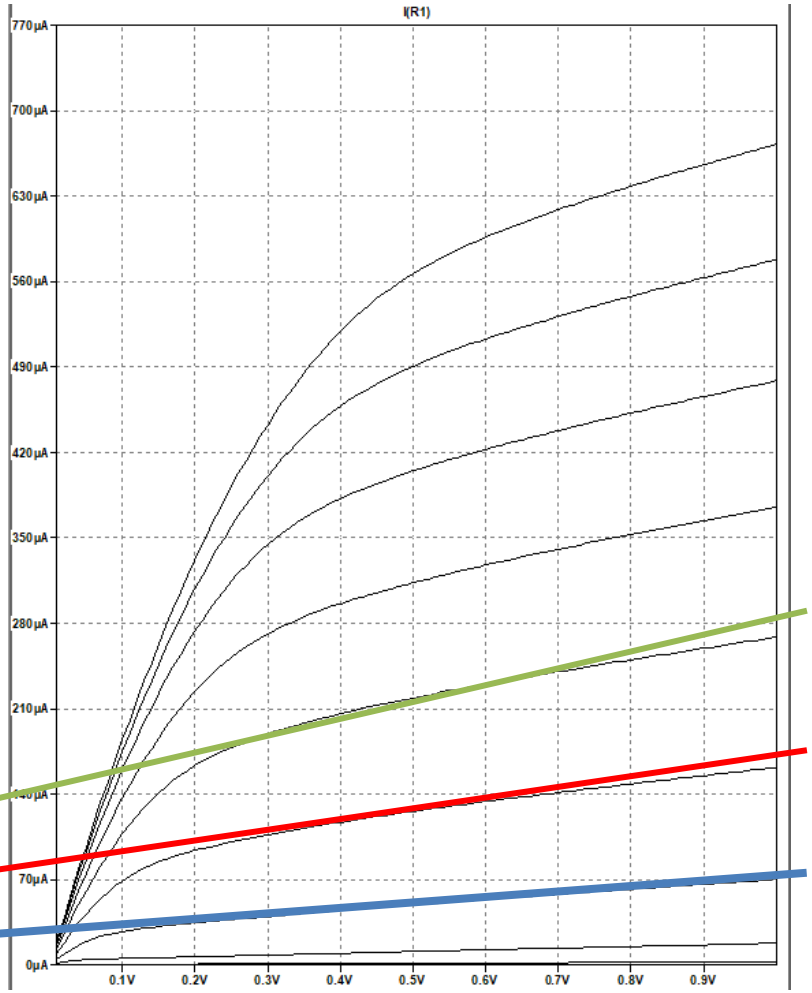
3. Features extraction

- Simulations performed in LTSpice:

What about if we use a narrow process? → L = 50 nm

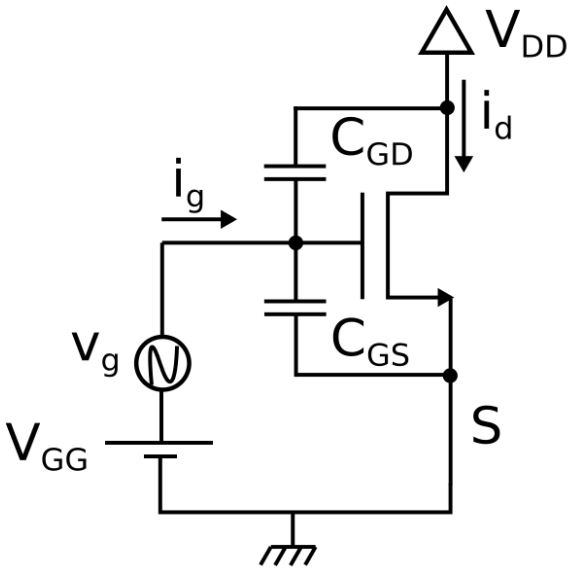


W = 1 u
L = 50 nm



$V_A \approx -1{,}5V \rightarrow \lambda_n = 0.67\ V^{-1}$

4. Transistor bandwidth (BW)



$$\frac{i_d}{i_g} = \frac{g_m}{2\pi f(C_{GS} + C_{GD})}$$

$$\text{GBW} \approx \frac{3\mu_n V_{DS,sat}}{4\pi L^2}$$

- The lower L, the faster the device and the lower the output resistance.
- $V_{DS,sat}$ high → they are faster but the get into the linear region easily.
- NMOS faster than PMOS.

- Short channel devices

$$\text{GBW} \propto \frac{V_{DS,sat}}{L}$$

- Switching frequency

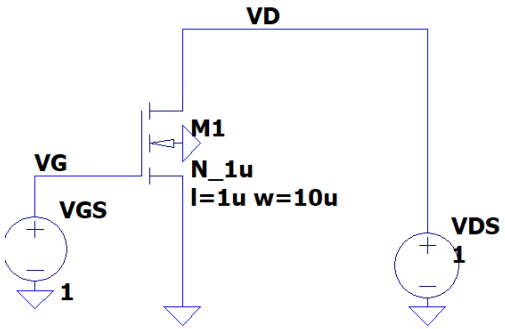
$$f_T \propto \frac{V_{GS} - V_T}{L^2}$$

- L_{min} > 100 nm → high gain.
- L_{min} < 100 nm → high speed.

5. General tips for analog design

- Trade-off between bandwidth and gain → $L \geq 2L_{min}$.
- Rule of thumb → $V_{DS,sat}$ = 5% of V_{DD}.
- The real performance of transistors is more complex than the behavior described by equations. In general a designer uses equations to propose a first design to be refined afterwards by simulations.
  - The equations provide more accurate results for large technologies.
  - For low voltage and narrow technologies (< 50nm) the equations are more complex.
- CAD tools are used extensively.

➢ CMOS device (long channel)

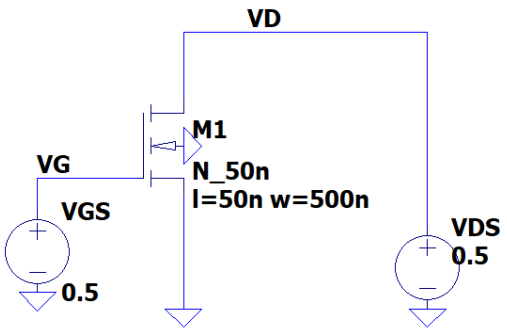


Ids: 31.7 uA
Vth: 822 mV
Vdsat: 187 mV
Gm: 248 uA/V
Gds: 4.6 uA/V

$$\frac{Gm}{Ids} = 7.8$$

$$Rout = \frac{1}{Gds} = 217k\Omega$$

➢ CMOS device (short channel)



Ids: 53.8 uA
Vth: 348 mV
Vdsat: 149 mV
Gm: 407 uA/V
Gds: 28 uA/V

$$\frac{Gm}{Ids} = 7.5$$

$$Rout = \frac{1}{Gds} = 36k\Omega$$

Bibliography

- Allen, P. E., & Holberg, D. R. (2002). CMOS analog circuit design. New York: Oxford University Press.
- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Simulations are performed through software LTSPice, provided courtesy of Analog Devices and authored by Mike Engelhardt.

Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.