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Unit 3. Analog CMOS fundamental circuits

System-on-Chip and efficient electronic circuit integration techniques

Carlos III University of Madrid, Spain

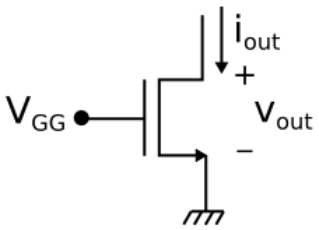
Electronics Technology Department

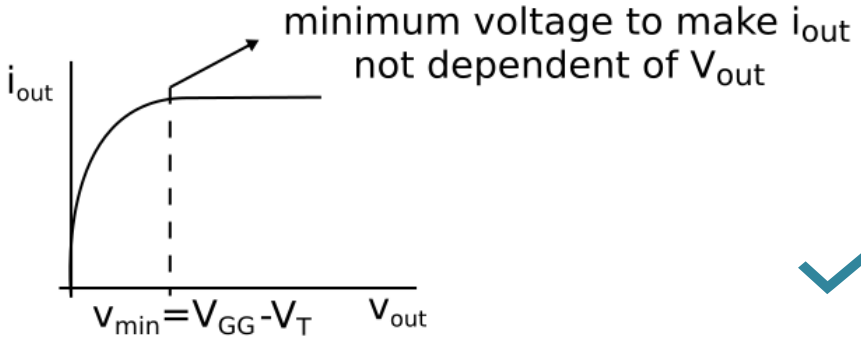
Outline

1. Current sinks/sources
2. Current mirrors
3. Examples of current mirrors
4. Switches and active resistors
5. References of currents and voltages

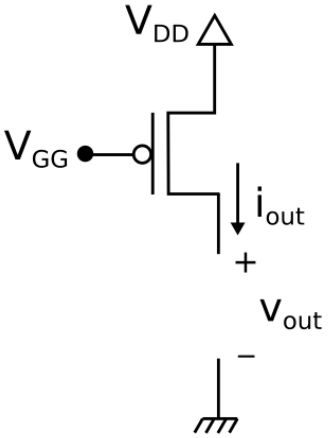
1. Current sinks/sources

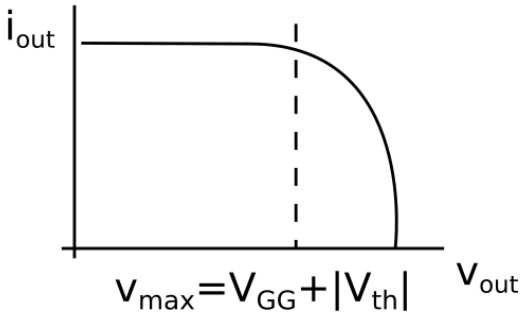
- Current sink





- Current source





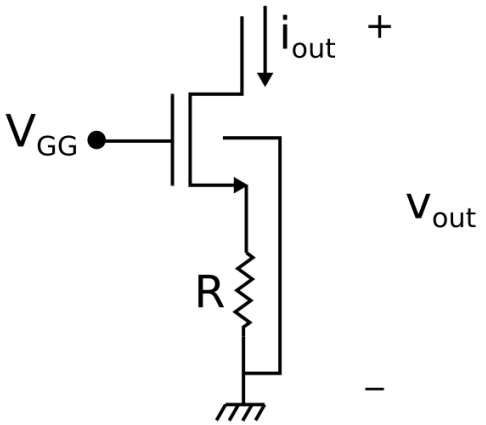
✓ Simple designs

✗ $r_{out} = \frac{1}{\lambda I_D}$ → channel modulation

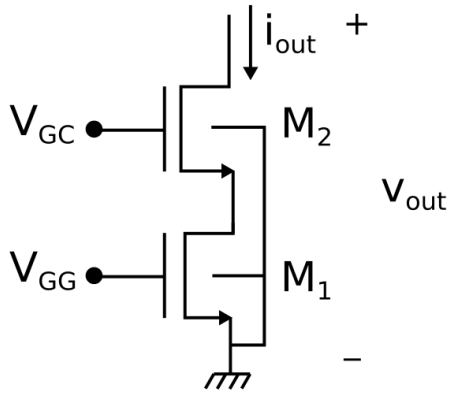
✗ Reducing v_{min} (current sink) and increasing V_{max} are required

1. Current sinks/sources

- How to increase the output resistance?



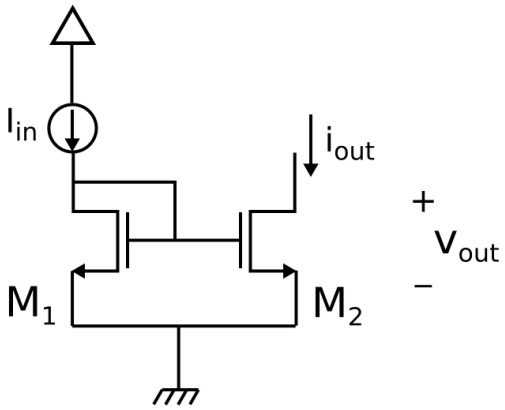
$$r_{out} \approx g_m r_{ds} R$$



$$r_{out} \approx g_{m2} r_{ds2} r_{ds1}$$

2. Current mirrors

- Basic structure:



$$i_{out} = \frac{W/L|_{M2}}{W/L|_{M1}} I_{in} \qquad r_{out} = r_{ds2}$$

  - A current mirror takes the current from one branch (I_{in}) and copies it into the other one (i_{out}) considering the size ratio between M_1 and M_2.

- Error sources in the ratio iout/Iin:
  - Channel modulation:

$$\frac{i_{out}}{I_{in}} = \frac{W/L|_{M2}}{W/L|_{M1}} \cdot \boxed{\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}}$$

Different V_{DS} will suppose different current ratio

  - Short channel devices → higher error.

Solution? → **Increasing r_{out}.**

2. Current mirrors

- Error sources in the ratio i_{out}/I_{in}:
  - V_T variation:
    - Two devices placed close in layout → maximum V_T variation of 10 mV.
    - Oxide gradients may suppose variations in the μC_{ox} product.

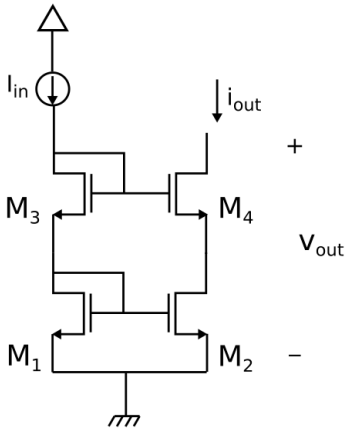
$$\frac{i_{out}}{I_{in}} = \frac{W/L|_{M2}}{W/L|_{M1}} \cdot \boxed{\left(\frac{V_{GS} - V_{th2}}{V_{GS} - V_{th1}}\right)^2}$$ Error term

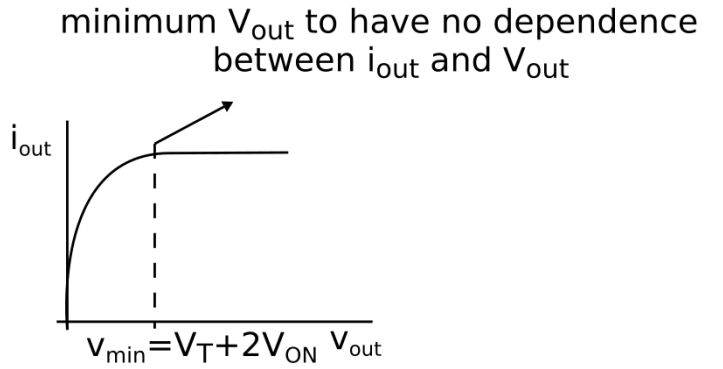
    - The higher the current I_{in} the lower the error.

  - Aspect ratio between the devices in layout:
    - For W and L > 10 μm → error negligible.
    - Symmetric designs interleaving devices minimize differences in the aspect ratio.

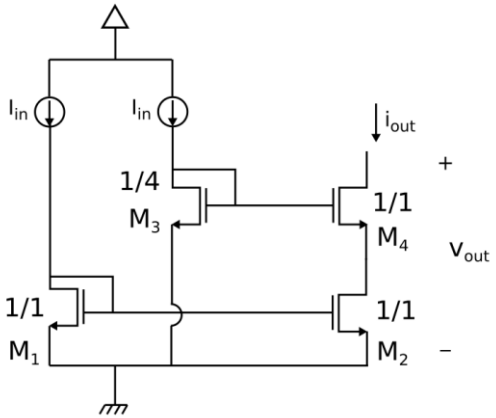
2. Current mirrors

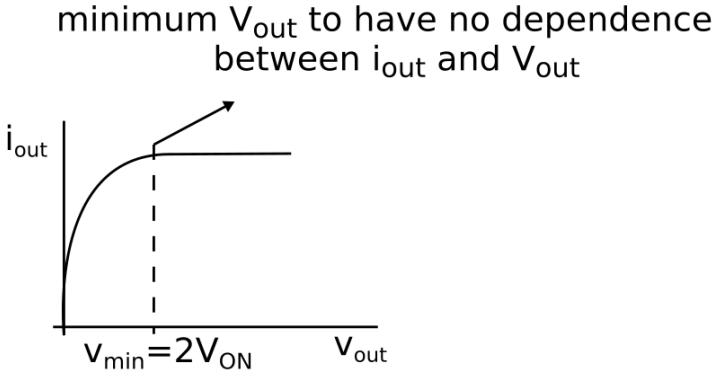
- How to increase the output resistance?
  - Current mirror with cascode: $r_{out} = r_{ds2} + r_{ds4} + g_{m4} r_{ds4} r_{ds2}$





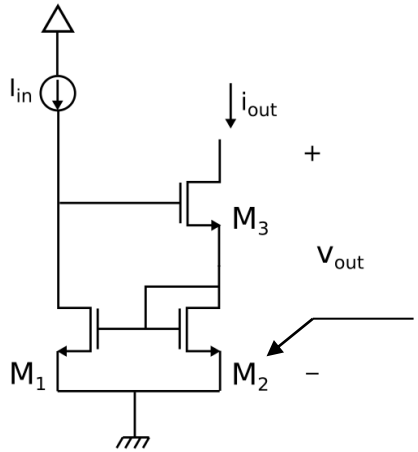
  - Current mirror with cascode and higher V_{out} variation possible:





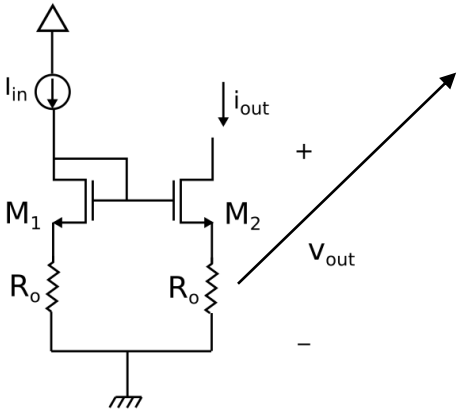
2. Current mirrors

- How to increase the output resistance?
  - Wilson current mirror: $$r_{out} \approx r_{ds3} + r_{ds2}\frac{1 + r_{ds3}g_{m3} + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}}$$



$$r_{M2} = \frac{r_{ds2}}{1 + g_{m2}r_{ds2}}$$

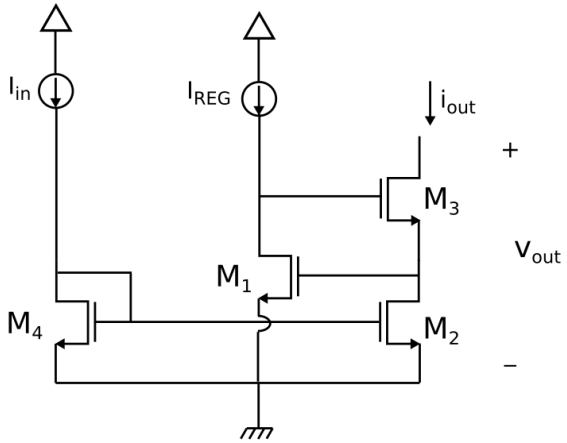
  - Degenerated current mirror: $r_{out} \approx g_{m2}r_{ds2}R_o$



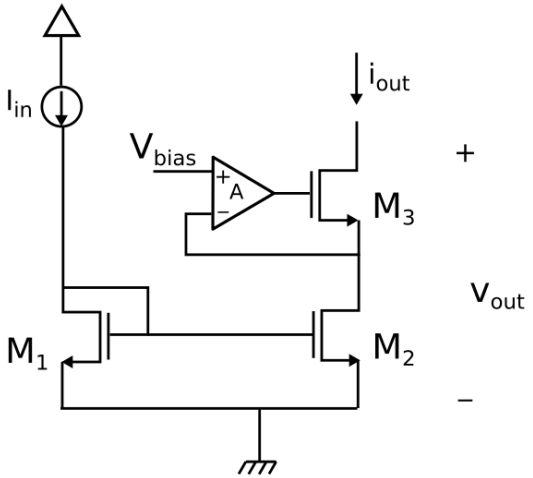
Higher output swing because we have one single device at the output stage.

2. Current mirrors

- Regulated current mirror:



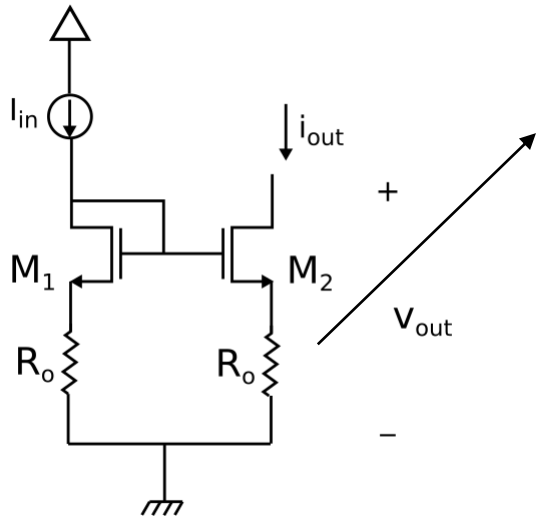
$$r_{out} \approx g_{m1} g_{m3} r_{ds1} r_{ds2} r_{ds3}$$



$$r_{out} \approx g_{m3}(1 + A) r_{ds3} r_{ds2}$$

2. Current mirrors

- Degenerated current mirror: $r_{out} \approx g_{m2} r_{ds2} R_o$

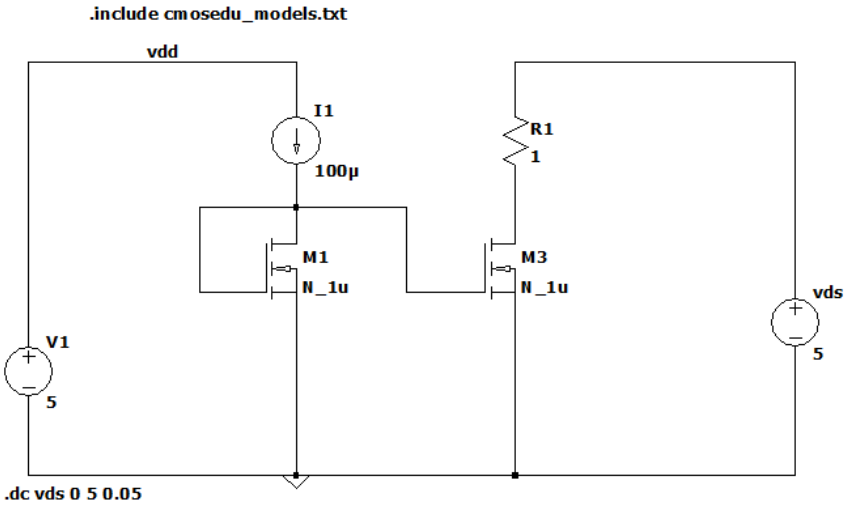


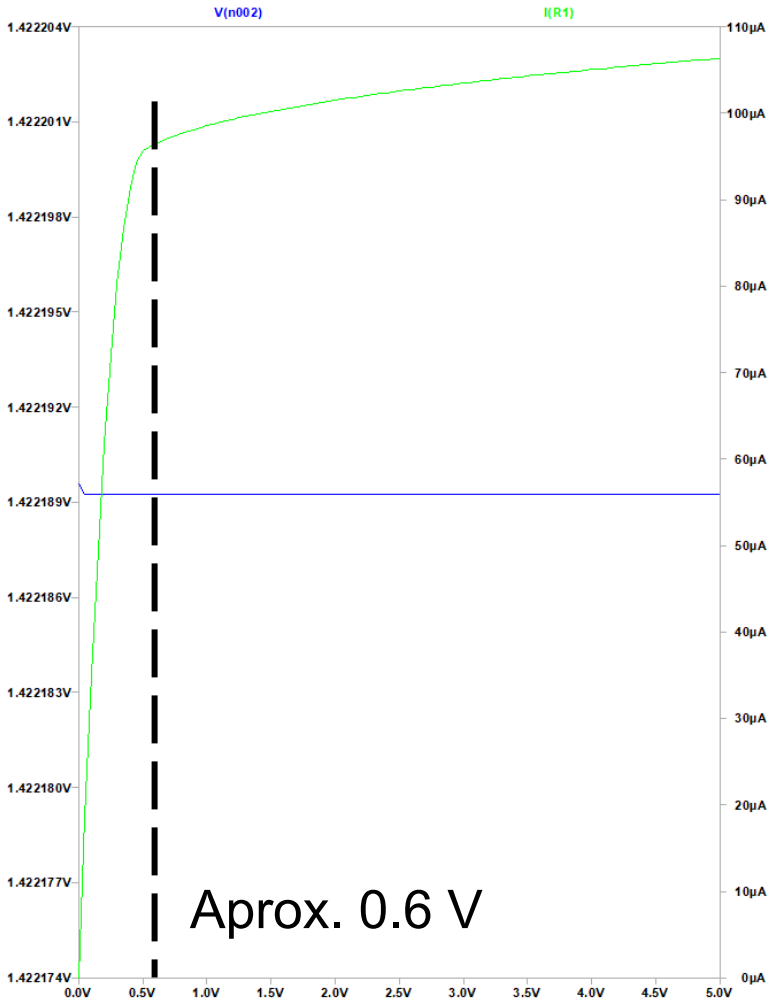
Higher output swing because we have one single device at the output stage.

Tips for current mirror design:

- Increasing output resistance r_{out}.
- The higher the current the less error due to VT.
- The bigger the devices the less error due to aspect ratio.
- Longer L → less error due to channel modulation.
- To minimize the error due to VT → multiple W/L aspect ratios.
- Symmetric layout designs.

3. Examples of current mirrors

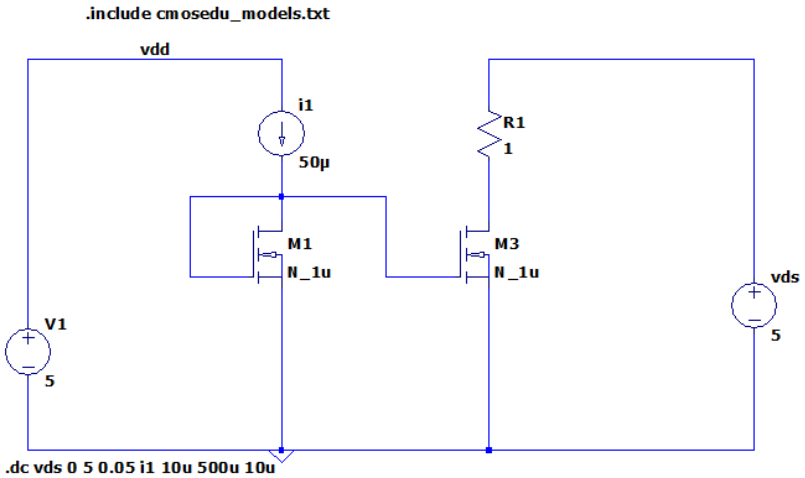


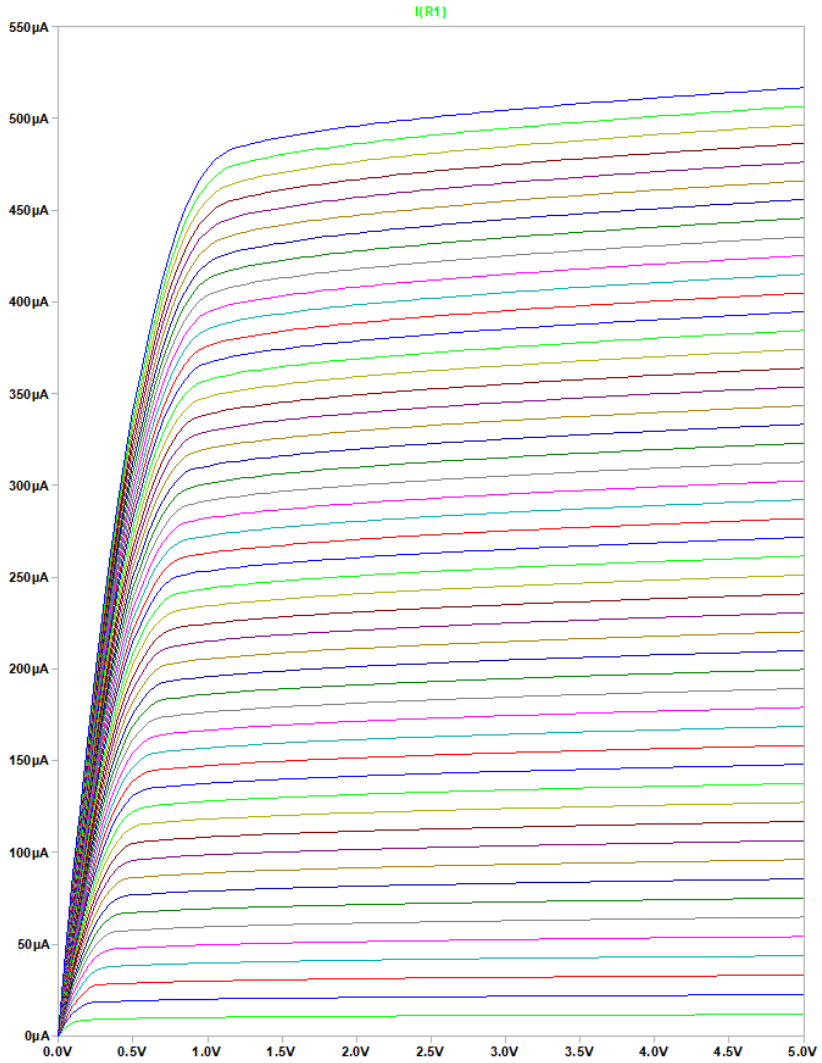


V_{GS} = 1.42 V, V_T = 0.8V

$V_{min} = V_{ON}$ = 1.42 – 0.8 = 0.62 V

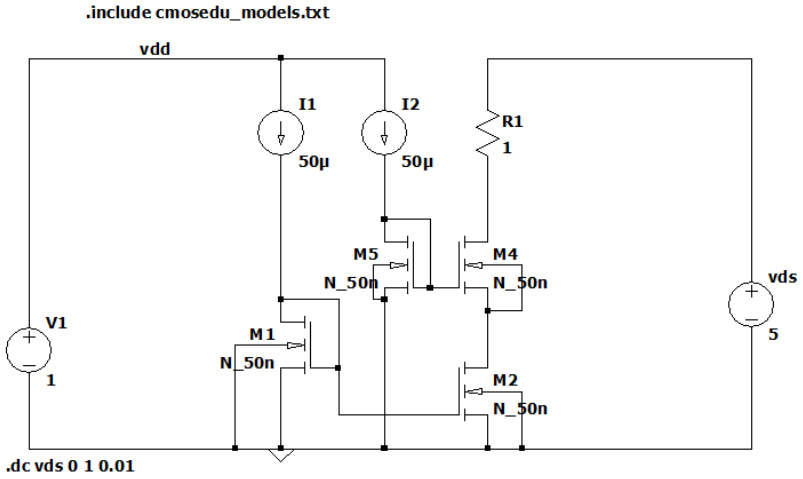
3. Examples of current mirrors

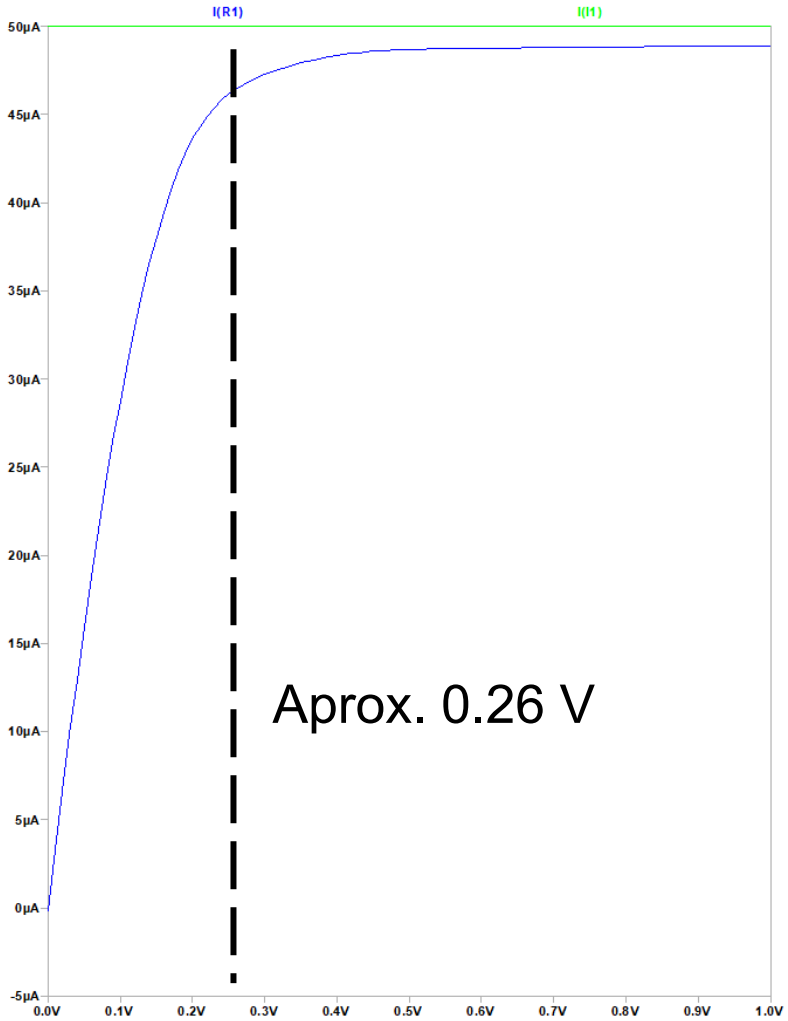




The lower the current the lower the required V_{ON}

3. Examples of current mirrors



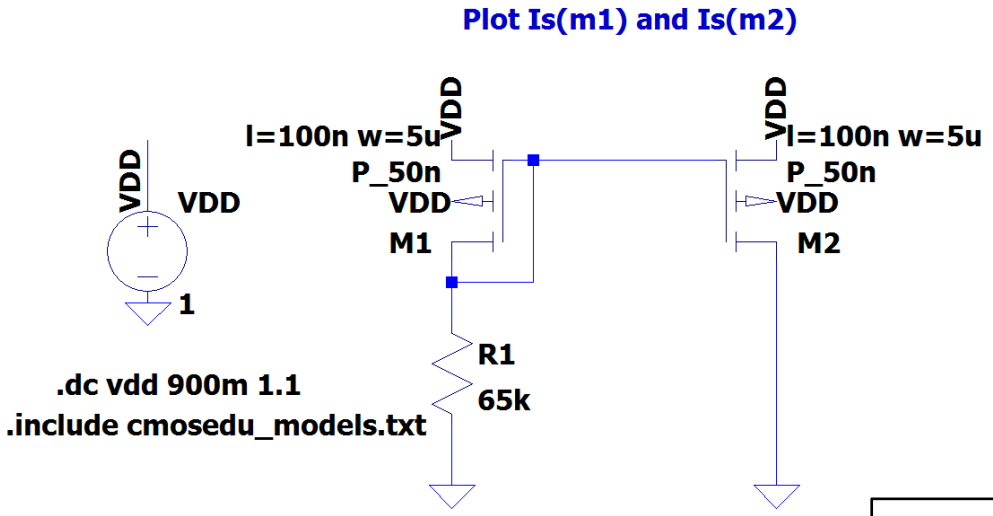


V_{GS} = 0.4 V, V_T = 0.28V

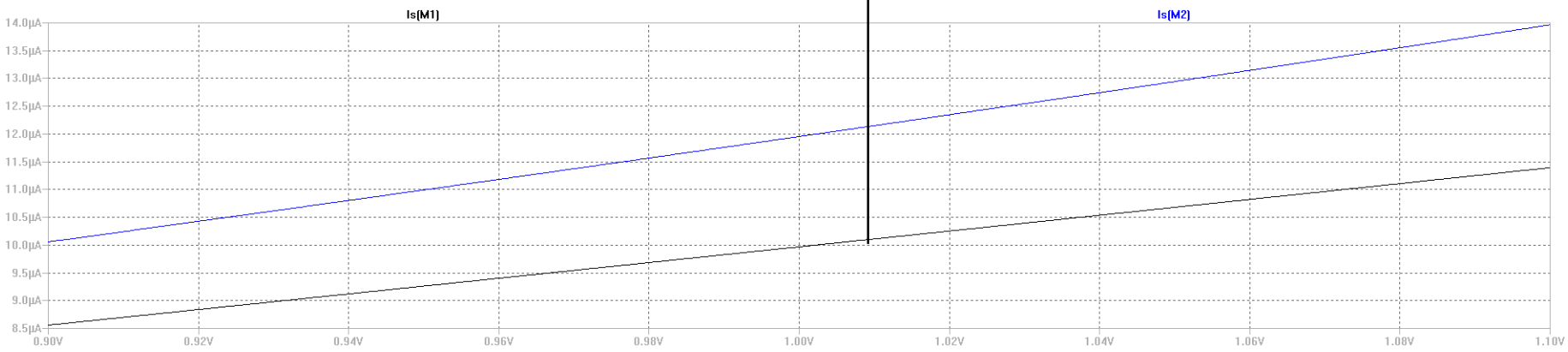
$V_{min} = 2*V_{ON}$ = 0.24 V

Aprox. 0.26 V

3. Examples of current mirrors

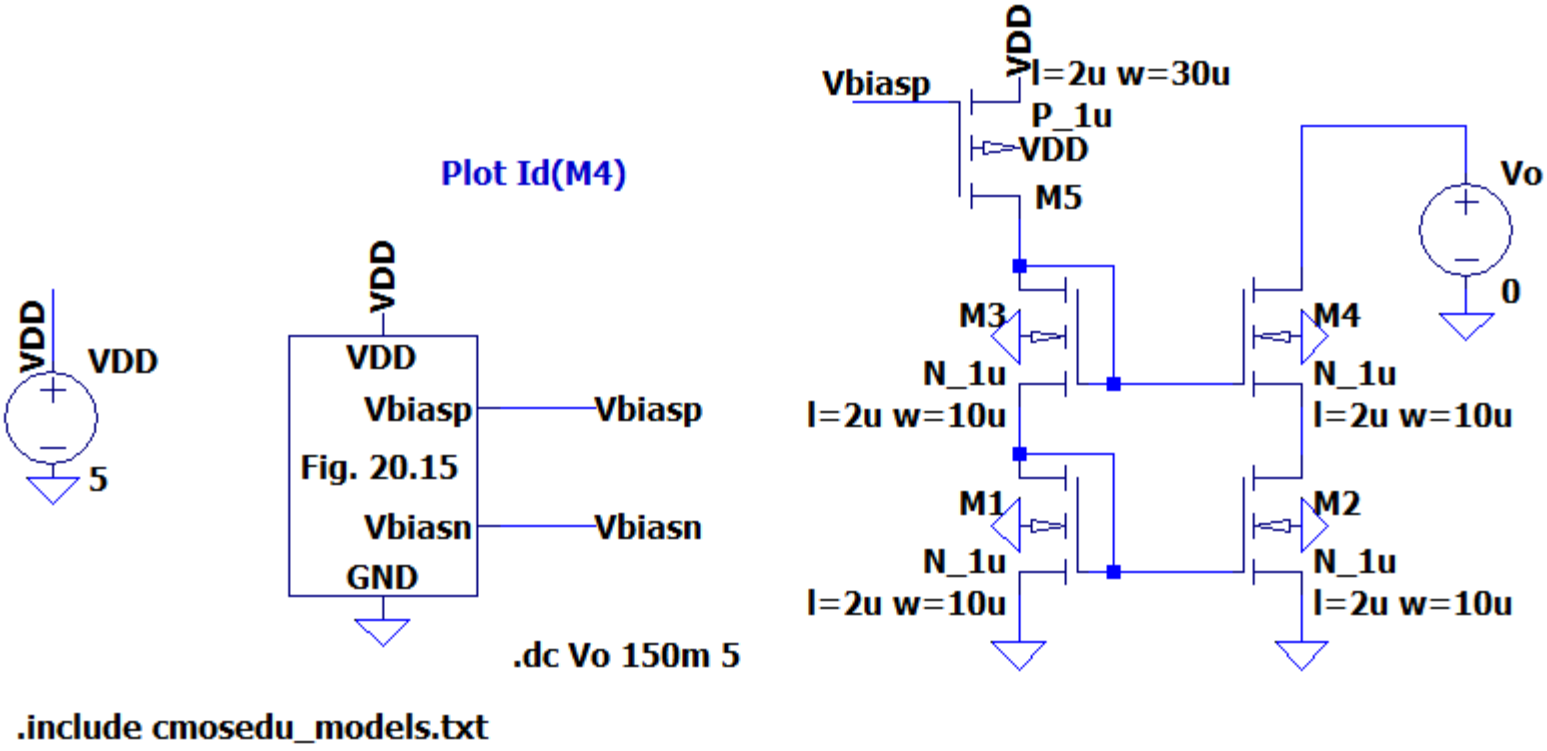


Error current due to channel modulation



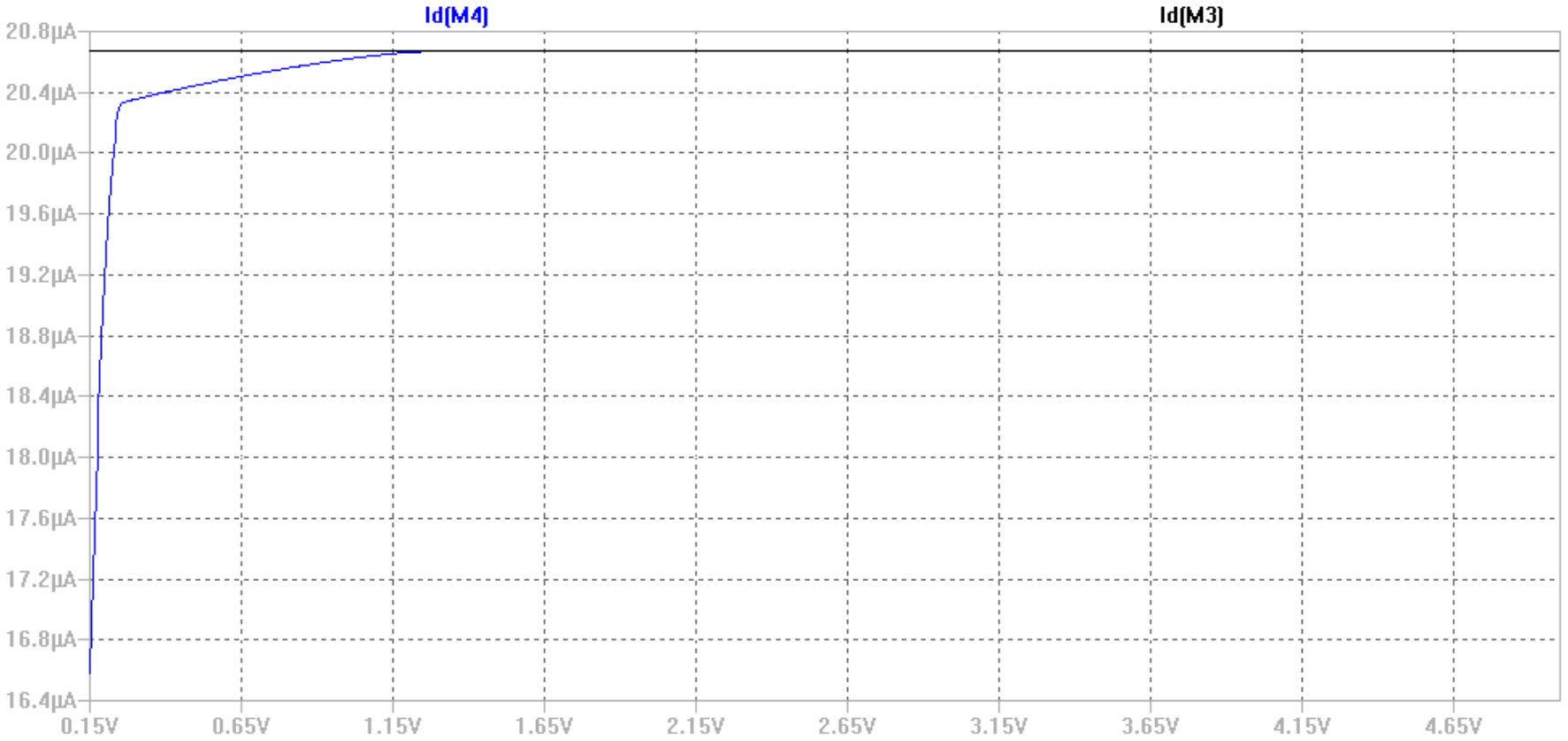
3. Examples of current mirrors

I_{ref}=20 μA



All transistors has the same size, and therefore the same V_T and $V_{DS,sat} \rightarrow V_{GSi}=V_{DS,sat}+V_T$
$V_{G3}=V_{G4}=V_{GS3}+V_{GS1}=2V_{DS,sat}+2V_T \rightarrow V_{DS2}=V_{G4}-V_{GS4}=V_{DS,sat}+V_T$ (V_T more than needed!!!)
The minimum V_o to set M4 in sat is: $V_{o,min}=V_{DS2}+V_{DS,sat}=2V_{DS,sat}+V_T=1.3V$

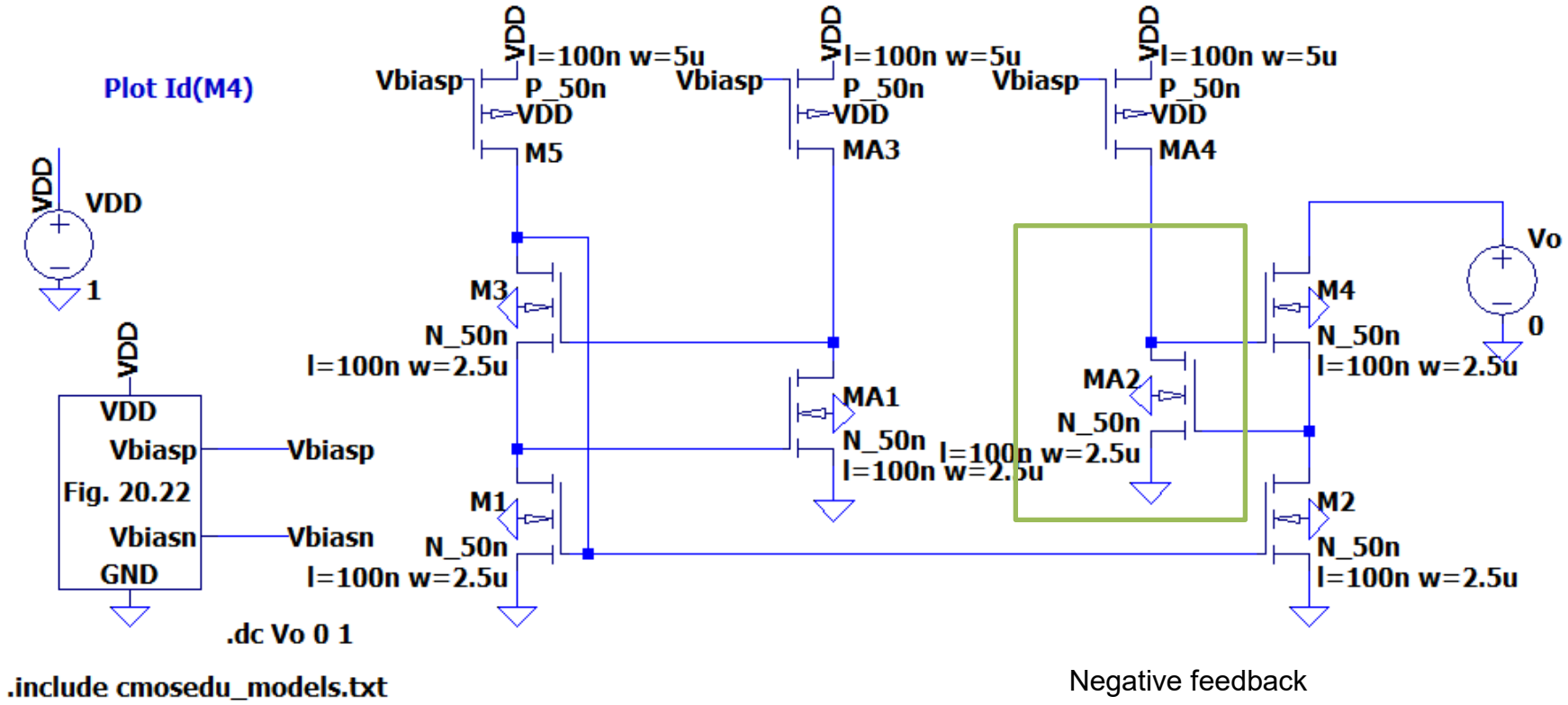
3. Examples of current mirrors



We need a minimum voltage of 1.3V!

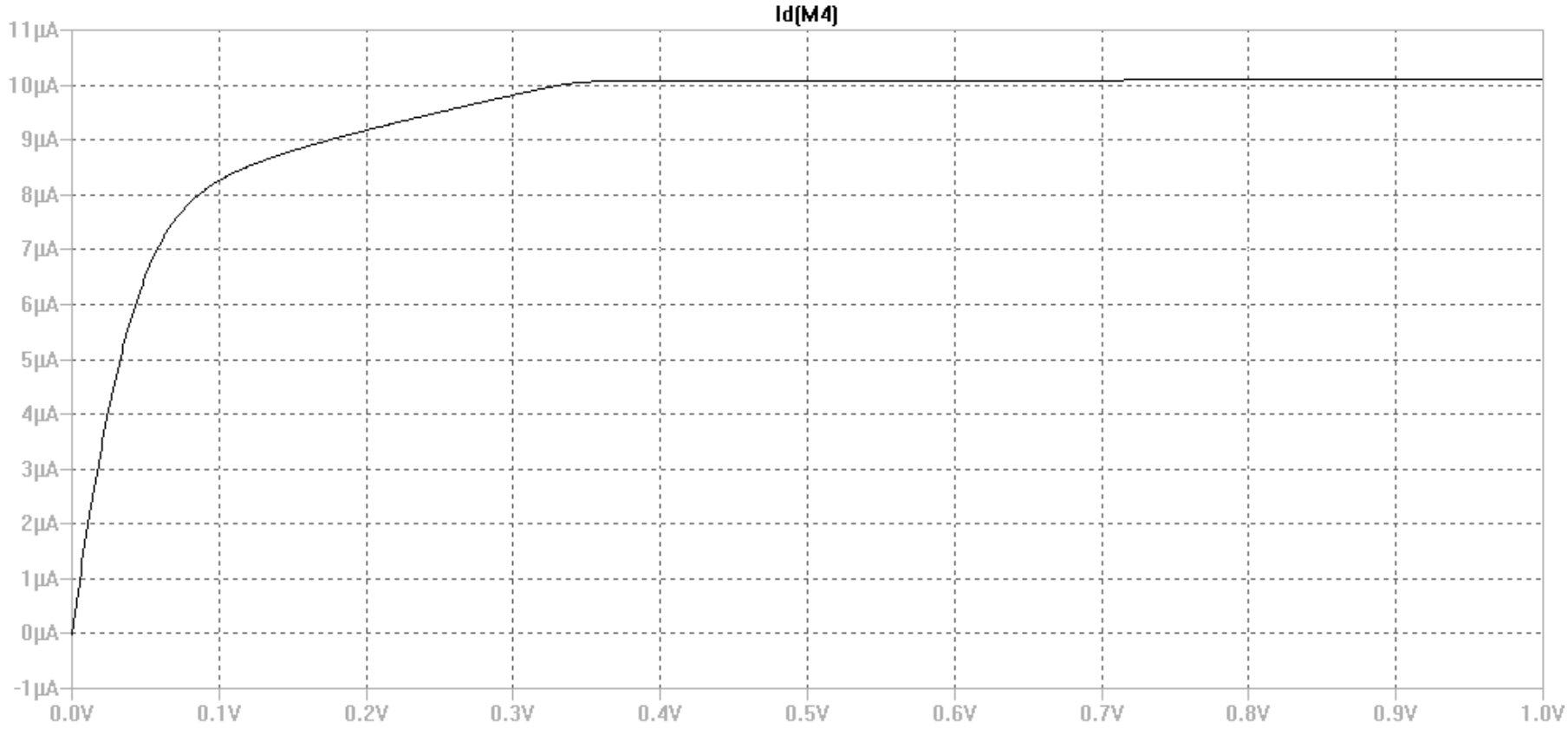
3. Examples of current mirrors

I_{ref}=10 μA All transistors are equally sized



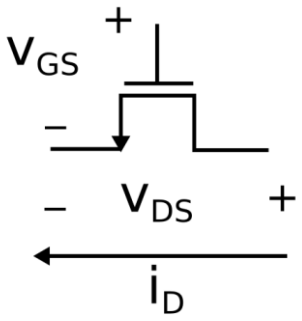
Negative feedback

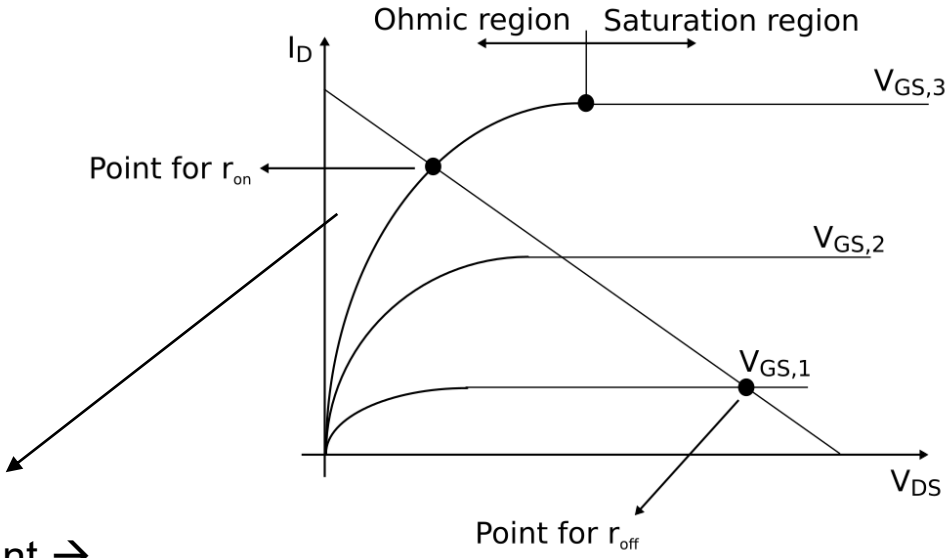
3. Examples of current mirrors



4. Switches and active resistors

- MOS devices can be used to implement switches





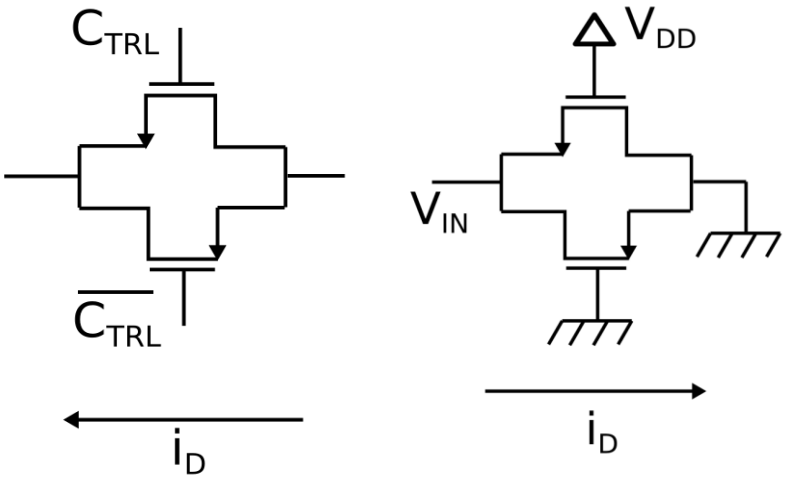
To ensure this operating point → $|V_{GS}|>>|V_{DS}|$

$$i_D = C_{ox}\mu_n \frac{W}{L}\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \rightarrow \quad r_{ON} = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{C_{ox}\mu_n \frac{W}{L}(V_{GS} - V_{th} - V_{DS})}$$

Variable R_{ON}

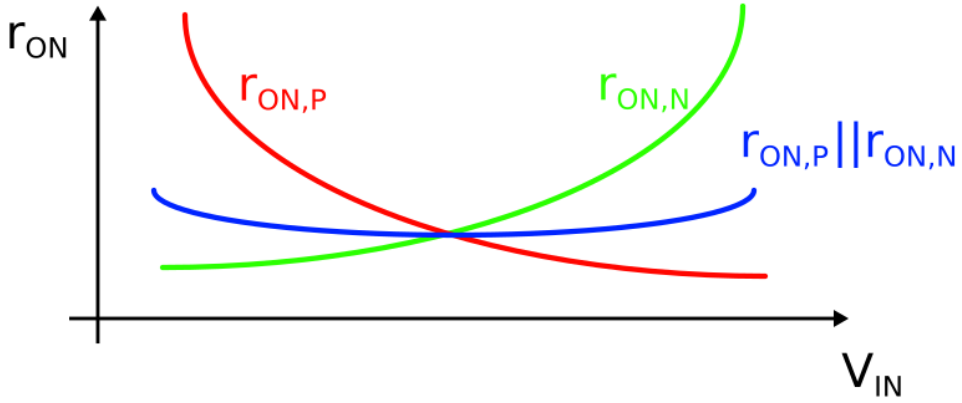
4. Switches and active resistors

- Enhanced version to increase analog dynamic range:



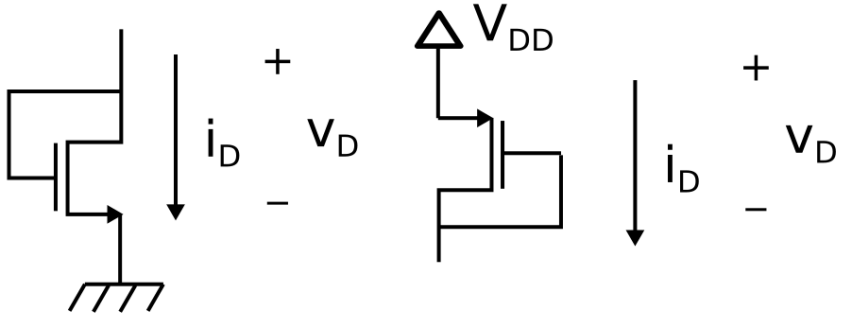
$$r_{ON,N} = \frac{1}{C_{ox}\mu_n \frac{W}{L}_N \left(V_{DD} - V_{th,n} - V_{IN}\right)}$$

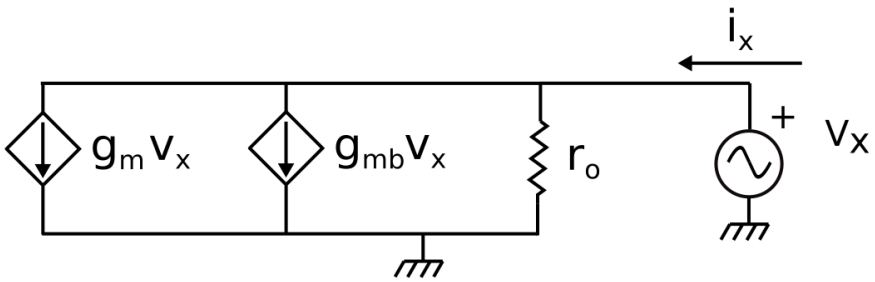
$$r_{ON,P} = \frac{1}{C_{ox}\mu_P \frac{W}{L}_P \left(V_{IN} - V_{th,p}\right)}$$



4. Switches and active resistors

- Active resistor: connecting the gate to the drain:



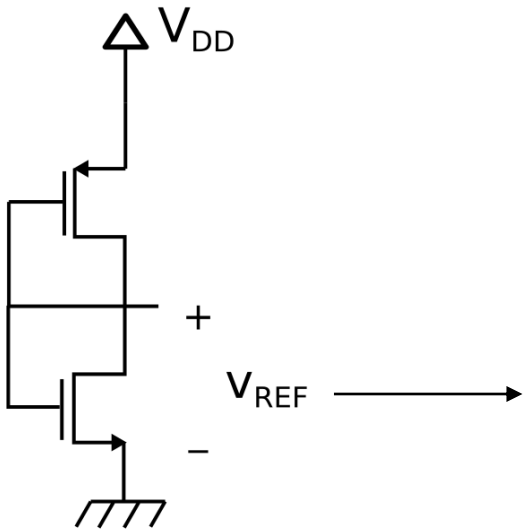


$$R_{eq} = \frac{1}{g_m + g_{mb} + {}^{1}/_{r_o}} \approx \frac{1}{g_m}$$

Non-linearity is mitigated by restricting V_{DS} variations.

5. Reference of currents and voltages

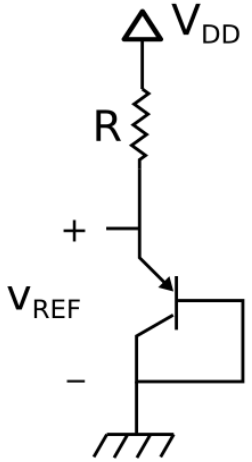
- Independent of power supply and temperature.



This voltage strongly depends on V_{DD} → not a good reference.

- How to improve it? → We may use the pn junction of a BJT device:

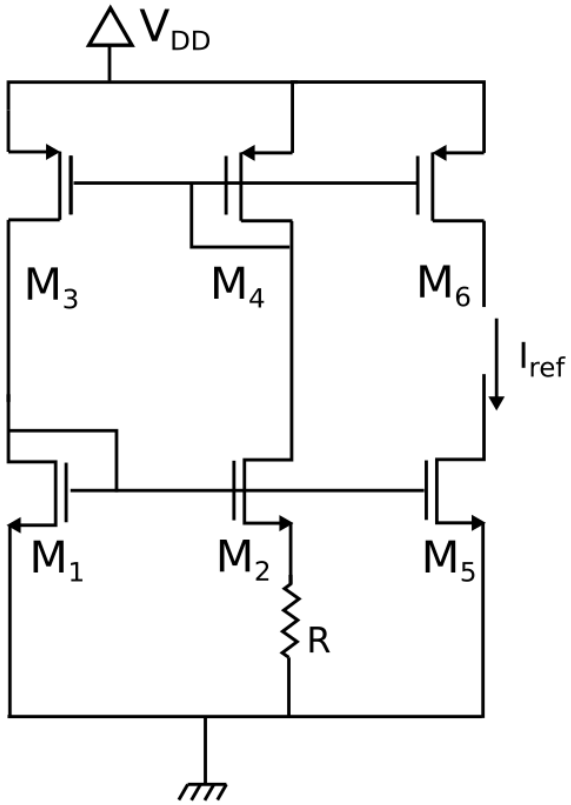
$$V_{REF} \approx \frac{kT}{q} \ln \frac{V_{DD}}{RI_s}$$



V_{DD} sensitivity less than one.

5. Reference of currents and voltages

- Power-supply independent current reference:



Bibliography

- Allen, P. E., & Holberg, D. R. (2002). CMOS analog circuit design. New York: Oxford University Press.
- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Simulations are performed through software LTSPice, provided courtesy of Analog Devices and authored by Mike Engelhardt.

Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.