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Unit 4. Single-ended and differential amplifiers

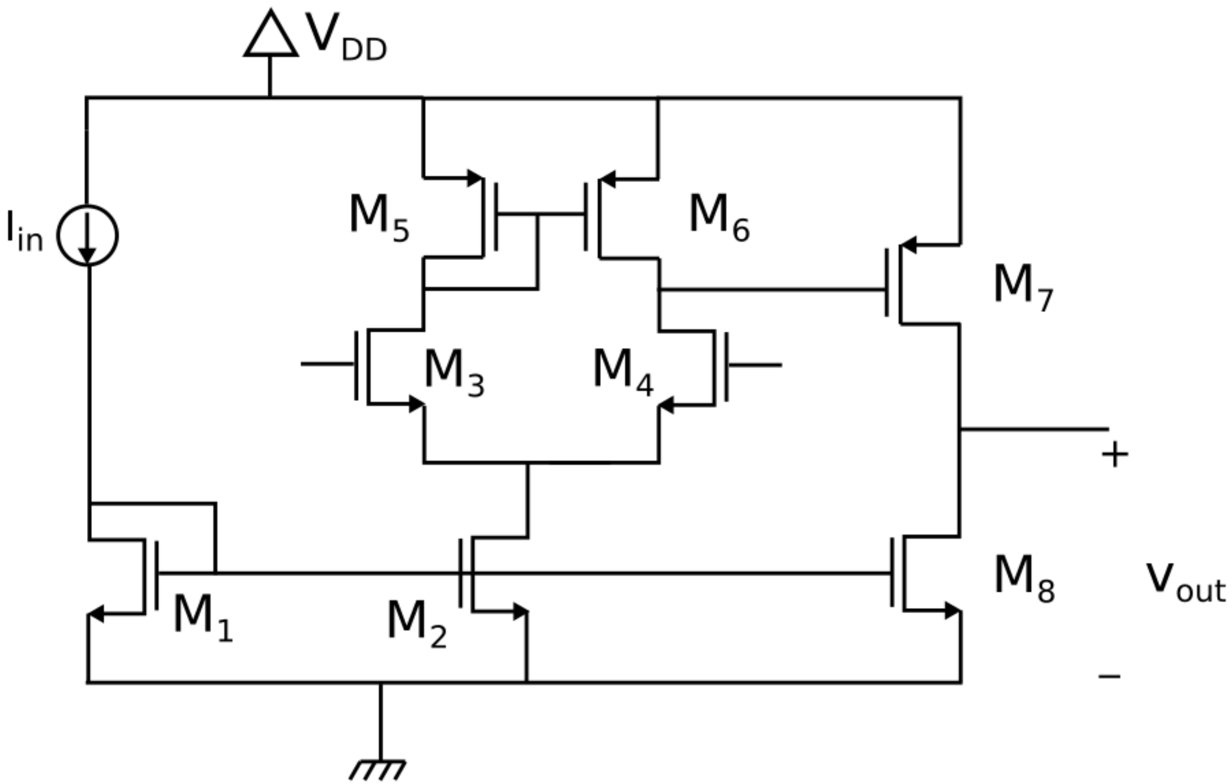
System-on-Chip and efficient electronic circuit integration techniques

Carlos III University of Madrid, Spain
Electronics Technology Department

Outline

1. **Single-ended amplifiers**
2. **Miller effect**
3. **Cascode amplifiers**
4. **Examples of single-ended amplifiers**
5. **Differential amplifiers**

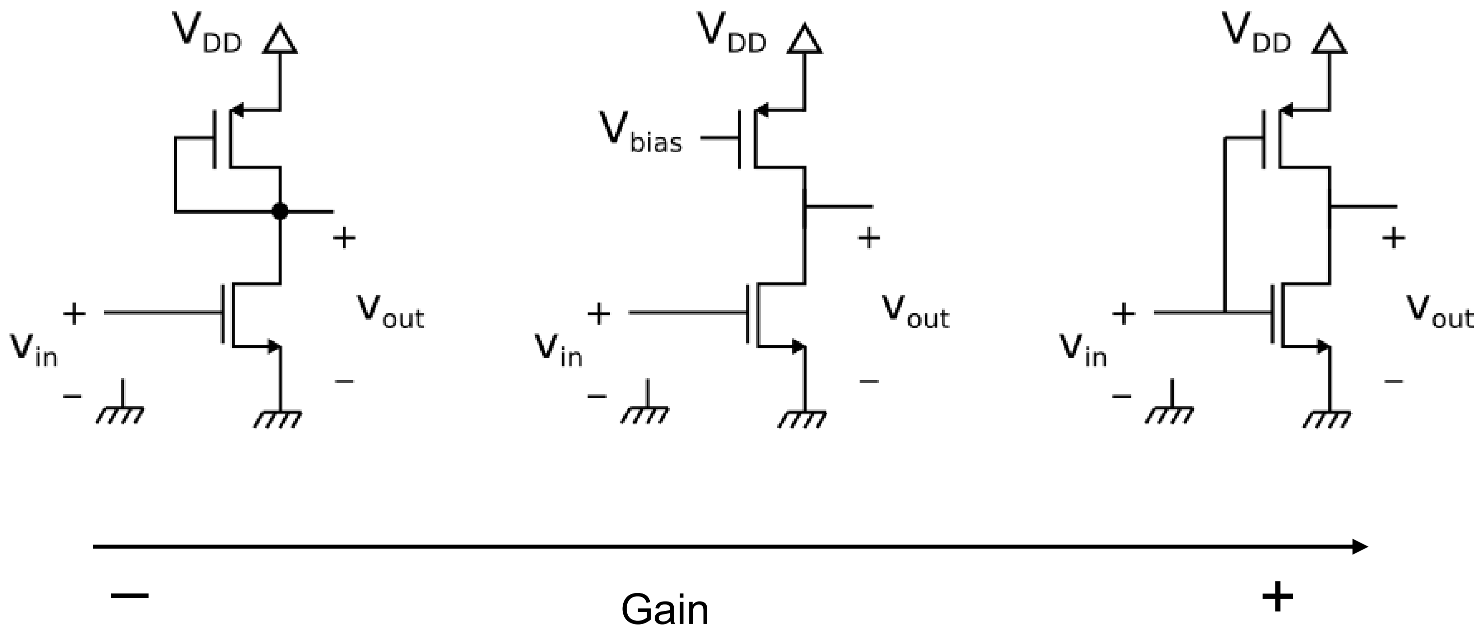
- Basic structure of an operational amplifier



1) M3, M4 turn a voltage into a current.
2) M5, M6 turn a current into a voltage.
3) M7 turns a voltage into a current.
4) M8 turns a current into a voltage.

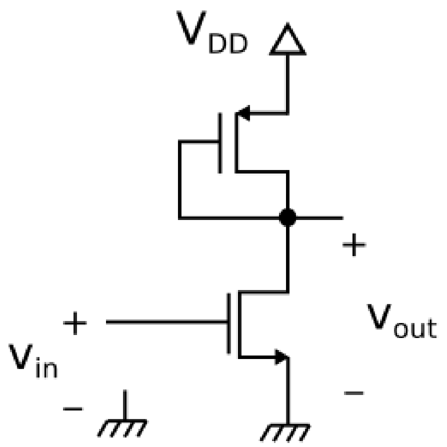
1. Single-ended amplifiers

- Common-source configuration:
  - **High voltage, current and power gain.**
  - **High input resistance.**
  - **High output resistance.**
  - Inverting stage (180º phase shift between input and output).
  - It is commonly used as the amplification stage in a multi-stage amplifier.

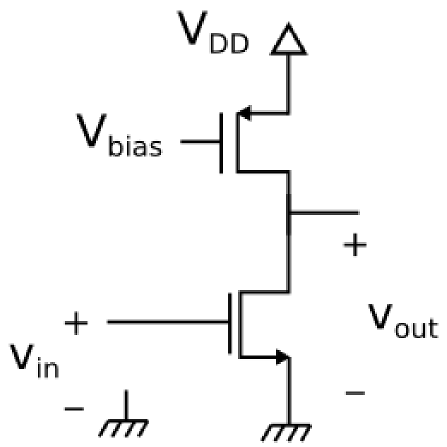


1. Single-ended amplifiers

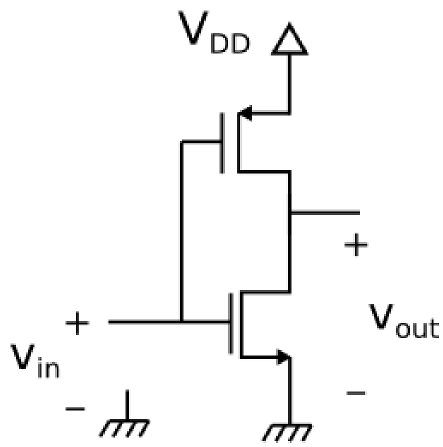
- Common-source configuration:



Active PMOS Load



Current-source Load

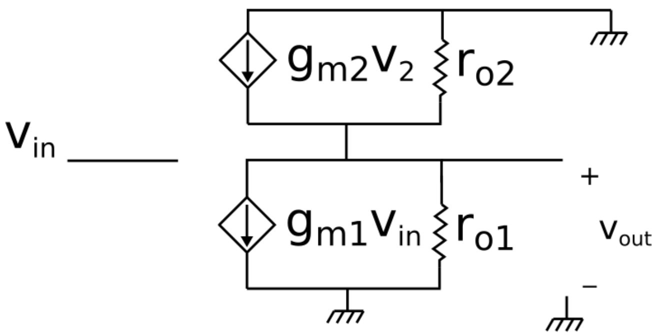


Push-Pull

1. Single-ended amplifiers

- Common-source configuration:

Active PMOS Load

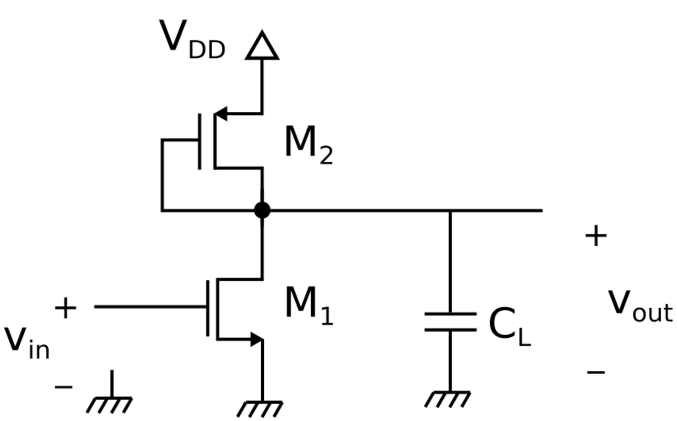


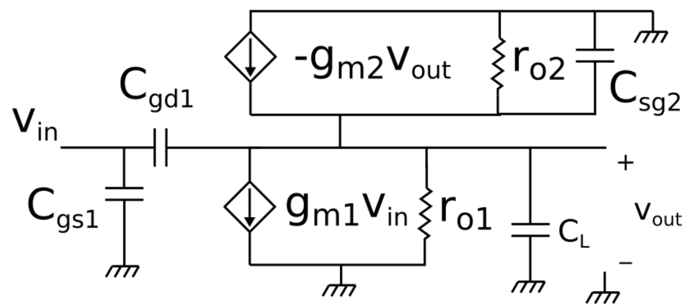
$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}} \propto \frac{W_1/L_1}{W_2/L_2}$$

$$r_{out} \approx \frac{1}{g_{m2}}$$

High resistance

Frequency response





$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1} - sC_{gd1}}{g_{m2} + s(C_{sg2} + C_{gd1} + C_L)}$$

$$p_1 = -\frac{g_{m2}}{C_{sg2} + C_{gd1} + C_L} \qquad z_1 = \frac{g_{m1}}{C_{gd1}}$$

- Common-source configuration: Frequency response

Active PMOS Load

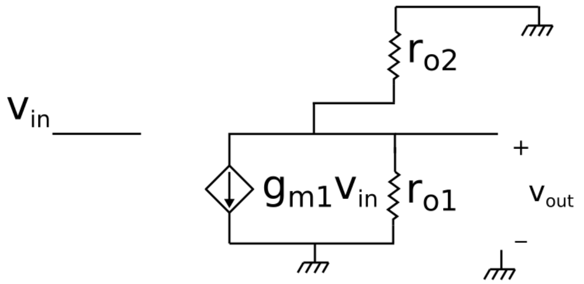
$$p_1 = -\frac{g_{m2}}{C_{sg2} + C_{gd1} + C_L} = -\frac{\sqrt{\mu_p C_{ox} {}^{W_2}/_{L_2} I_D}}{C_{sg2} + C_{gd1} + C_L} \qquad z_1 = \frac{g_{m1}}{C_{gd1}}$$

$p_1 < z_1$ → amplifier's bandwidth is limited by p_1.

To enhance amplifier's bandwidth:
- ➢ Increase the bias current.
- ➢ Reduce L.

$$p_1 \propto \frac{1}{L}\sqrt{\frac{I_D}{W}}$$

Current-source Load



$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{{}^{1}/_{r_{o1}} + {}^{1}/_{r_{o2}}} \propto \frac{1}{\sqrt{I_D}} \qquad r_{out} = r_{o1}||r_{o2}$$

g_{m2} removed!

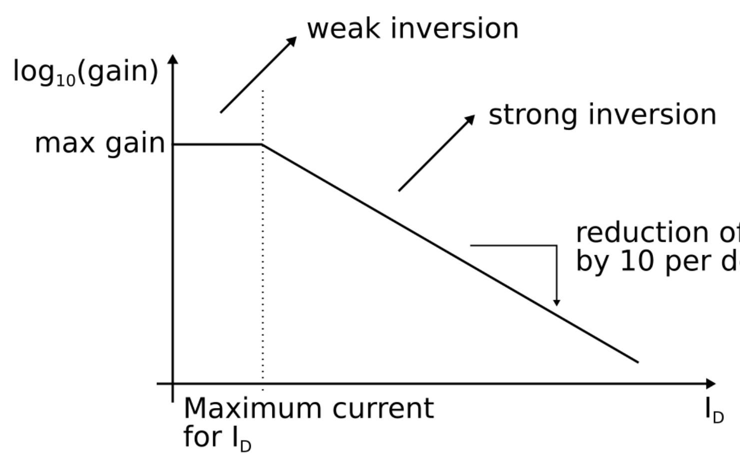
1. Single-ended amplifiers

- Common-source configuration:

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{{}^{1}\!/_{r_{o1}} + {}^{1}\!/_{r_{o2}}} \propto \frac{1}{\sqrt{I_D}}$$

"Weak inversion" → the gain is constant.

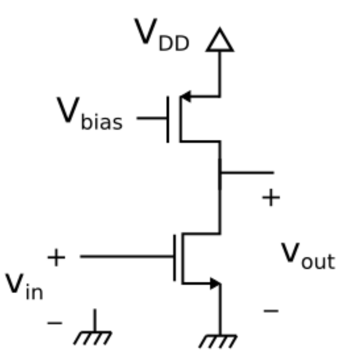
Current-source Load



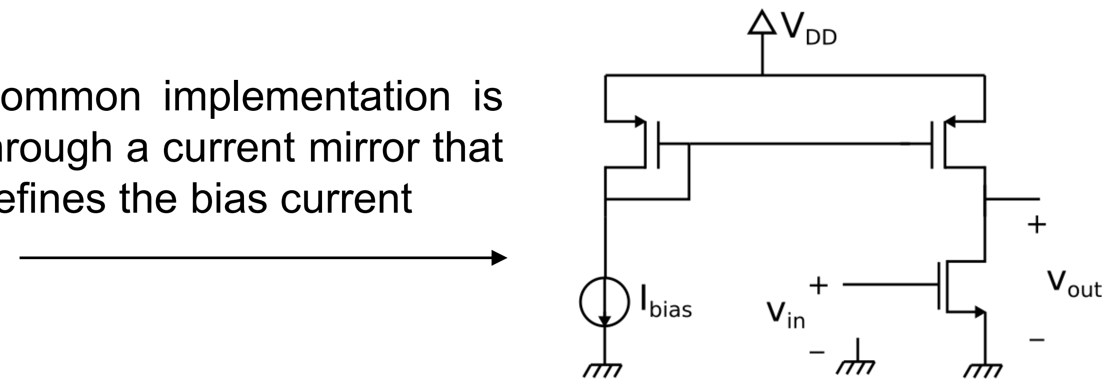
Frequency response:

$$p_1 \approx -\frac{{}^{1}\!/_{r_{o1}} + {}^{1}\!/_{r_{o2}}}{C_{gd2} + C_{gd1} + C_L} \propto \frac{I_D}{WL}$$

The higher the current the higher the bandwidth…but the lower the gain.

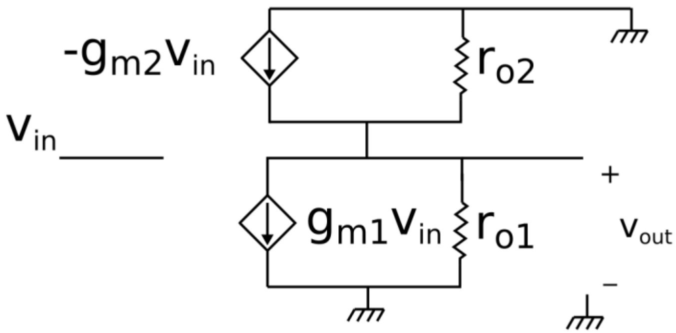


Common implementation is through a current mirror that defines the bias current



1. Single-ended amplifiers

- Common-source configuration:

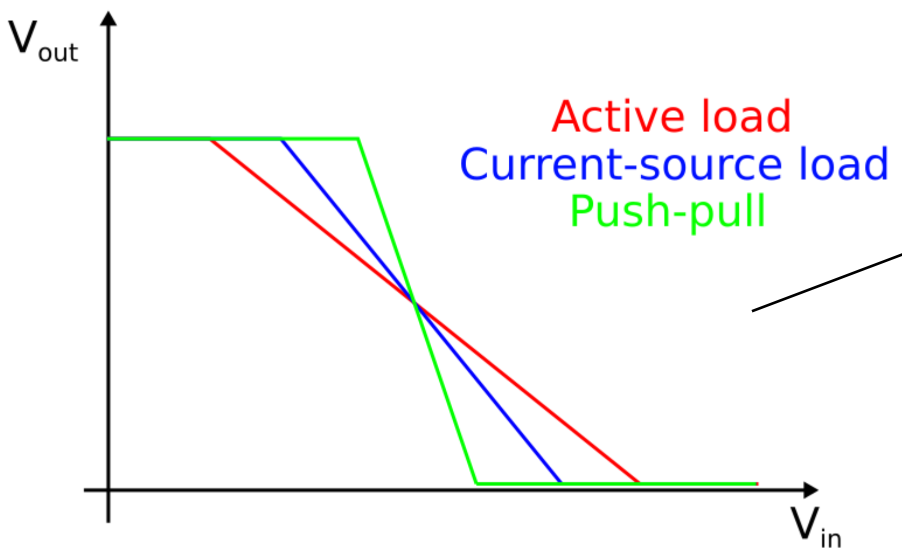


Push-pull

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}+g_{m2}}{1/r_{o1}+1/r_{o2}} \propto \frac{1}{\sqrt{I_D}}$$

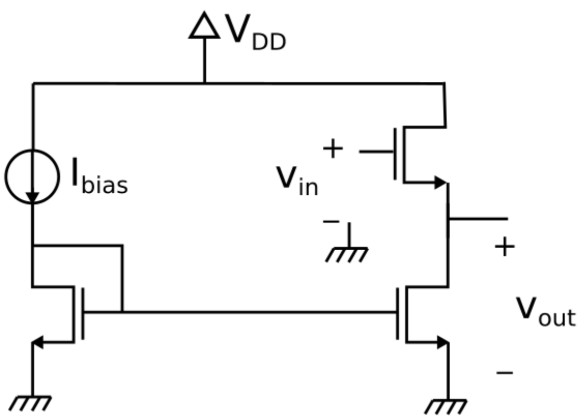
$$r_{out} = r_{o1}||r_{o2}$$

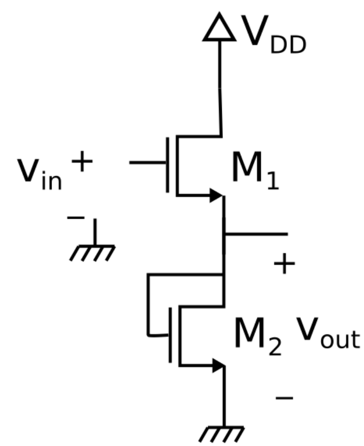
Current depends on V_{DD}.



The higher the gain the lower the dynamic range at the input

- Common-drain configuration:
  - **High current gain.**
  - **High input resistance.**
  - **Low output resistance.**
  - **Low voltage gain.**
  - Non-inverting stage (no phase shift between input and output).
  - It is commonly used as the output stage in a multi-stage amplifier to provide a low output resistance with a gain approximately equal to 1.



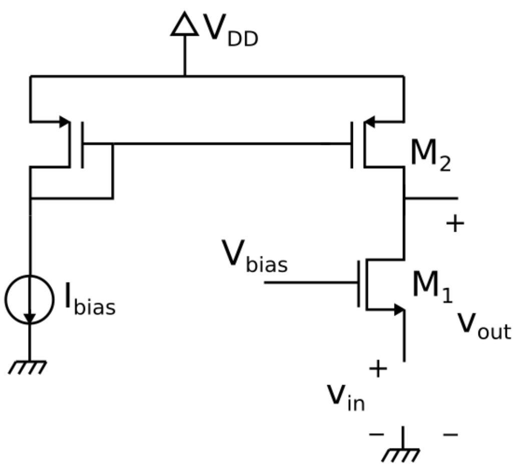


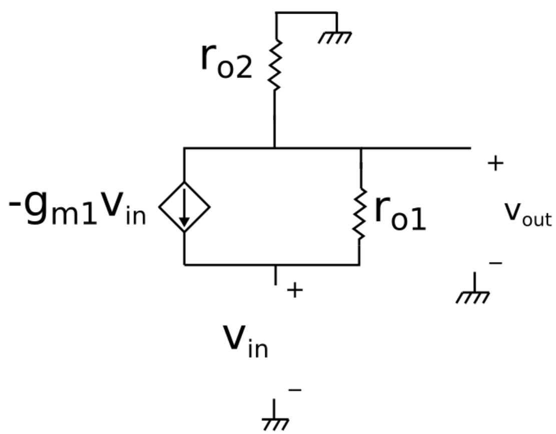
$$\frac{v_{out}}{v_{in}} \approx 1 \qquad r_{out} \approx \frac{1}{g_{m1}}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}}{g_{m2} + g_{m1}} \qquad r_{out} \approx \frac{1}{g_{m1} + g_{m2}}$$

1. Single-ended amplifiers

- Common-gate configuration:
  - **High voltage gain (similar to current source configuration).**
  - **Current gain equal to 1.**
  - **Low input resistance.**
  - **High output resistance.**
  - Non-inverting stage (no phase shift between input and output).
  - Input resistance can be increased with an external resistor.





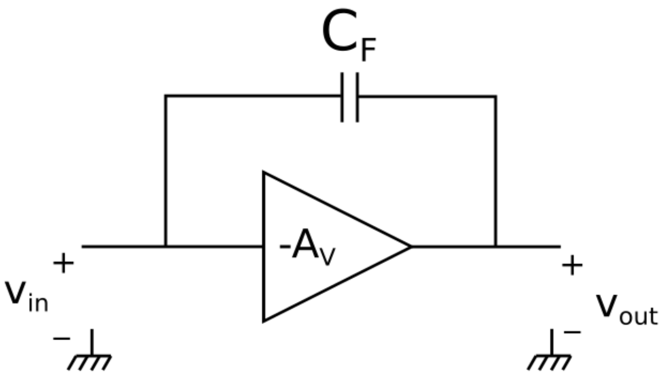
$$\frac{v_{out}}{v_{in}} \approx g_{m1}(r_{o1}||r_{o2})$$

$$r_{out} \approx (r_{o1}||r_{o2})$$

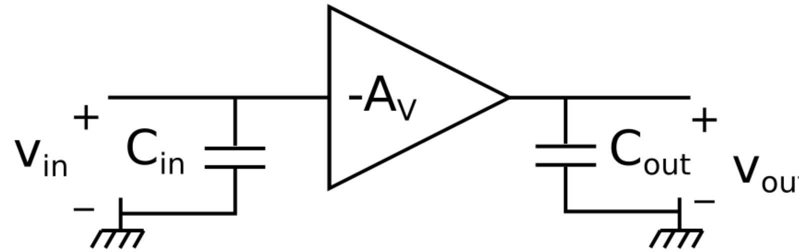
$$r_{in} \approx \frac{1}{g_{m1}}$$

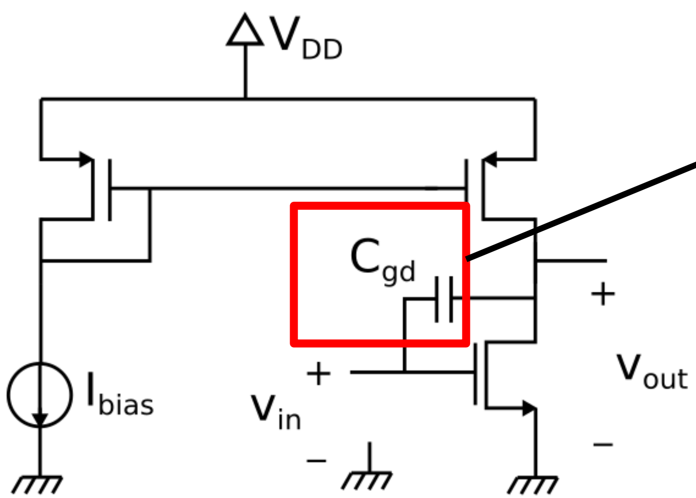
2. Miller effect

$$C_{in} = C_F(1 + |A_V|) \qquad C_{out} = C_F\left(1 + \frac{1}{|A_V|}\right)$$



Equivalent circuits

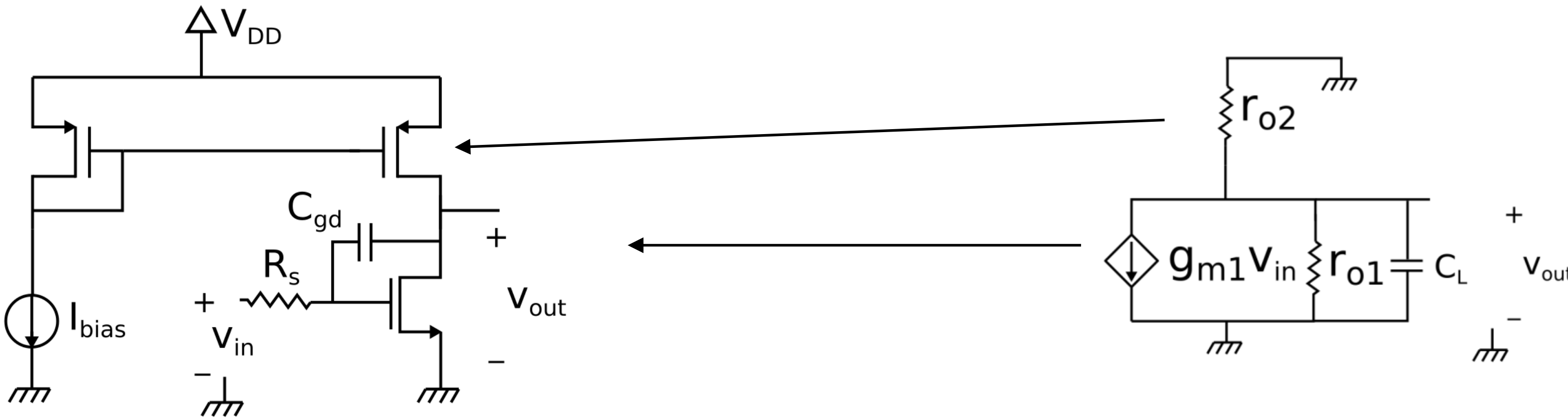




C_{gd} is multiplied by amplifier's gain:

- Higher input capacitance → slower circuit.
- Amplifier's bandwidth is decreased.

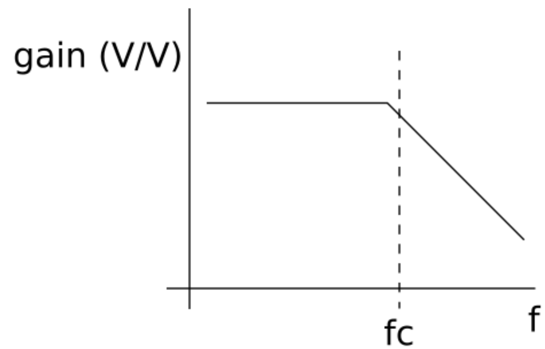
2. Miller effect



If C_L is the dominant capacitor:

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{{}^{1}/_{r_{o1}} + {}^{1}/_{r_{o2}} + sC_L}$$

$$f_c = \frac{1}{2\pi r_{out} C_L} \qquad GBW = \frac{g_{m1}}{2\pi C_L}$$



If not, considering parasitic capacitances:

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}(r_{o1}||r_{o2})}{1 + s\left(R_s\left(C_{gs1} + C_{gd1}(1 + g_{m1}(r_{o1}||r_{o2}))\right) + \underbrace{(r_{o1}||r_{o2})(C_{gd1} + C_L)}_{\text{Previous dominant pole}}\right)}$$

C_{gd1} is small but has a strong influence!

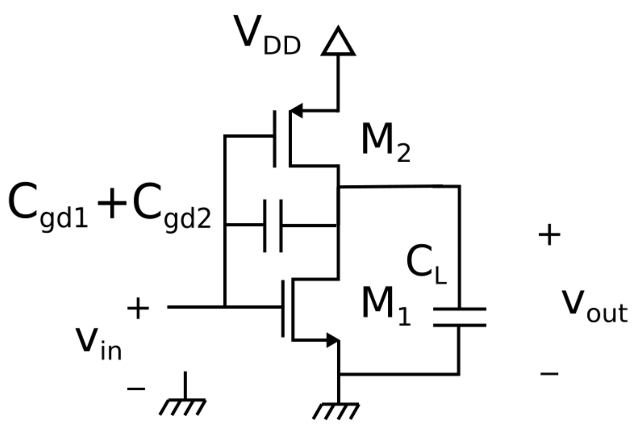
Previous dominant pole

2. Miller effect

In high-frequency designs where we limit C_L:
- Miller effect dominates → Reduce C_{GD}.
- Small devices.
- Increase V_{GS} → to increase the current.

In low-power designs (less current → lower BW):
- C_L dominates.
- Large devices.
- Reduce V_{GS} → to reduce the current.

- Miller effect in push-pull configuration:



If C_L dominates and $g_{m1}=g_{m2}$

$$\frac{v_{out}}{v_{in}} \approx -\frac{2g_{m1}}{1/r_{o1} + 1/r_{o2} + sC_L}$$

$$f_c = \frac{1}{2\pi r_{out} C_L}$$

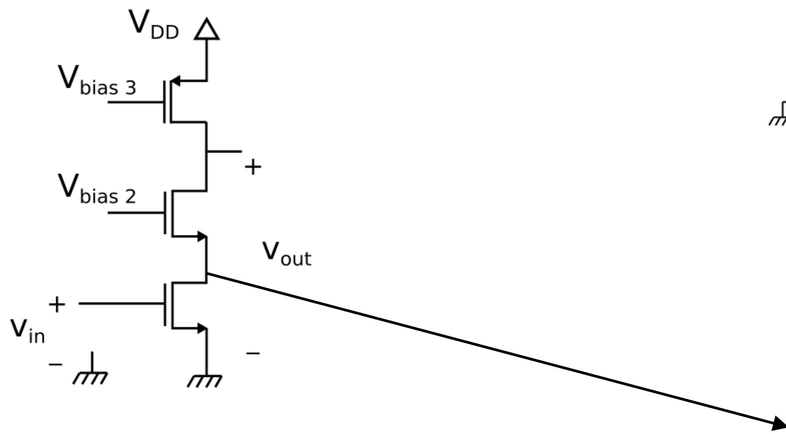
$$GBW = \frac{2g_{m1}}{2\pi C_L}$$

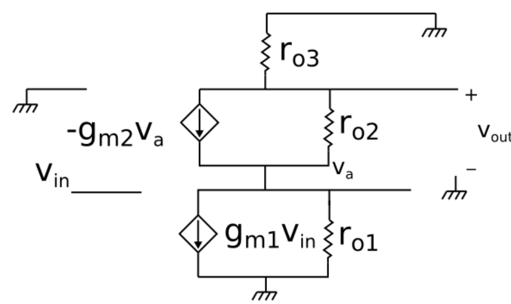
GBW doubles

3. Cascode amplifiers

Advantages of cascode structures in comparison to previous architectures:

- **Higher output impedance** → higher gain.
- For similar BW → higher gain. For the same gain → higher BW.
- **Alleviate Miller effect** → suitable for high-frequency designs.
- **Alleviate short-channel effects**.





Looking at this node (Va):

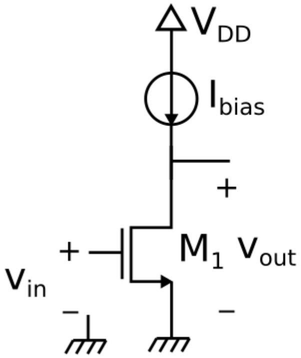
$$\frac{v_{out}}{v_{in}} \approx -g_{m1}r_{o3} = -\sqrt{\frac{2\mu_n C_{ox} W_1}{L_1 \lambda_3^2 I_D}}$$

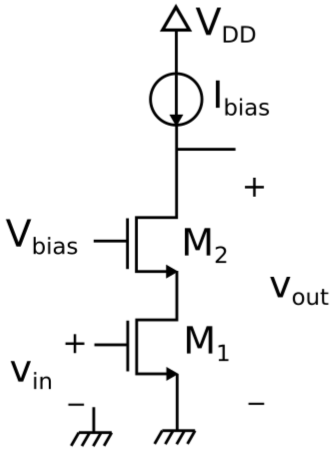
$$\frac{W_1}{L_1} = \frac{W_2}{L_2} \qquad r_{o2} = r_{o3}$$

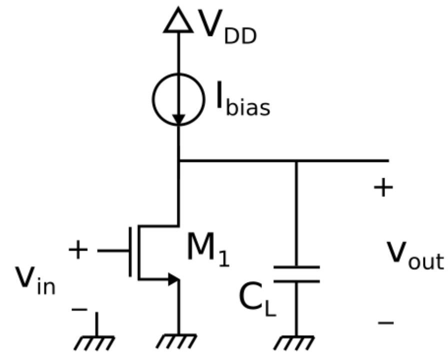
$$r_{out} \approx r_{o3}$$

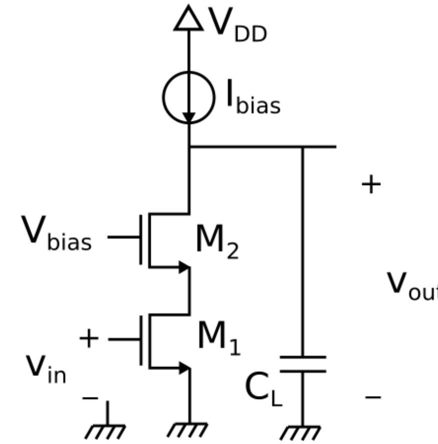
$$\frac{v_a}{v_{in}} \approx -2$$ → Gain doubles → From V_a to V_{out} we have a common-gate configuration

3. Cascode amplifiers









$$\frac{v_{out}}{v_{in}} \approx -g_{m1} r_{o1}$$

$$R_{out} \approx r_{o1}$$

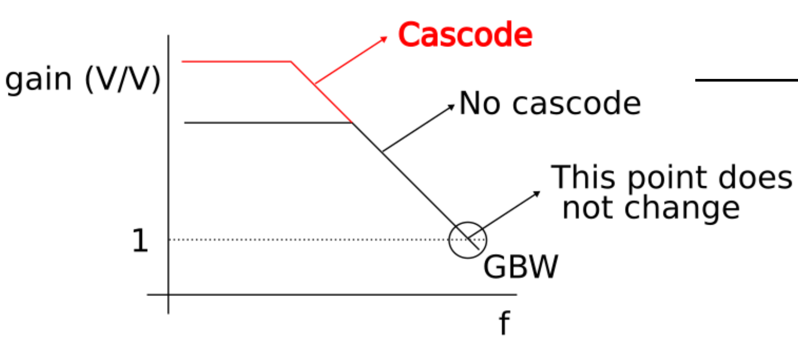
$$\frac{v_{out}}{v_{in}} \approx -g_{m1}(r_{o1} g_{m2} r_{o2})$$

$$R_{out} \approx r_{o1} g_{m2} r_{o2}$$

$$BW \approx \frac{1}{2\pi R_{out} C_L}$$

$$GBW \approx \frac{g_{m1}}{C_L}$$

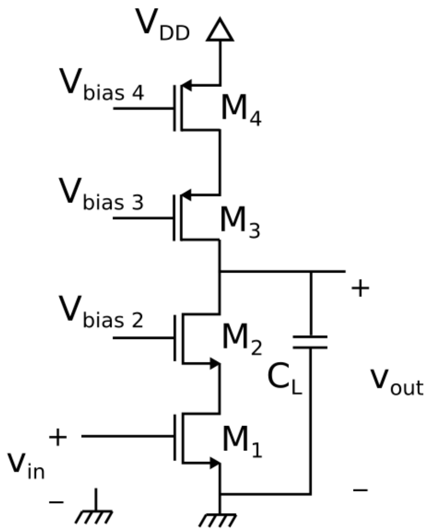
For both!



→ Improving of low-frequency gain

3. Cascode amplifiers

To increase even more the output resistance and then the gain:



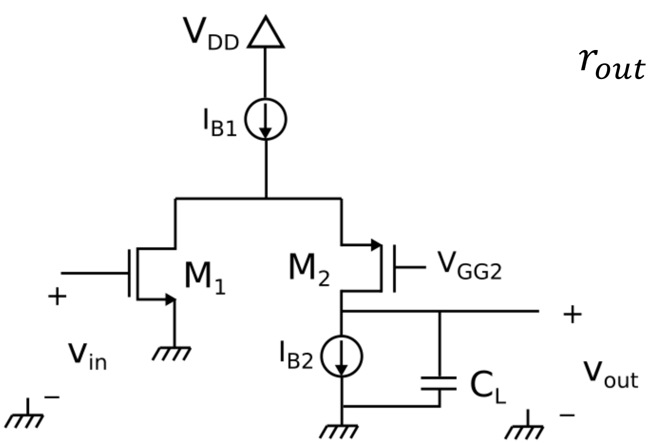
$$r_{out} \approx g_{m2} r_{o1} r_{o2} || g_{m3} r_{o3} r_{o4}$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1} r_{out}$$

$$f_c = \frac{1}{2\pi r_{out} C_L}$$

$$GBW = \frac{g_{m1}}{2\pi C_L}$$

- **Telescopic cascode.**
- Suitable for high voltage supply.
- L > 120 nm.
- Low input and output dynamic range.



$$r_{out} \approx g_{m2} r_{o1} r_{o2}$$

$$\frac{v_{out}}{v_{in}} \approx -g_{m1} g_{m2} r_{o1} r_{o2}$$

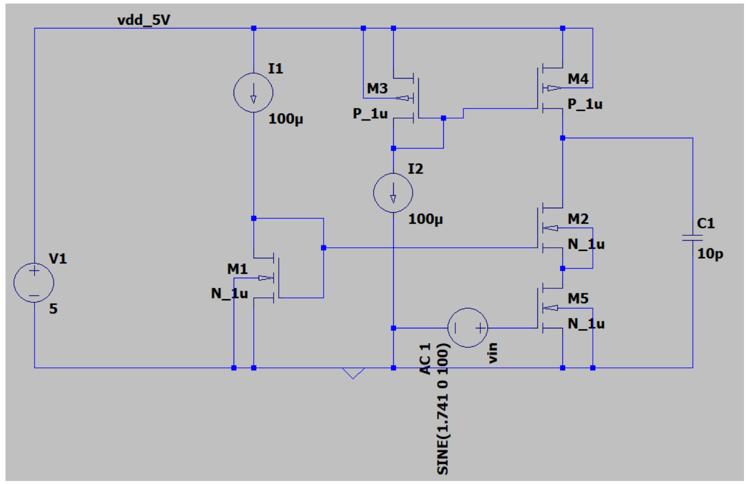
$$f_c = \frac{1}{2\pi r_{out} C_L}$$

$$GBW = \frac{g_{m1}}{2\pi C_L}$$

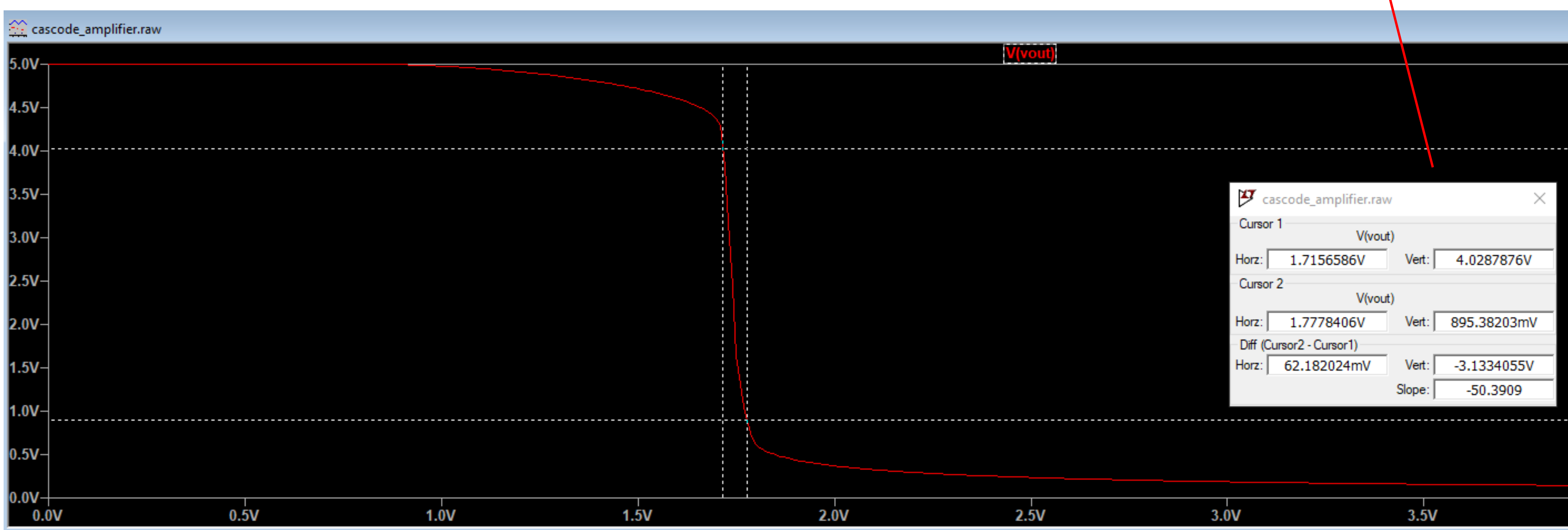
- **Folded cascode.**
- Suitable for low voltage supply.
- Enhanced input and output dynamic range.
- Power consumption doubles.

4. Examples of single-ended amplifiers

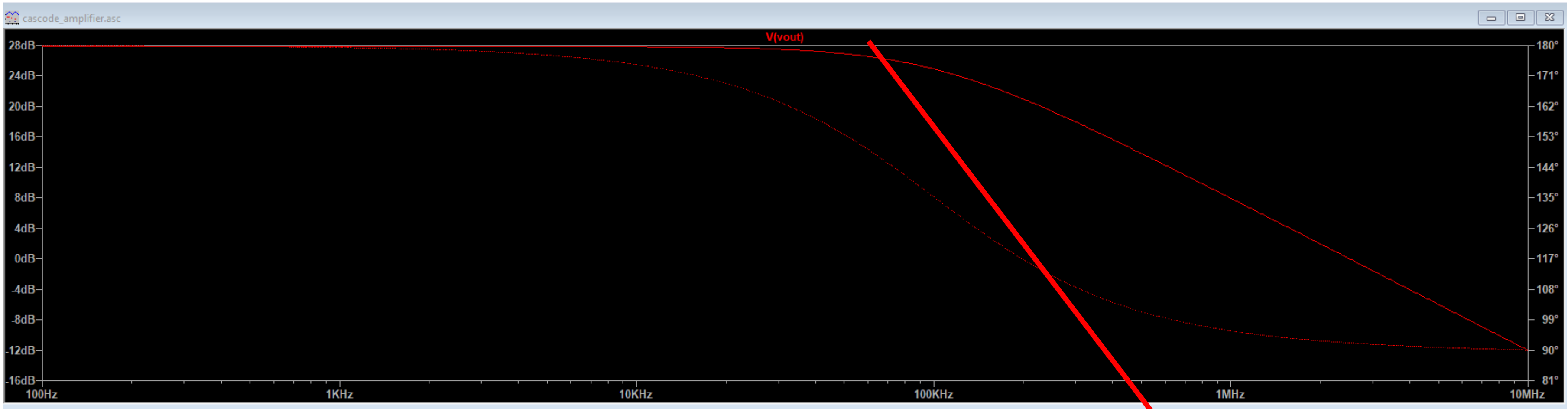
L = 1µm



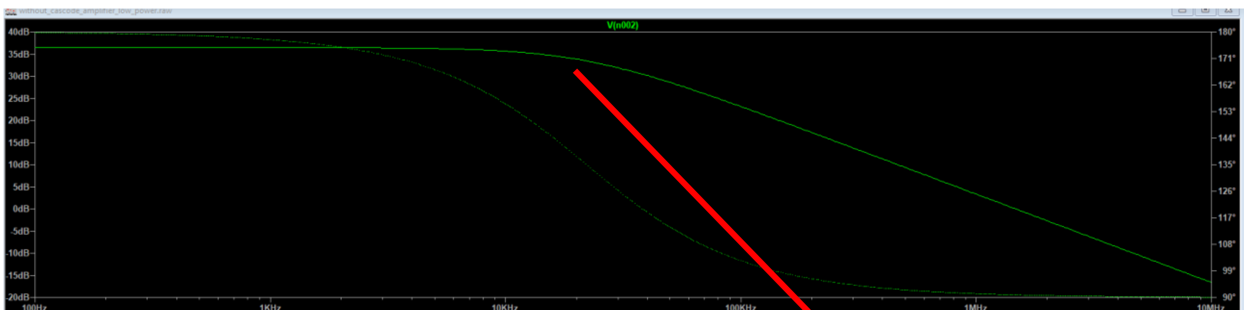
3.13V/0.06 = 52 V/V

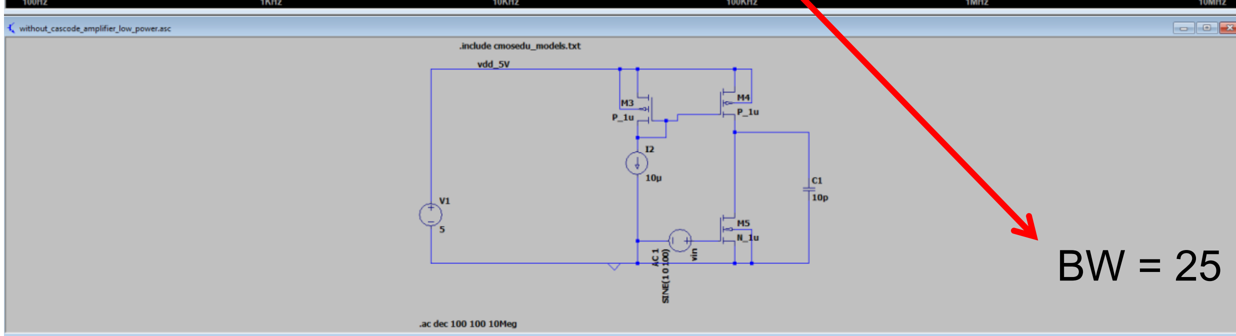


4. Examples of single-ended amplifiers



BW = 60 kHz

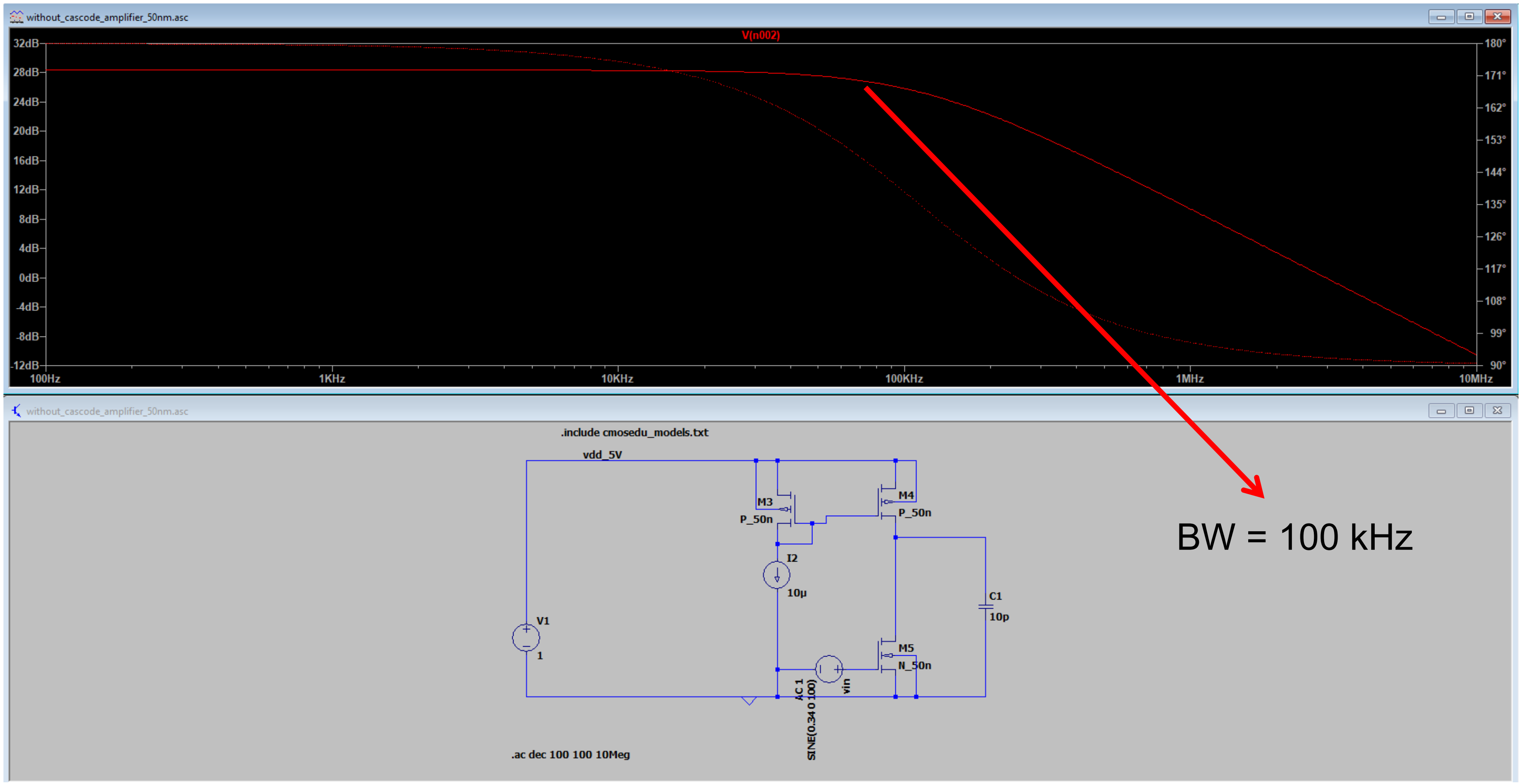




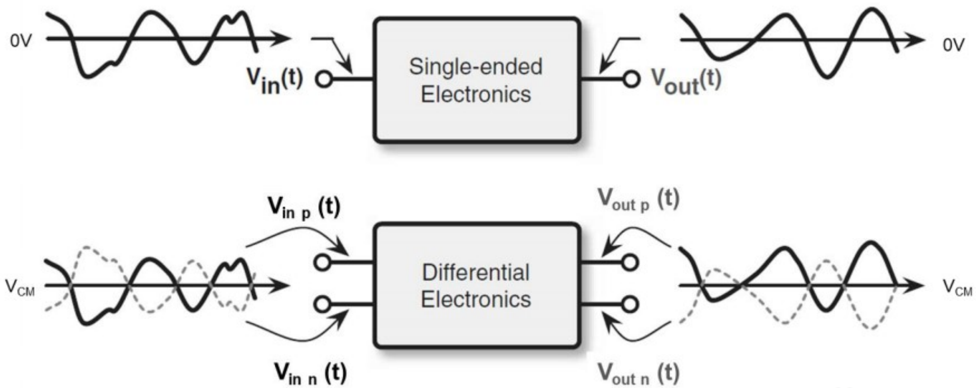
No cascode connection→Similar gain but lower BW.

BW = 25 kHz

Going towards a narrower node (50nm) → BW enhanced



5. Differential amplifiers



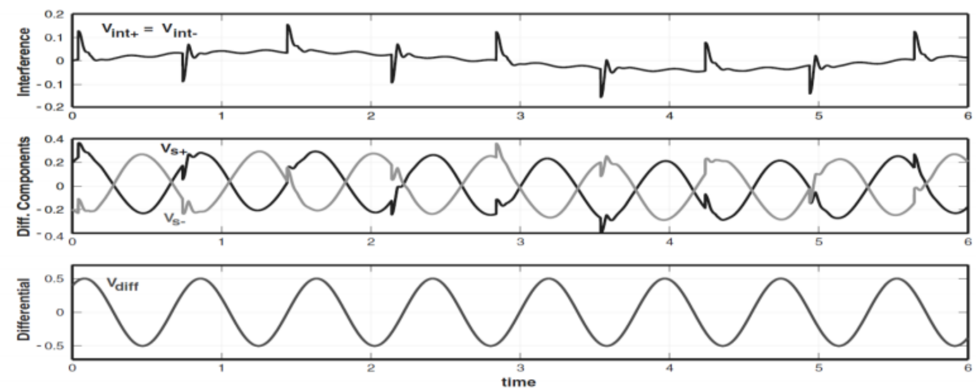
Peak amp=2Vpk

Peak amp=Vpk

$$V_{in\,diff}(t) = V_{in\,p}(t) - V_{in\,n}(t)$$

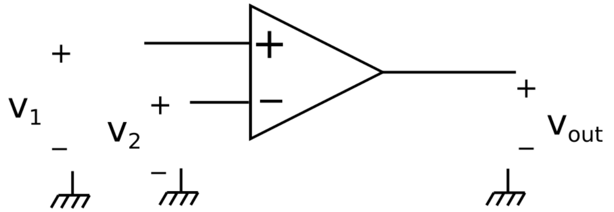
$$V_{out\,diff}(t) = V_{out\,p}(t) - V_{out\,n}(t)$$

Differential circuits are required to mitigate common noise

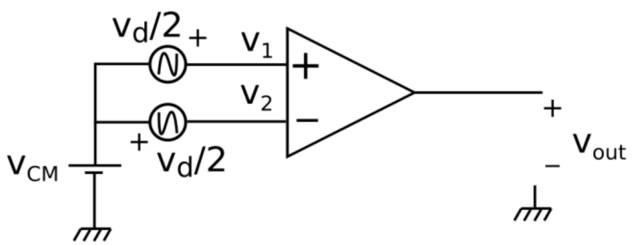


- Remove common signals between both channels (common interferences and even harmonics).
- In data converters → **+3 dB SNR improvement**.
- Common-Mode Feed-Back (**CMFB**) control circuits are required.
- They consume more than “single-ended” circuits, but show better noise performance.

5. Differential amplifiers



V_1, V_2 y V_{out} are single-ended signals → they are referred to GND



$V_1=V_{CM}+V_d/2$

$V_2=V_{CM}-V_d/2$

$V_d=V_1-V_2$

$V_{CM}=(V_1+V_2)/2$

V_d is the differential mode input voltage

V_{CM} is the common mode input voltage

- V_{out} can be expressed as a combination of both the differential and the common mode signals:

$$v_{out} = A_d v_d + A_{CM} v_{CM} = A_d(v_1 - v_2) + A_{CM}\left(\frac{v_1 + v_2}{2}\right)$$

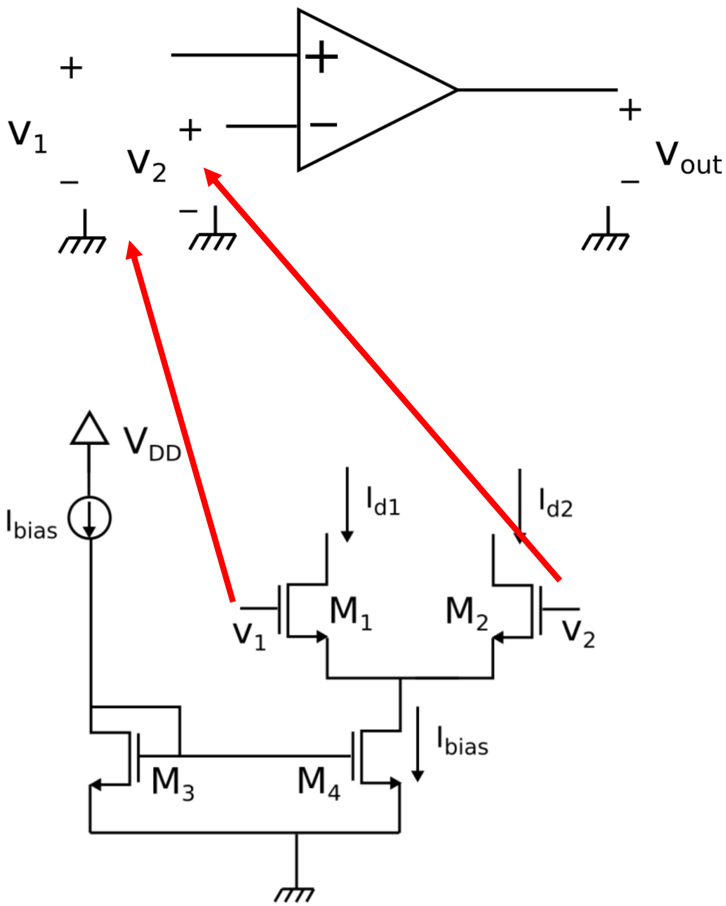
Differential-mode gain (A_d) — Common-mode gain (A_{CM})

$$CMRR = 20\log_{10}\frac{A_d}{A_{CM}}$$

Common-Mode Rejection Ratio

ICMR (Input common-mode range): V_{CM} range to keep differential gain

5. Differential amplifiers

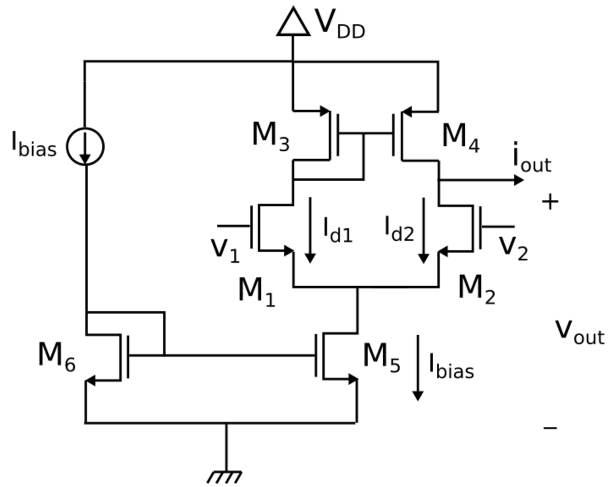


$$I_{bias} = i_{d1} + i_{d2}$$

$$v_d = v_1 - v_2 = \sqrt{\frac{2i_{D1}}{\mu_n C_{OX}\frac{W_1}{L_1}}} - \sqrt{\frac{2i_{D2}}{\mu_n C_{OX}\frac{W_2}{L_2}}}$$

$$g_m(v_d = 0) = \sqrt{\frac{\mu_n C_{OX} W I_{bias}}{4L}}$$

The higher I_{bias} the higher g_m



$$i_{out} = i_{d1} - i_{d2}$$

Si $V_d>0$ → i_{out} increases, V_{out} increases
Si $V_d<0$ → i_{out} decreases, V_{out} decreases

$$g_{md}(v_d = 0) = \frac{\partial i_{out}}{\partial v_d} = \sqrt{\frac{\mu_n C_{OX} W I_{bias}}{L}} = g_{m1}$$

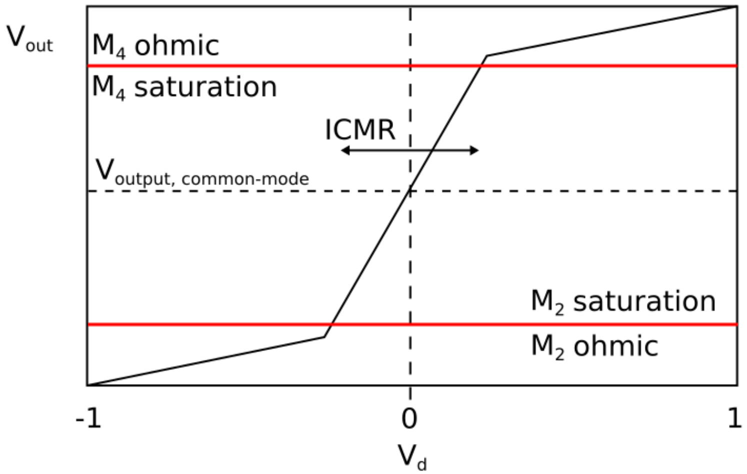
- Simple way of turning a differential signal into a single-ended one (Vout).
- Typically used in the input stage of operational amplifiers and comparators.
- Saturation requirements:

$$V_{DS2} \geq V_{GS2} - V_{thN}$$

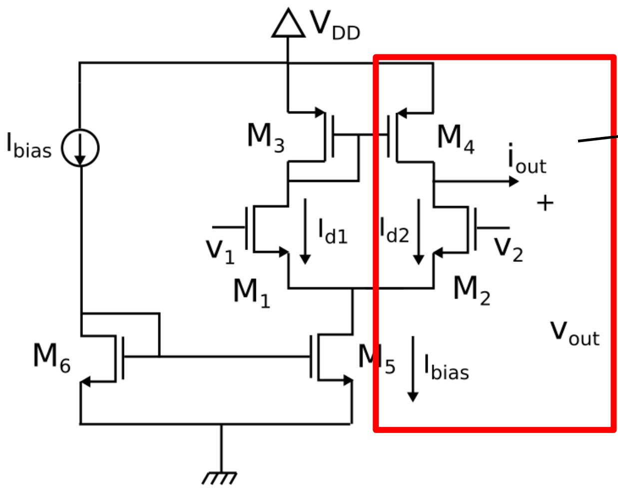
$$\rightarrow V_{out} \geq V_{CM} - 0.5v_d - V_{thN}$$

$$V_{SD4} \geq V_{SG4} - V_{thP}$$

$$\rightarrow V_{out} \leq V_{DD} - V_{SG4} + V_{thP}$$



5. Differential amplifiers



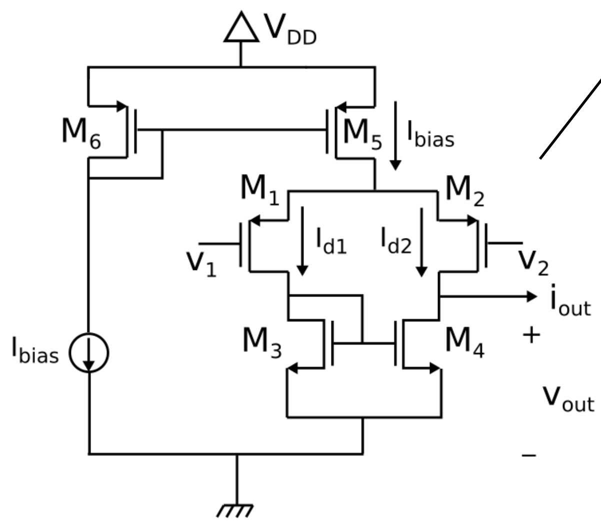
Common-source configuration:

$$A_d = \frac{v_{out}}{v_d} = g_{m1}(r_{o2}||r_{o4}) = \frac{2}{\lambda_2 + \lambda_4}\sqrt{\frac{\mu_n C_{OX} W}{I_{bias} L}}$$

Example: W/L=2 e I_{bias}=10uA → $A_{d,NMOS} = 52$

$A_{d,PMOS} = 35$

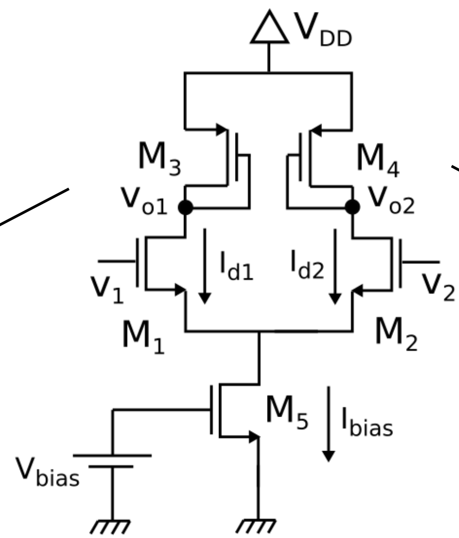
Equivalence with PMOS devices:



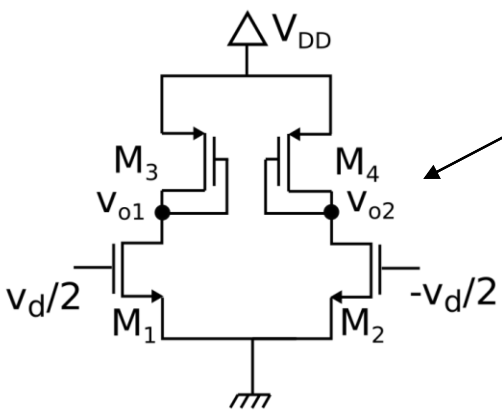
PMOS transconductance is lower than NMOS one

5. Differential amplifiers

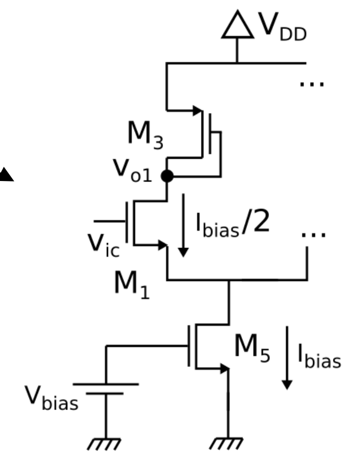
General circuit



Differential mode

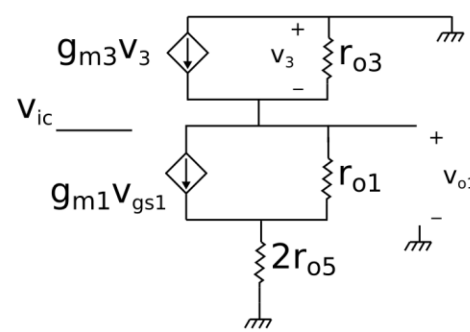


Common mode



$$\frac{v_{o1}}{v_d} = -\frac{g_{m1}}{2g_{m3}}$$

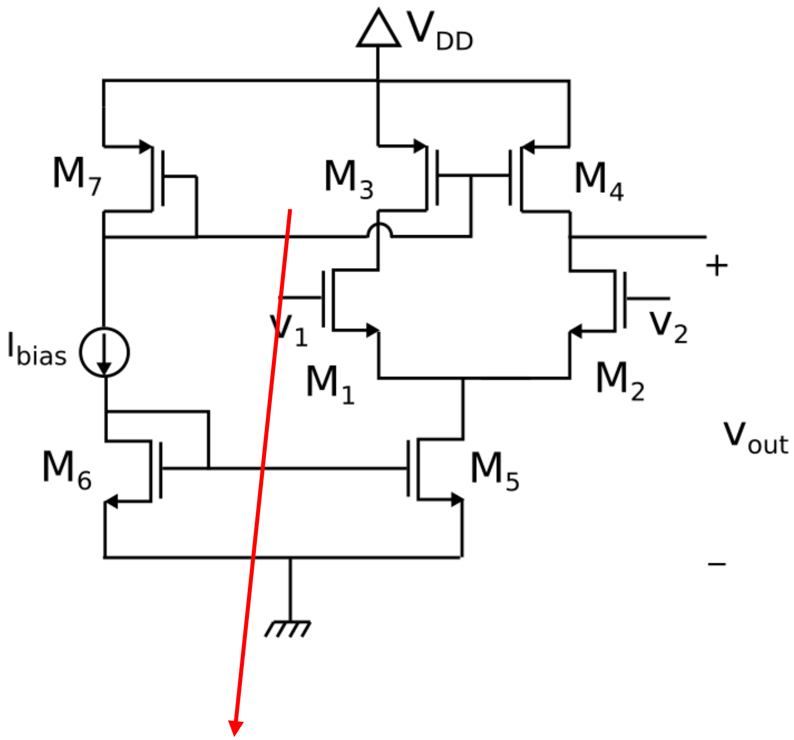
$$\frac{v_{o2}}{v_d} = +\frac{g_{m2}}{2g_{m4}}$$



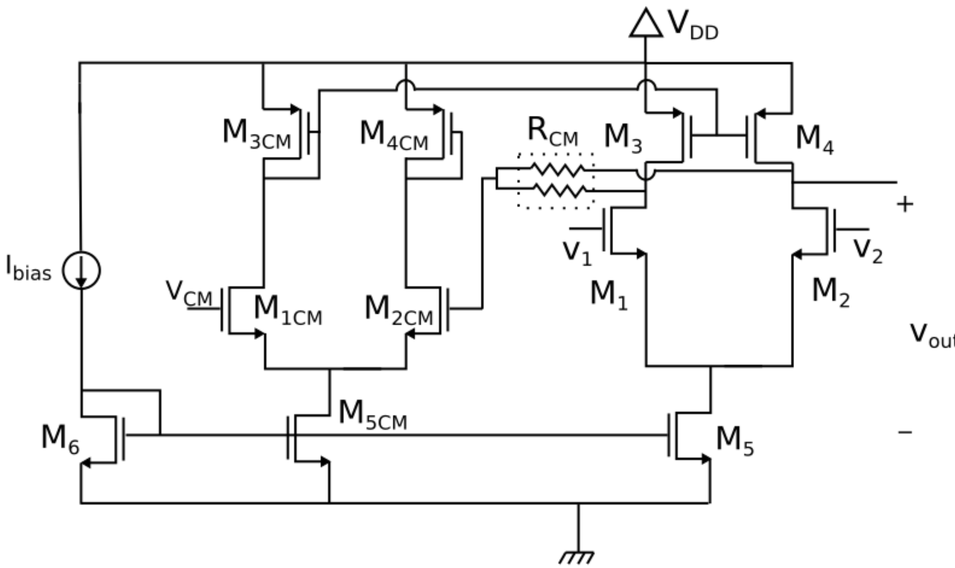
$$\mathrm{CMRR} = 20\log_{10}\frac{\mathrm{v_{o1}}/\mathrm{v_{id}}}{\mathrm{v_{o1}}/\mathrm{v_{ic}}} = \mathbf{20\log_{10} g_{m1} r_{o5}}$$

$$\frac{v_{o1}}{v_{ic}} = -\frac{1}{2g_{m3}r_{o5}}$$

- Differential amplifier with current-source load



$$A_d = \frac{v_3 - v_4}{v_d} = g_{md}(r_{o2}||r_{o4}) = \frac{2}{\lambda_2 + \lambda_4}\sqrt{\frac{\mu_n C_{OX} W}{I_{SS} L}}$$

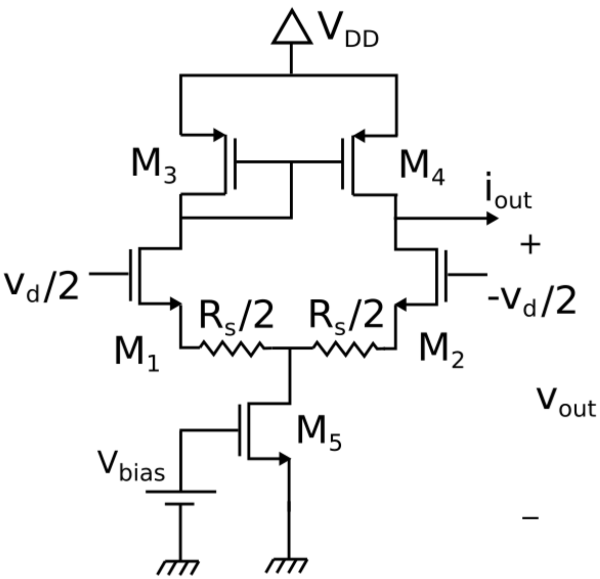


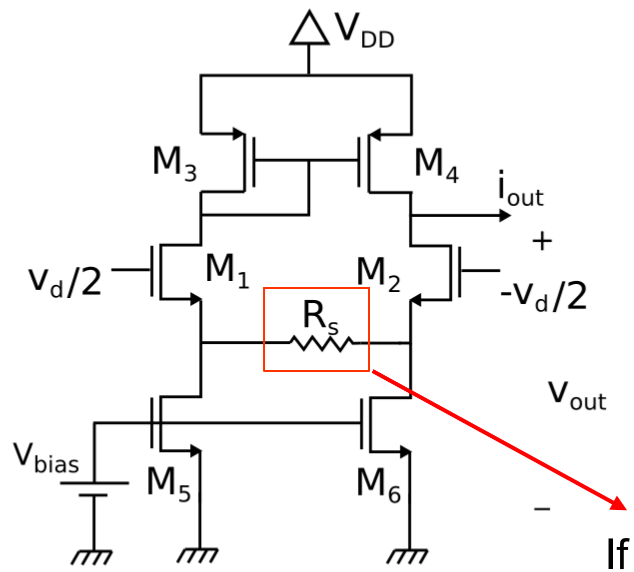
M3 is not diode connected → higher ICMR

CMFB → to control output DC voltage

5. Differential amplifiers

- Degenerated differential pair → to improve linearity





Suitable for low voltage supply.

If large use a transistor biased in linear region

$$g_m = \frac{i_{out}}{v_d} = \frac{g_{m1}}{2 + g_{m1}R_S} \approx \frac{1}{R_S}$$

Bibliography

- Allen, P. E., & Holberg, D. R. (2002). CMOS analog circuit design. New York: Oxford University Press.
- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Simulations are performed through software LTSPice, provided courtesy of Analog Devices and authored by Mike Engelhardt.

Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.