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Unit 5. Operational amplifiers (opamps) and OTAs

System-on-Chip and efficient electronic circuit integration techniques

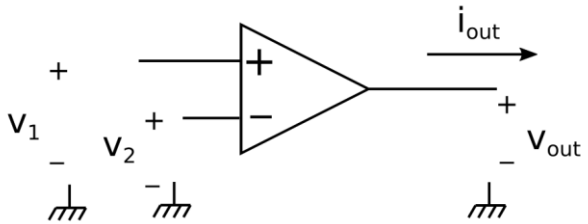
Carlos III University of Madrid, Spain

Electronics Technology Department

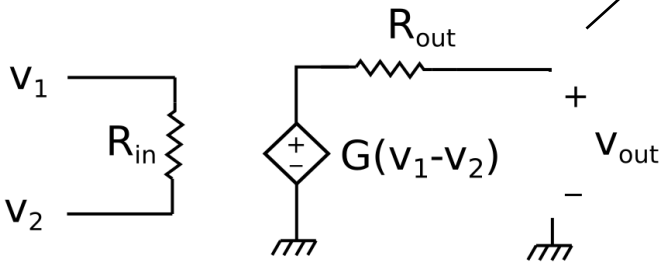
Outline

1. Basic concepts
2. Compensation techniques
3. Two-stage architecture design
4. Cascode structures
5. Symmetric CMOS OTA
6. Output stages
7. CMFB circuits
8. Examples

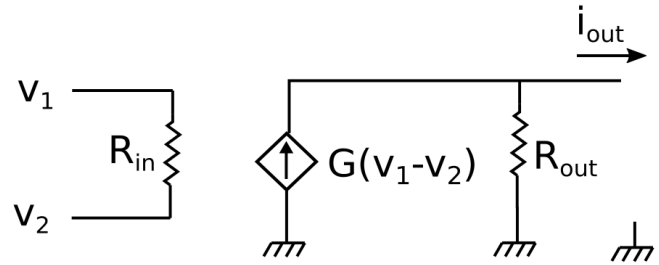
1. Basic concepts



Very large G → gain fixed when negative fedback→ stability?



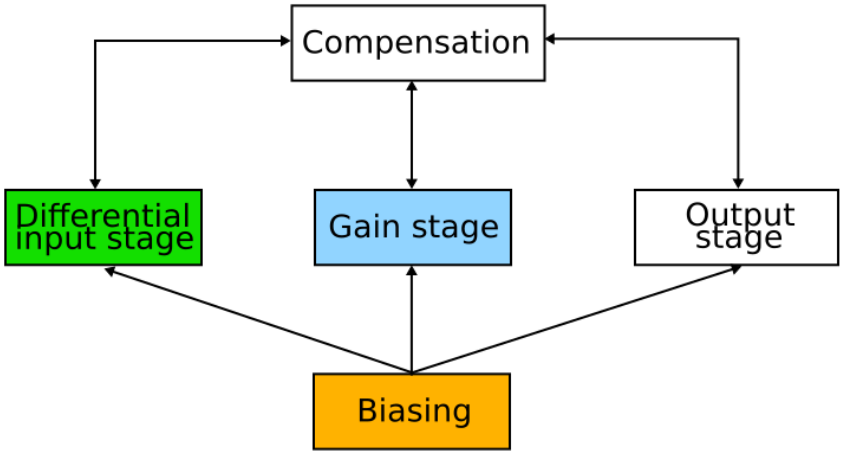
If R_{out} must be small, we need an output stage (buffer) → output voltage → opamp (classic definition of an operational amplifier)

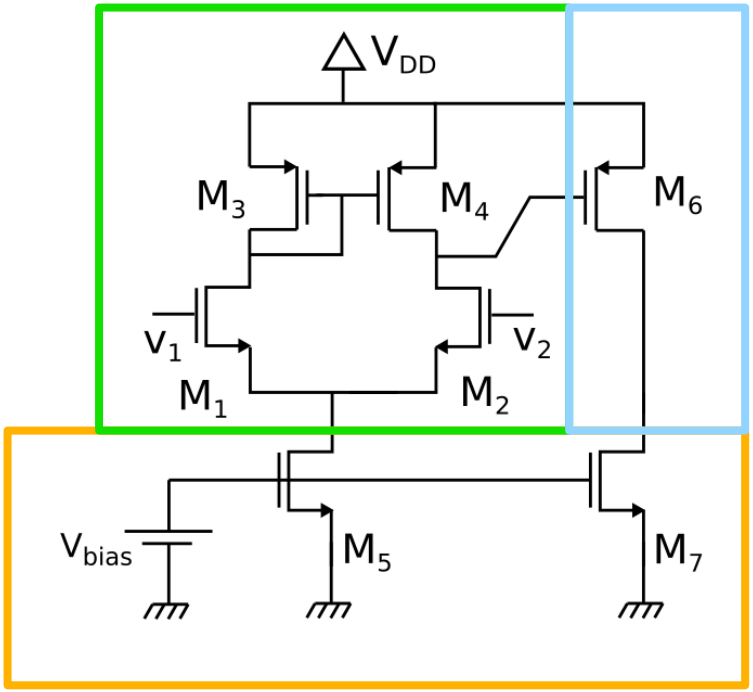


If R_{out} must be high, we do not need an output stage (unbuffered) → output current → OTA (operational transconductance amplifier), they only feed capacitive loads or very high resistances

1. Basic concepts

- Most of the opamps make use of two or more stages to have enough gain, especially with deep-submicron processes.
- General scheme:





1. Basic concepts

- Requirements for opamp design:
  1. Constraints due to the process selected:
     - ❑ Process specifications (V_{th}, intrinsic gain, C_{ox}, …).
     - ❑ Nominal voltage supply.
     - ❑ Maximum current.
     - ❑ Temperature range.
  2. Design requirements:
     - ❑ Gain.
     - ❑ GBW.
     - ❑ Maximum power.
     - ❑ SR.
     - ❑ ICMR.
     - ❑ CMRR.
     - ❑ PSRR.
     - ❑ Output swing.
     - ❑ Output resistance.
     - ❑ Noise.

$$\mathrm{PSRR} = 20\log_{10}\frac{\Delta V_{DD} A_V}{\Delta V_{out}}$$

Idea conception

- Design steps:

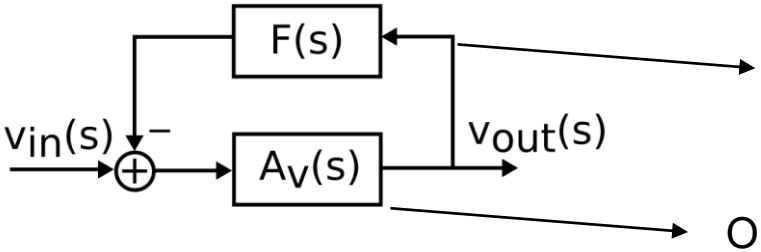
1. Select suitable architecture.
2. Select compensation technique to be implemented.
3. Architecture desing: devices' size and bias conditions.

Architecture optimization

4. Validation and tuning through simulations

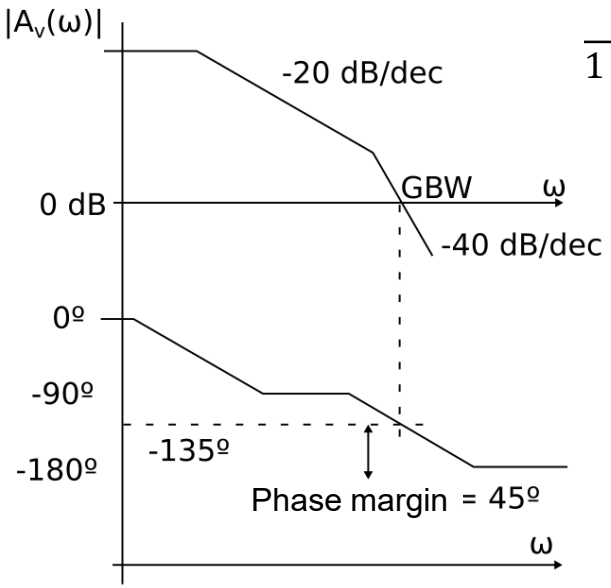
1. Basic concepts

- Opamp stability:

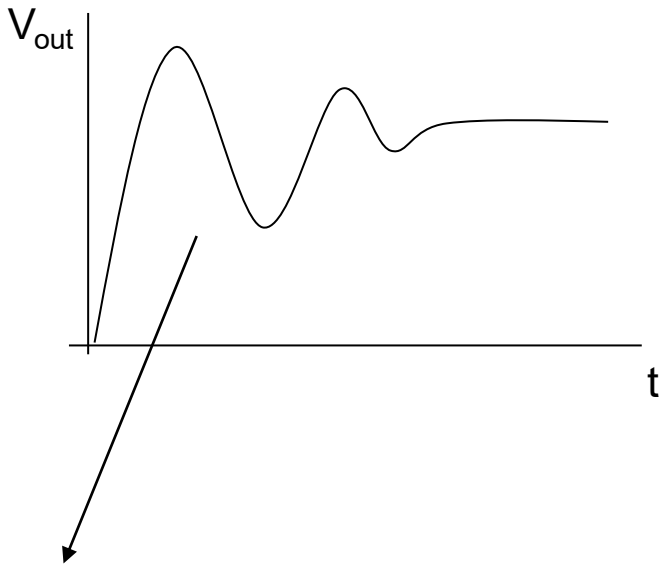


Feedback network: the worst case for stability is when F(s) = 1.

Opamp open loop gain.



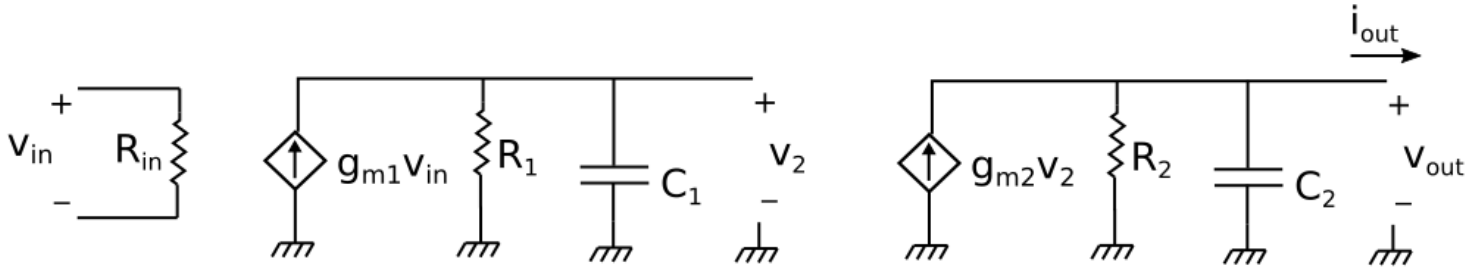
$$\frac{A_V(s)}{1 + A_V(s)F(s)}$$



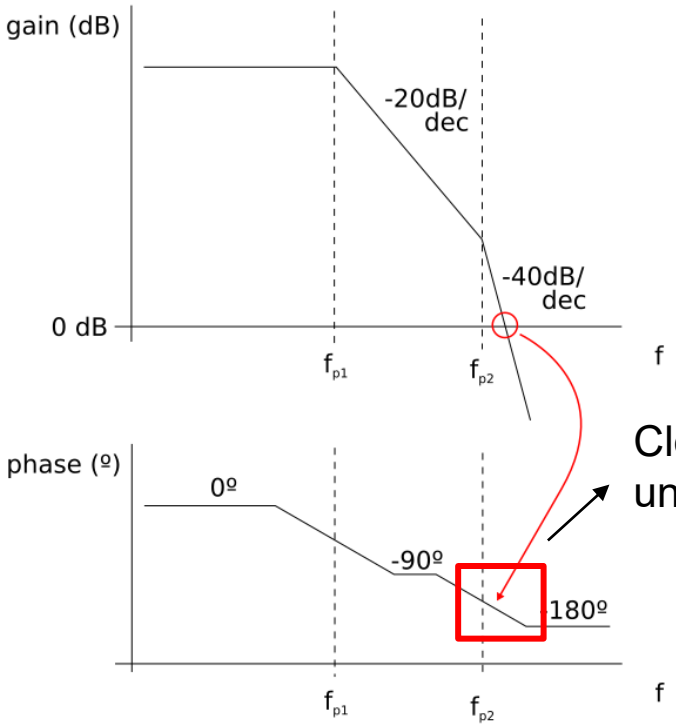
To avoid ringing at the output a phase margin higher than 45º is required (**preferably 60º**)

2. Compensation techniques

- General structure of a two-stage opamp:



$$p_1 = \frac{-1}{R_1 C_1} \qquad p_2 = \frac{-1}{R_2 C_2}$$

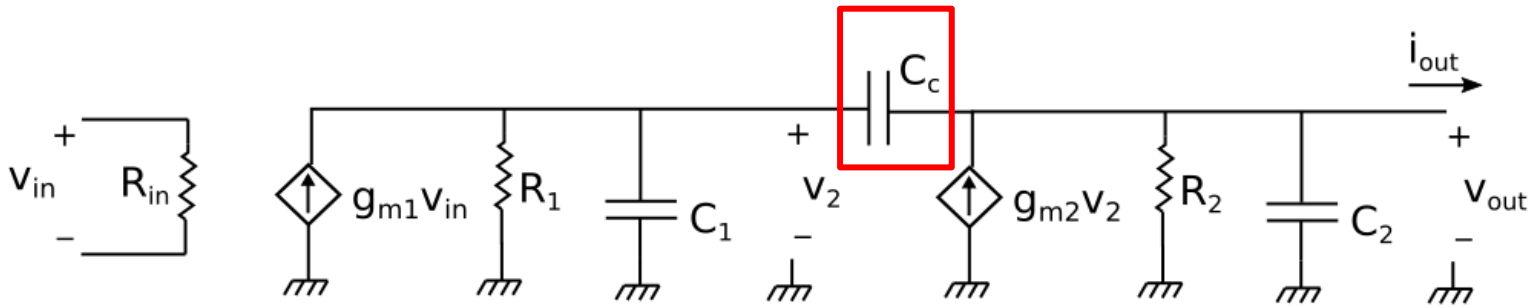


The open-loop frequency response of a negative-feedback loop using an uncompensated opamp and a feedback factor of F(s)=1.

Close to unstability

2. Compensation techniques

- Miller compensation:



$$p_1' = \frac{-1}{g_{m2}R_1R_2C_c} < p_1$$ → First pole is shifted to a lower frequency. DC gain remains.

$$\mathbf{p_2' \approx \frac{-g_{m2}}{C_2}} > p_2$$ → Second pole is shifted to a higher frequency. Phase margin increases.

$$\mathbf{C_2, C_c \gg C_1} \qquad \mathbf{z_1 \approx \frac{g_{m2}}{C_c}}$$ → A positive extra zero is added. Phase margin may be degraded.

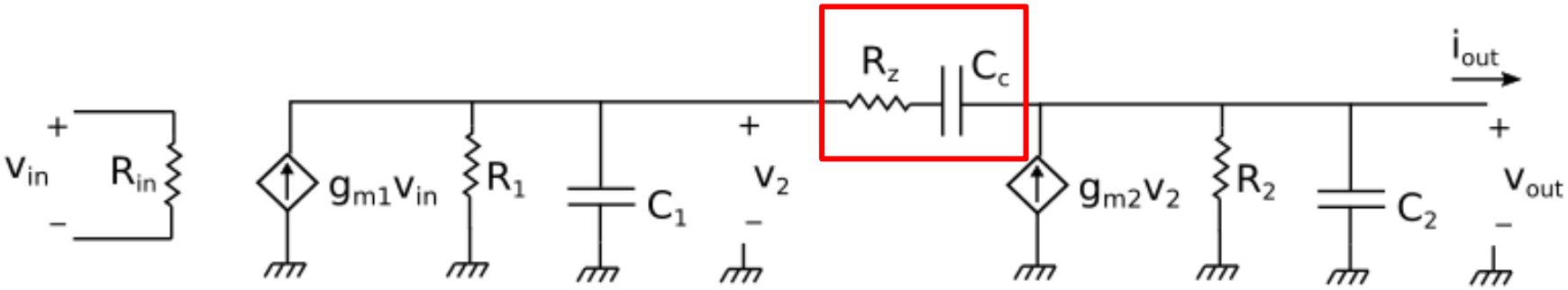
$$\mathbf{GBW \approx {g_{m1}}/{C_C}}$$

Recipe: If z_1 = 10*GBW:

- P_2 = 1.2*GBW → MF = 45º
- P_2 = 2.2*GBW → MF = 60º
  → $C_C = 0.22*C_2$

2. Compensation techniques

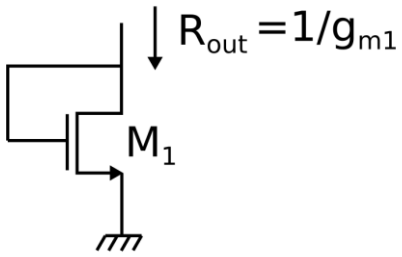
- Miller compensation: now we have a **positive zero that might limit GBW** → it can be compensated with a resistor.

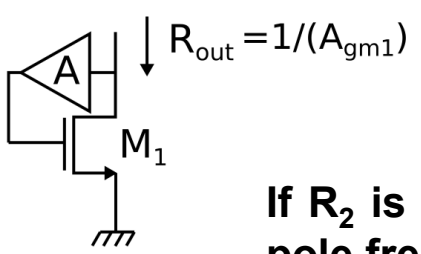


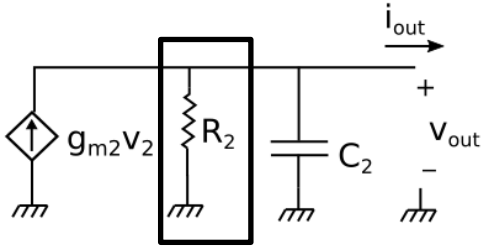
With the resistor we can control the zero frequency. Two options:

1. Remove the zero → $R_z = {}^{1}/_{g_{m2}}$.
2. Make the zero frequency equal to the second pole frequency → $\mathbf{R_z = \frac{C_C+C_2}{C_C}\frac{1}{g_{m2}}}$.

- Another way?



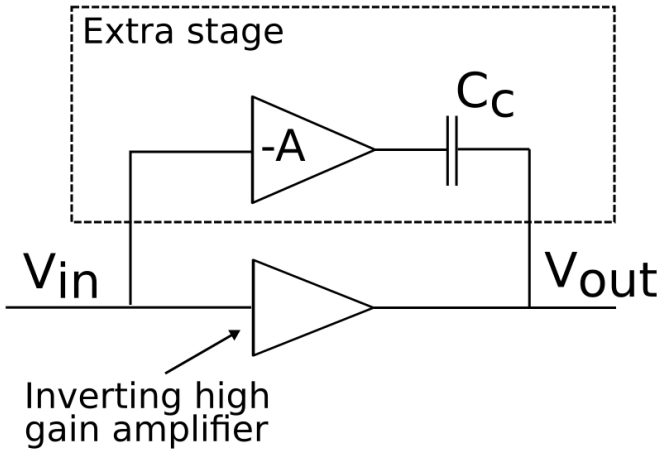


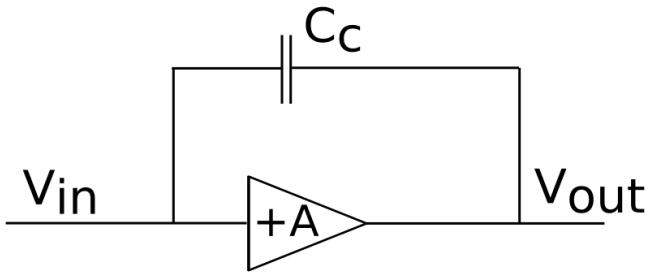


If R_2 is decreased the second pole frequency will increase.

2. Compensation techniques

- Feedforward compensation:

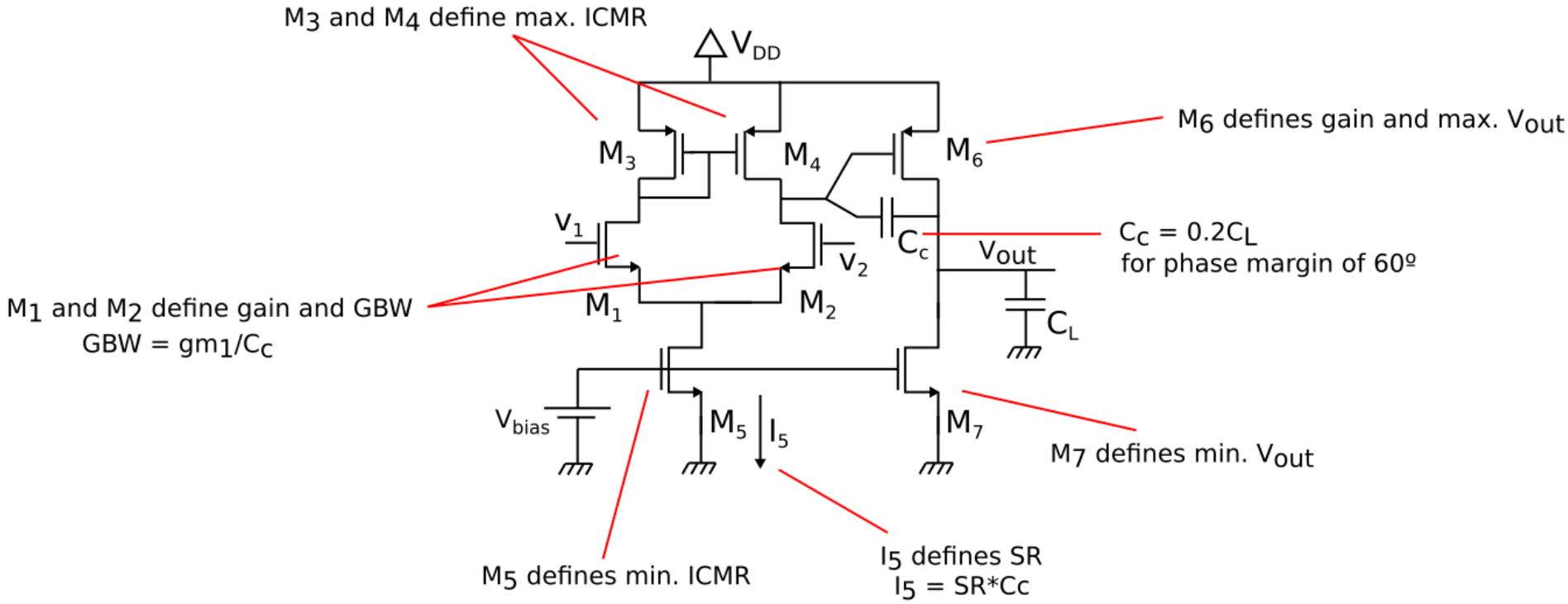




A negative extra zero is added → positive phase shift → phase margin is improved

Compensation technique used in common-drain configurations → C_C is designed to be a short-circuit at high frequencies.

3. Two-stage architecture design



Some tips:

- Gain defined by gm_1, gm_2, gm_6 and bias currents.
- GBW defined by I_5, gm_1 and gm_2.
- Slew-rate defined by I_5.

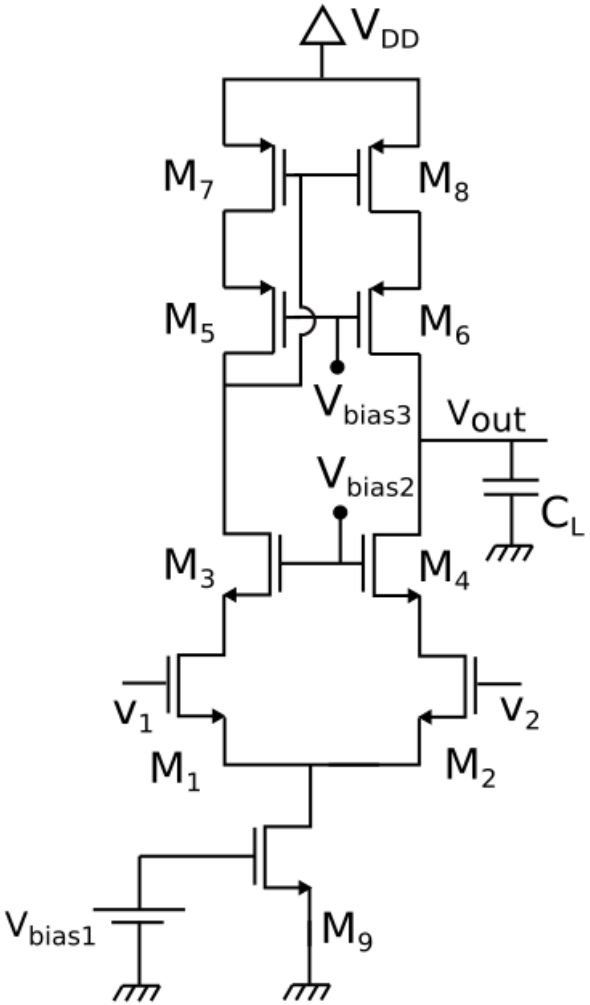
4. Cascode structures

- Two-stage opamp might have either limited gain or bandwidth. Additionally, PSRR is low → cascode-based configurations.
  1. Cascode structure in the first stage.
  2. Cascode structure in the second stage.
  3. Folded-cascode structure.
- Two-stage opamp → how to increase the gain?
  1. Increase the number of stages → higher unstability.
  2. Increase gm in the first or in the second stage.
  3. Increase r_{out} in the first or in the second stage.

  The third option is more energy efficient because the bias currents are decreased.
- Cascode structures → especially suitable for capacitive loads.

4. Cascode structures

1. Cascode structure in the first stage.



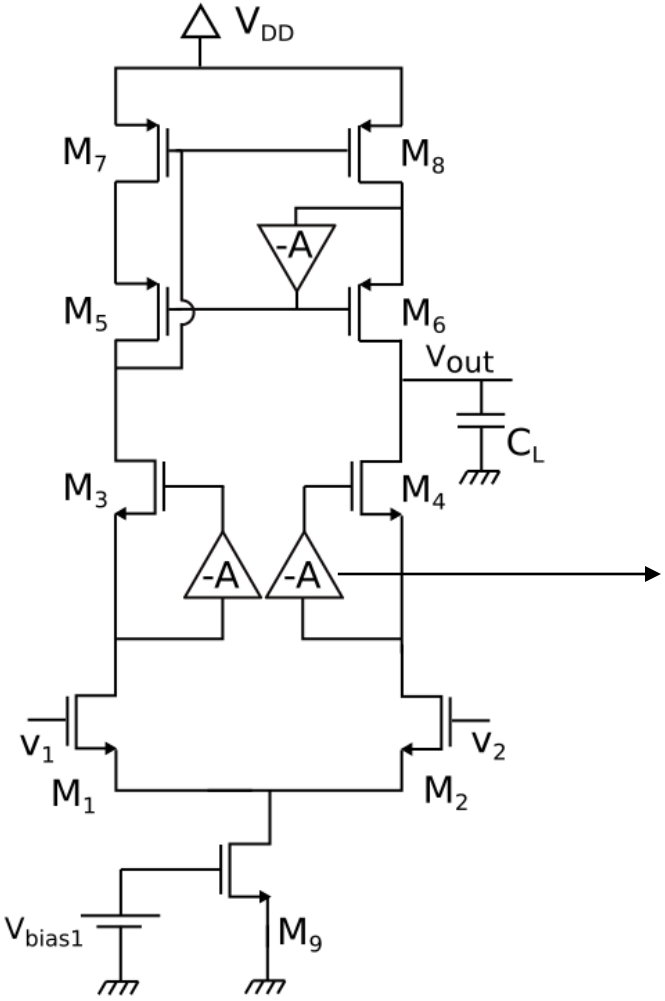
$$A_v = g_{m1} r_{out}$$

$$r_{out} \approx (g_{m4} r_{o4} r_{o2}) || (g_{m6} r_{o6} r_{o8})$$

$$p_1 \approx \frac{1}{r_{out} C_L} \qquad GBW = \frac{g_{m1}}{C_L}$$

4. Cascode structures

1. Cascode structure in the first stage with enhanced r_{out}.



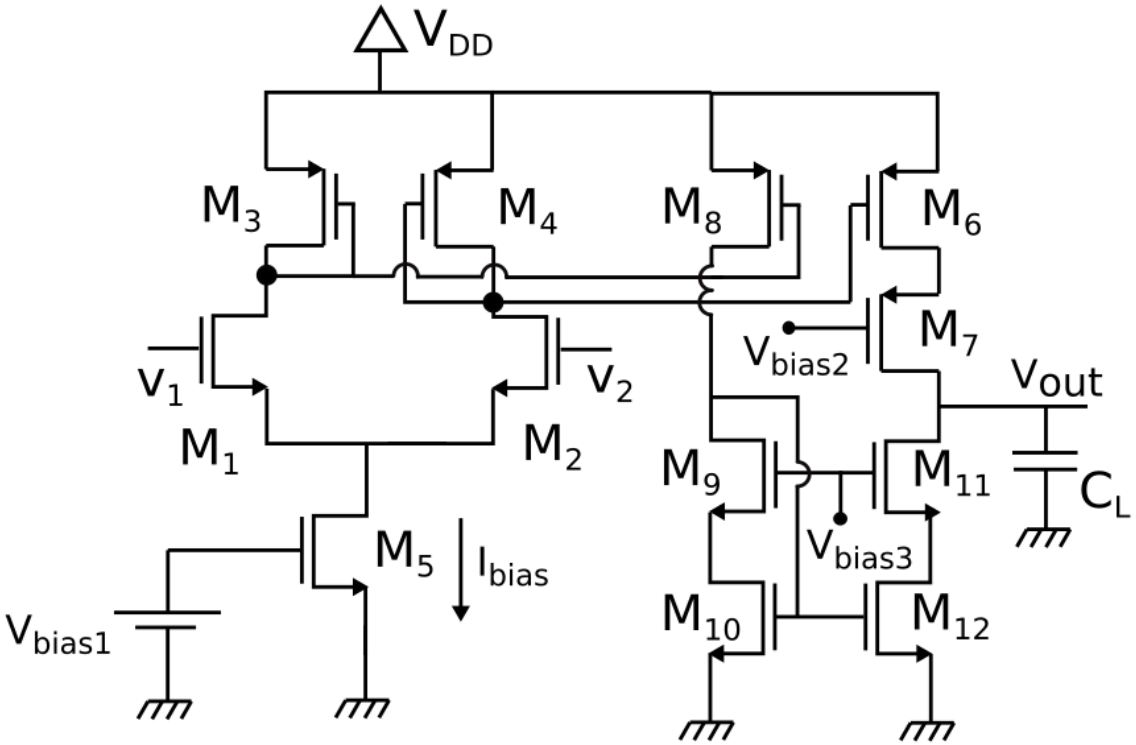
$$A_v = g_{m1} r_{out}$$

$$r_{out} \approx (A g_{m4} r_{o4} r_{o2}) || (A g_{m6} r_{o6} r_{o8})$$

The gain stage can be implemented with a simple common-source configuration

4. Cascode structures

2. Cascode structure in the second stage.



$$A_v = g_{m1} k r_{out}$$

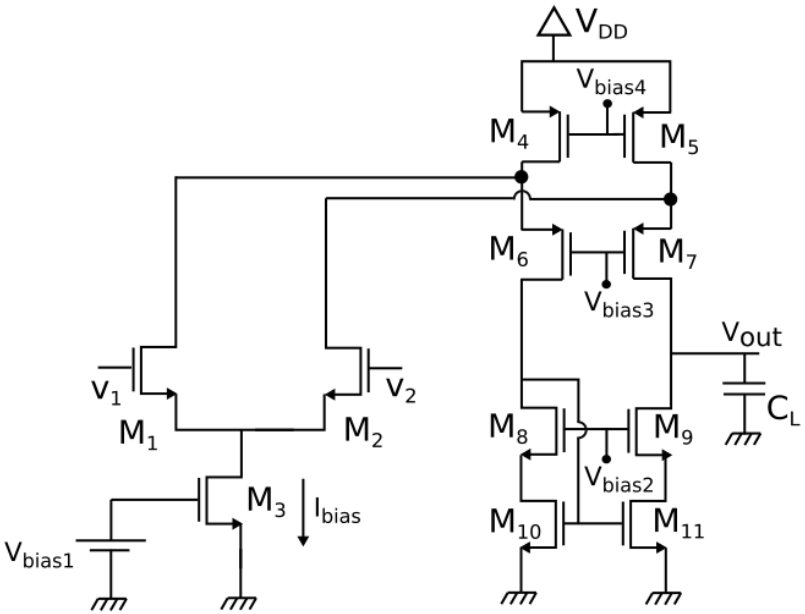
$$k = {g_{m8}}/{g_{m3}} = {g_{m6}}/{g_{m4}}$$

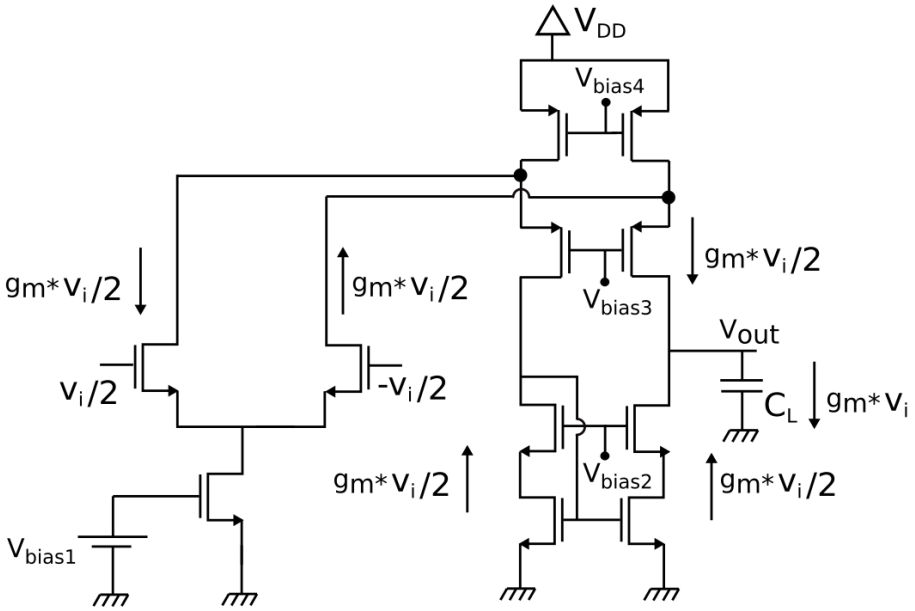
$$r_{out} \approx (g_{m11} r_{o11} r_{o12}) || \; || (g_{m7} r_{o7} r_{o6})$$

The pole of the first stage is located at high frequencies.

4. Cascode structures

3. Folded-cascode structure.





$$r_{out} \approx (g_{m9} r_{o9} r_{o11}) || (g_{m7} r_{o,7} (r_{o5} || r_{o2}))$$

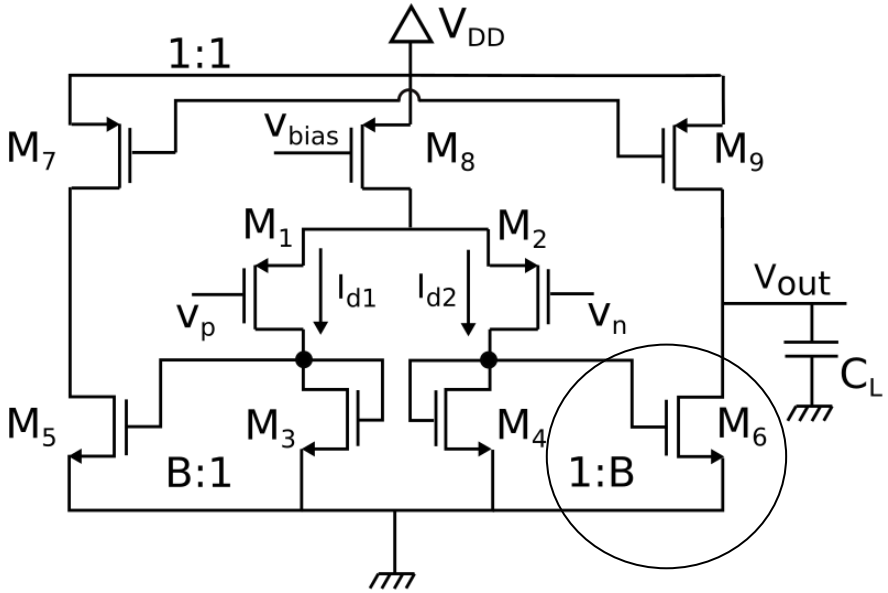
In practice, making all the PMOS and NMOS equal, respectively

$A_v = g_{m1} r_{out}$ ⟶ Maximum achievable gain ⟶ $A_v \approx {}^{3}/_{4}\, g_{m1} r_{out}$

Self-compensated → suitable for high frequency

High ICMR

5. Symmetric CMOS OTA



$$A_v \approx \mathbf{B}g_{m1}R_{out} \qquad R_{out} \approx (r_{o9})||(r_{o6})$$

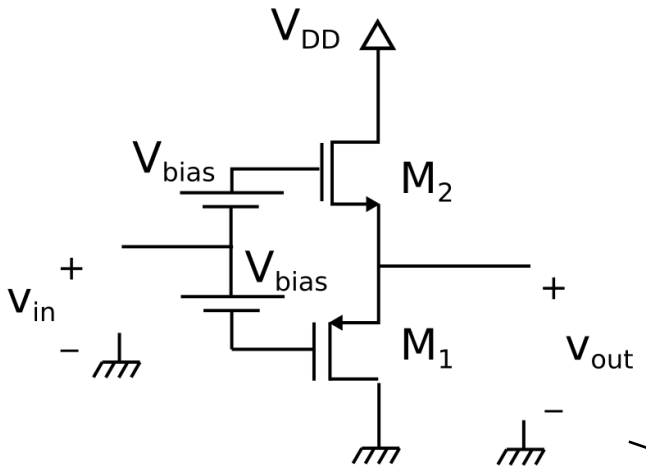
$$BW = \frac{1}{2\pi R_{out}C_L} \qquad GBW = \frac{\mathbf{B}g_{m1}}{2\pi C_L}$$

- Improved gain due to current amplification **B**.
- For wide-band performance → high-speed current amplifiers with large overdrive voltage (V_{GS}-V_{th}) and small L.

Non-dominant's pole at $\frac{g_{m4}}{2\pi C_{n1}}$, where $C_{n1} = (3+B)C_{GS4}$

6. Output stages

- All the structures seen till now have a very high output resistance (in the range of dozens of kΩs) → they only feed moderate capacitive loads and high resistances.
- If we need to feed either high capacitive loads (dozens of pFs) or low resistances (100 Ω) → we need a low output resistance → output stage required.
- Conventional source follower:



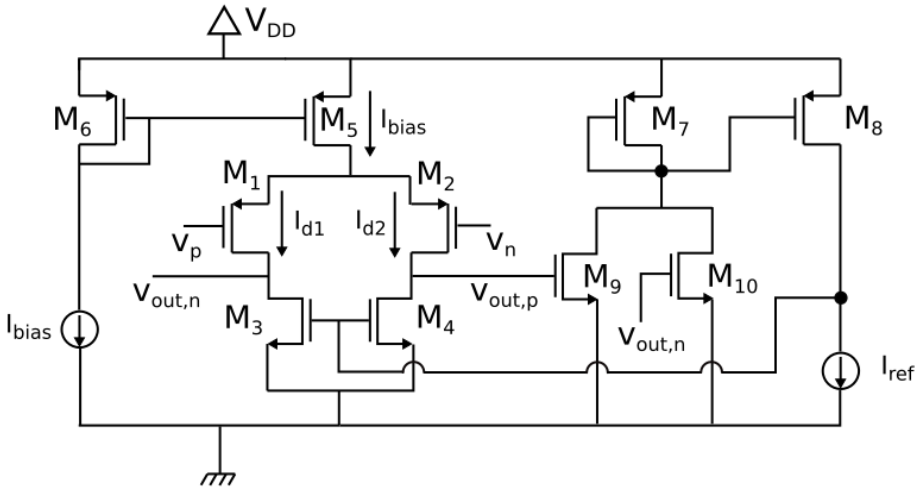
Source follower

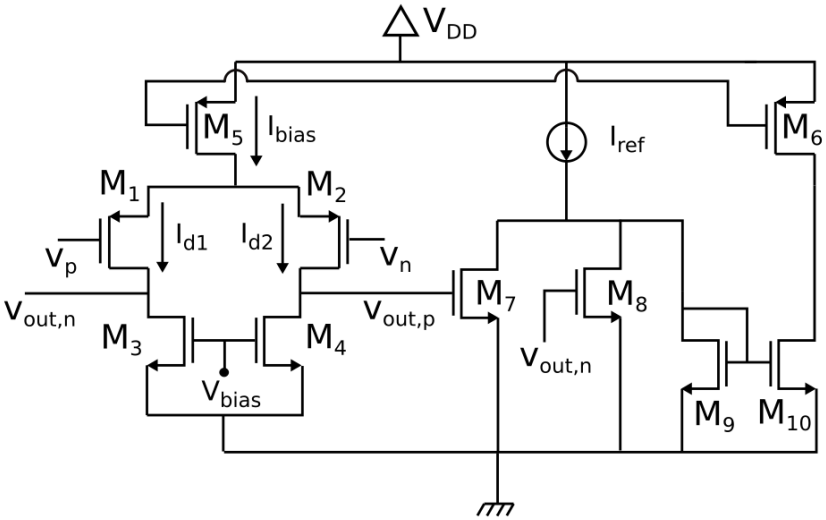
$$A_v = \frac{g_{m1} + g_{m2}}{g_{m1} + g_{m2} + r_{o1} + r_{o2}} \approx 1$$

$$r_{out} \approx \frac{1}{g_{m1} + g_{m2}}$$

AB class → lower power consumption

7. CMFB circuits





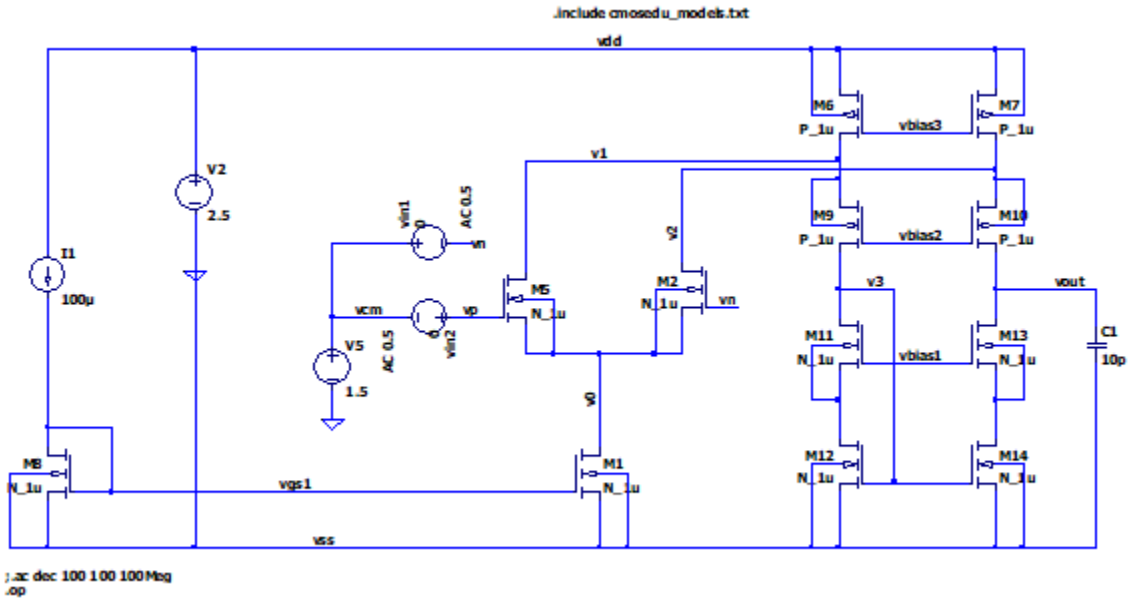
Three tasks:

1. Measure the output voltages.
2. Cancel out the differential signals.
3. Close the CMFB loop.

- CMFB circuit → **unitary gain.**
- It measures the output signal and removes differential component.
- Close-loop feedback → stability issues.
- **CMFB's bandwidth > opamp's bandwidth.**
- It should consume less power than the opamp itself.

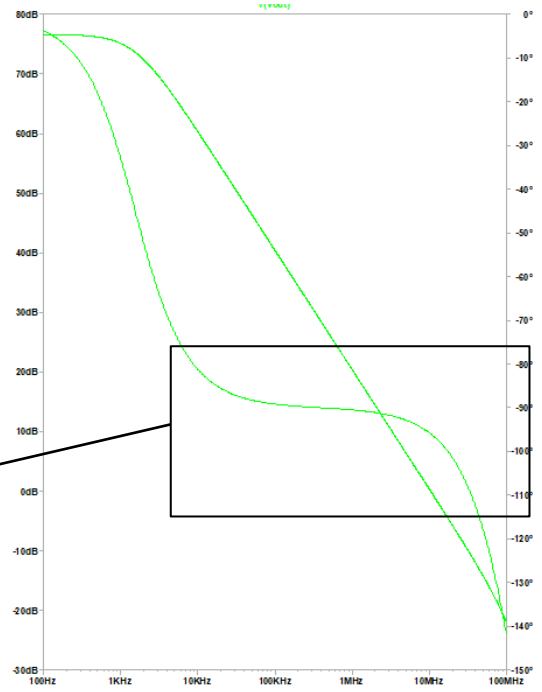
8. Examples

- Folded cascode OTA (1 um):



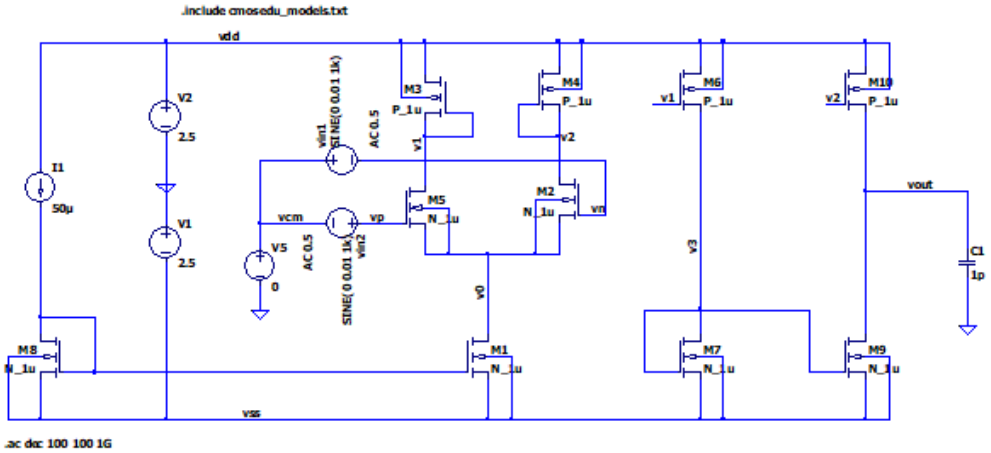

```
--- Operating Point ---

V(v2):          2.22352         voltage
V(vn):          1.5             voltage
V(v0):          0.610514        voltage
V(v1):          2.22352         voltage
V(vp):          1.5             voltage
V(vdd):         2.5             voltage
V(vcm):         1.5             voltage
V(vgs1):        1.38518         voltage
V(vbias3):      1.35            voltage
V(vbias2):      1.11            voltage
V(v3):          1.0617          voltage
V(vout):        1.0617          voltage
V(vbias1):      1.3             voltage
V(n001):        0.240131        voltage
V(n002):        0.240131        voltage
```

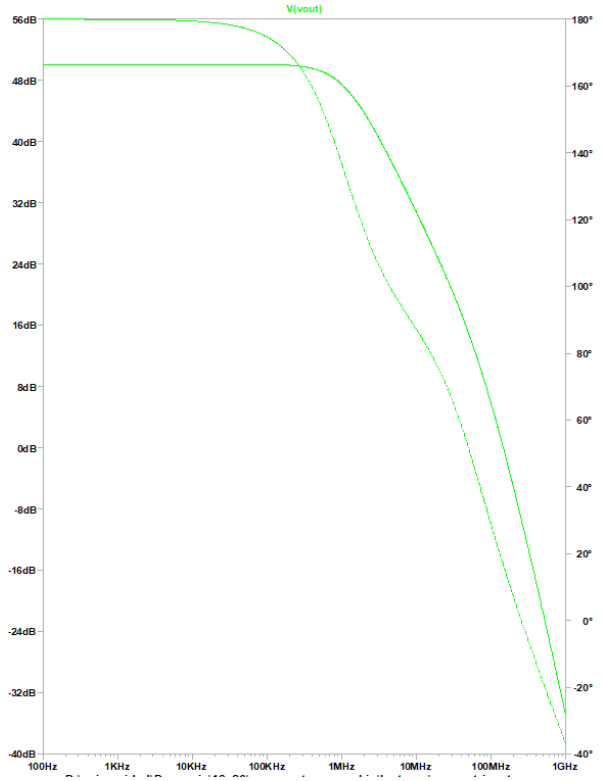
Self-compensated



8. Examples

- Folded cascode OTA (1 um):

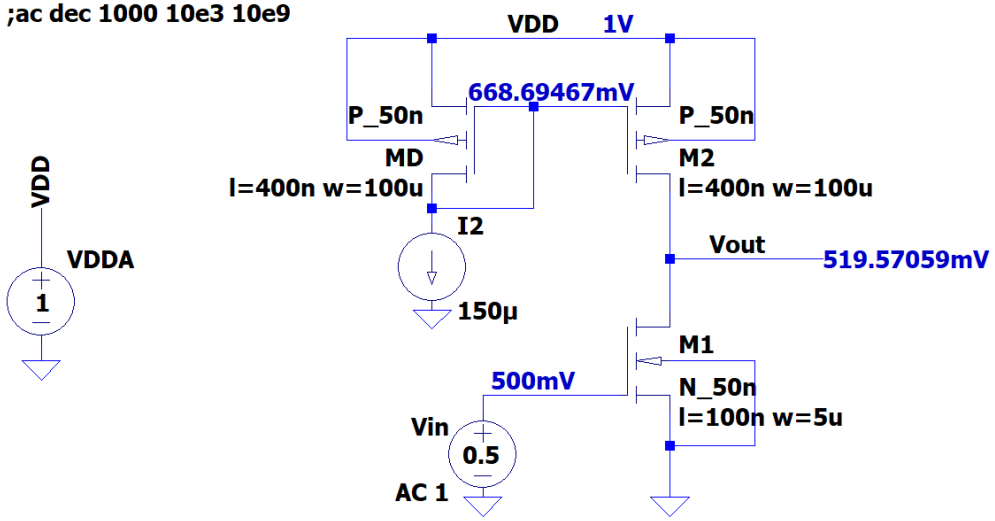




8. Examples

- Simple common-source single-ended amplifier (50 nm):

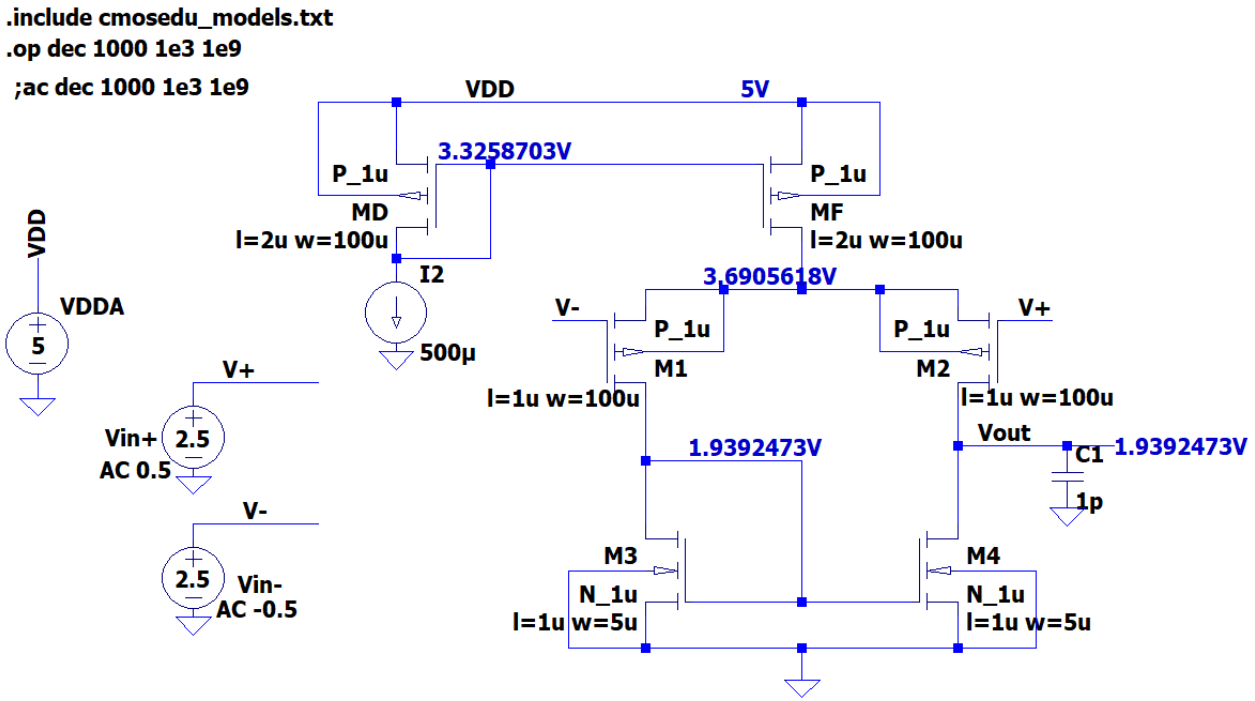
```
.include cmosedu_models.txt
.op dec 1000 10e3 10e9
;ac dec 1000 10e3 10e9
```



Name:	m1	m2	md
Model:	n_50n	p_50n	p_50n
Id:	1.54e-04	-1.54e-04	-1.50e-04
Vgs:	5.00e-01	-3.31e-01	-3.31e-01
Vds:	5.20e-01	-4.80e-01	-3.31e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00
Vth:	3.62e-01	-2.48e-01	-2.48e-01
Vdsat:	1.41e-01	-1.14e-01	-1.14e-01
Gm:	1.41e-03	1.97e-03	1.93e-03
Gds:	5.34e-05	2.50e-05	2.93e-05
Gmb	4.20e-04	6.32e-04	6.17e-04
Cbd:	4.36e-15	8.79e-14	9.10e-14
Cbs:	5.00e-15	1.00e-13	1.00e-13

8. Examples

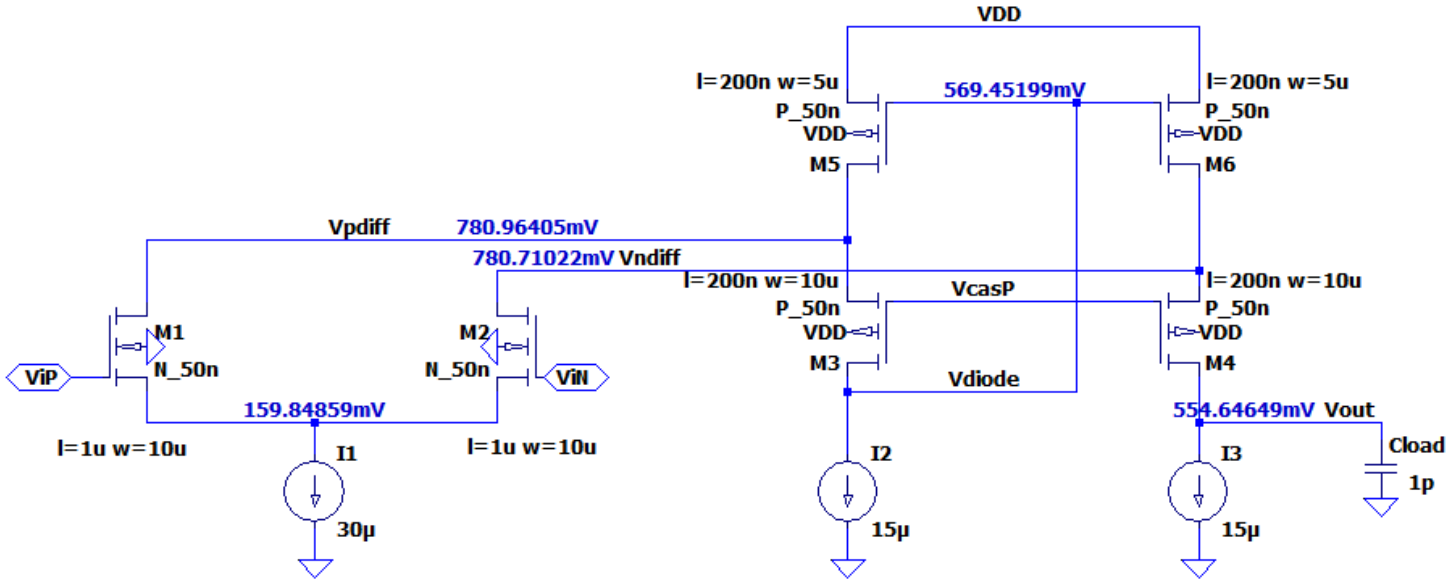
- Differential pair (1 um):



Name:	m3	m4	m2	m1	mf
Model:	n_1u	n_1u	p_1u	p_1u	p_1u
Id:	2.48e-04	2.48e-04	-2.48e-04	-2.48e-04	-4.95e-04
Vgs:	1.94e+00	1.94e+00	-1.19e+00	-1.19e+00	-1.67e+00
Vds:	1.94e+00	1.94e+00	-1.75e+00	-1.75e+00	-1.31e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	8.42e-01	8.42e-01	-8.92e-01	-8.92e-01	-9.29e-01
Vdsat:	6.63e-01	6.63e-01	-2.80e-01	-2.80e-01	-6.27e-01
Gm:	3.08e-04	3.08e-04	1.27e-03	1.27e-03	1.09e-03
Gds:	6.79e-05	6.79e-05	3.49e-05	3.49e-05	3.09e-05

8. Examples

- Simple folded-cascode (1 um):



Name:	m3	m4	m5	m6	m2
Model:	p_50n	p_50n	p_50n	p_50n	n_50n
Id:	-1.50e-05	-1.50e-05	-3.00e-05	-3.00e-05	1.50e-05
Vgs:	-3.81e-01	-3.81e-01	-4.31e-01	-4.31e-01	3.40e-01
Vds:	-2.12e-01	-2.26e-01	-2.19e-01	-2.19e-01	6.21e-01
Vbs:	2.19e-01	2.19e-01	0.00e+00	0.00e+00	-1.60e-01
Vth:	-3.32e-01	-3.32e-01	-2.78e-01	-2.78e-01	2.72e-01
Vdsat:	-9.95e-02	-9.93e-02	-1.64e-01	-1.64e-01	9.36e-02
Gm:	2.26e-04	2.26e-04	2.68e-04	2.68e-04	1.98e-04
Gds:	5.73e-06	5.19e-06	1.76e-05	1.75e-05	4.82e-06

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Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.