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Unit 6. Comparators

System-on-Chip and efficient electronic circuit integration techniques

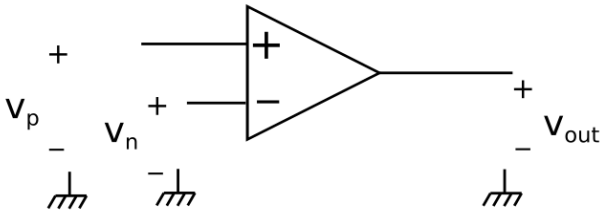
Carlos III University of Madrid, Spain

Electronics Technology Department

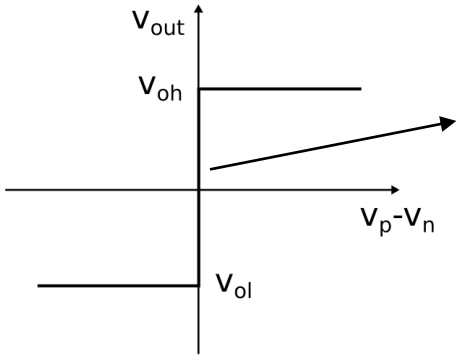
Outline

1. Basic concepts
2. Open-loop comparators
3. Hysteresis
4. Regenerative or latched comparators

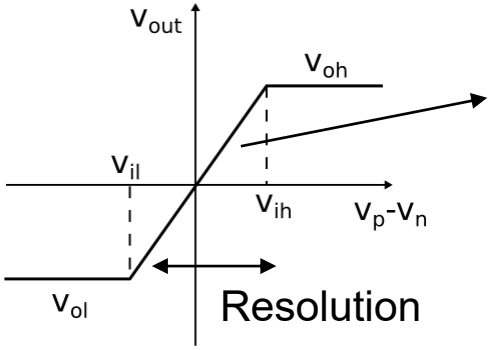
1. Basic concepts



- A comparator is defined as a circuit with a binary output V_{out} whose value depends on the comparison between two inputs V_p and V_n.



Infinite gain



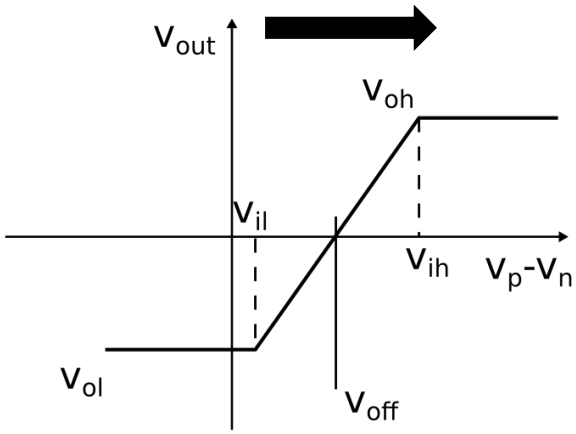
Finite gain

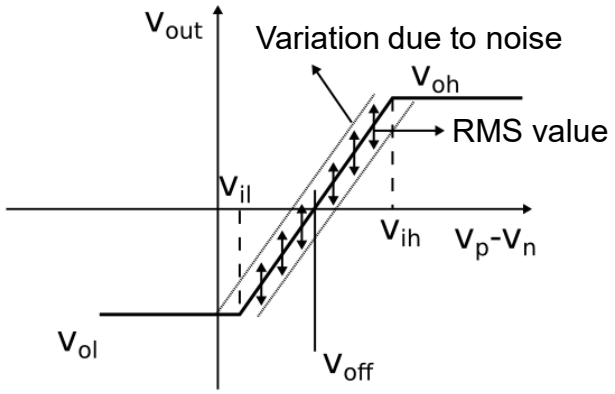
$$A_V = \frac{v_{oh} - v_{ol}}{v_{ih} - v_{il}}$$

$$v_{out} = \begin{cases} v_{oh} \text{ si } v_p > v_n \\ v_{ol} \text{ si } v_p < v_n \end{cases}$$

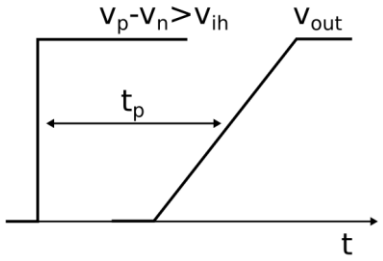
$$v_{out} = \begin{cases} v_{oh} \text{ si } v_p - v_n > v_{ih} \\ A_V(v_p - v_n) \text{ si } v_{il} < v_p - v_n < v_{ih} \\ v_{ol} \text{ si } v_p - v_n < v_{il} \end{cases}$$

1. Basic concepts





- The curve is usually not centered at zero → input offset (V_{off}) → highly dependent parameter.
- ICMR: range of DC input voltage to have the devices working in saturation → similar to amplifiers.
- Noise in comparators is of special relevance due to random variations in the gain→ jitter issues and resolution losses in data converters.



- Propagation delay (tp) is limited by two phenomena:
  1) Frequency response.
  2) SR: the highest current available.

1. Basic concepts

1) Frequency response:

Assuming a first-order filter with dominant pole → $t_p = \frac{1}{2\pi f_p} \ln \frac{2k}{2k-1}$

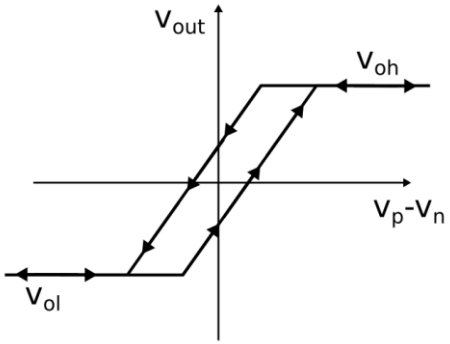
$$k = \frac{v_p - v_n}{(v_p - v_n)_{mín}}$$

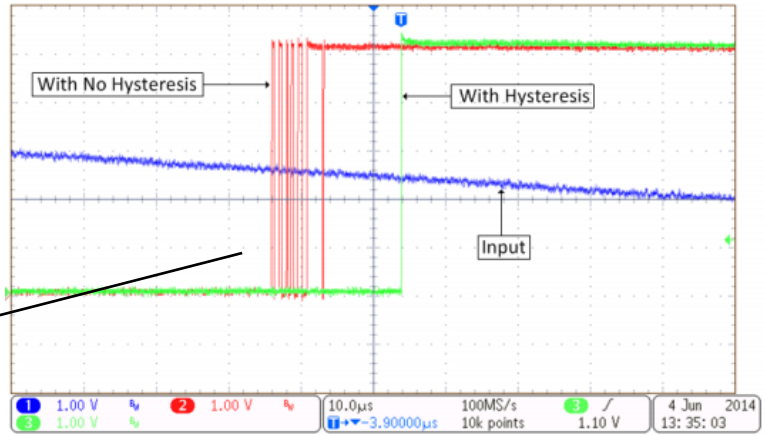
2) SR: $t_p = \frac{v_{oh} - v_{ol}}{2SR}$

The propagation delay varies with the input signal V_p-V_n →

The highest the V_p-V_n the lowest the propagation delay with a minimum one defined by SR.

- Hysteresis:

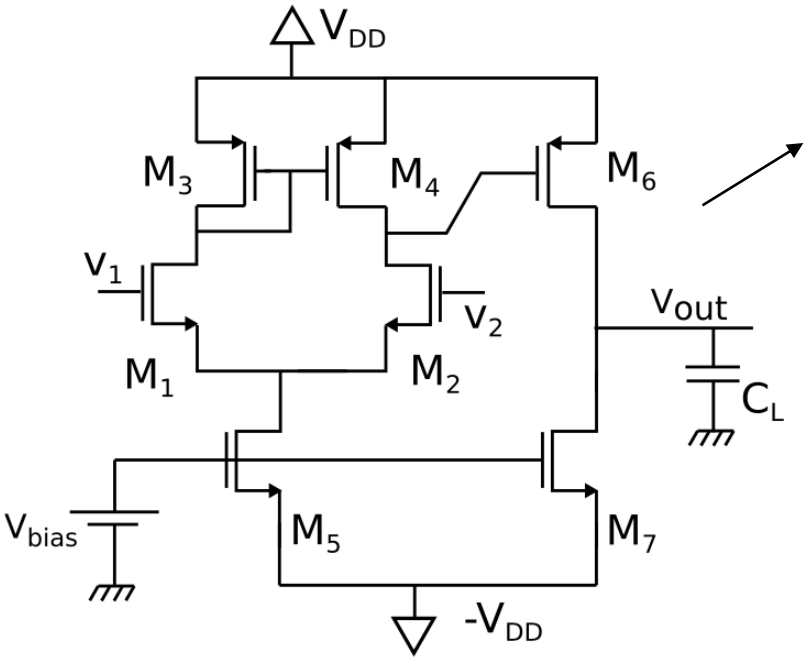




Hysteresis help avoid fast transitions due to noise

2. Open-loop comparators

- What do we need for a comparator? → A differential input stage and enough gain → for instance, Miller opamp accomplishes with these requirements.
- Amplifiers **with no compensation circuitry** to avoid limiting bandwidth and enable a faster response.



V_{oh} → se alcanza cuando M6 no está en saturación

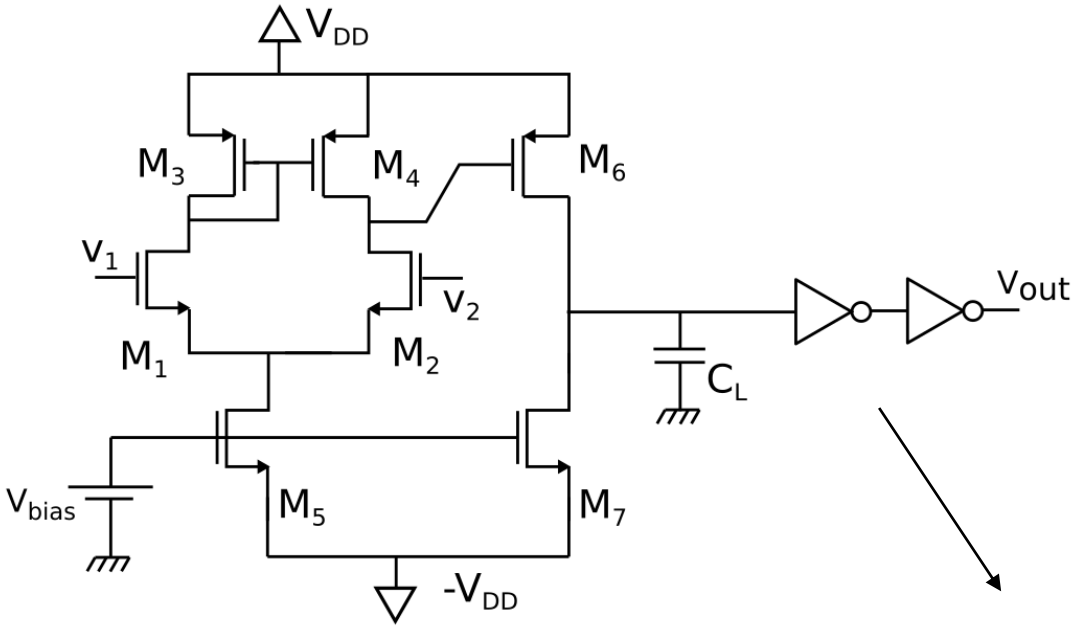
V_{ol} → $-V_{DD}$

DC gain → similar to opamp

$$v_{mín} = \frac{v_{oh} - v_{ol}}{\text{Ganancia(DC)}}$$

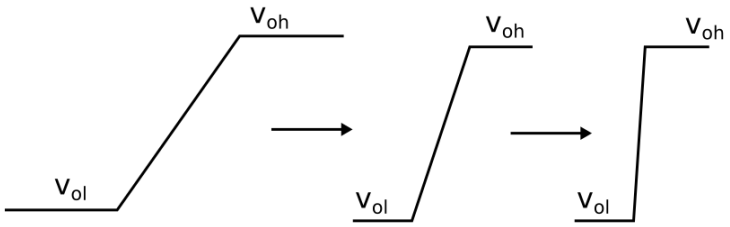
2. Open-loop comparators

- To improve resolution, we can use digital buffers at the output:



- High ICRM
- High power consumption
- High offset and propagation delay

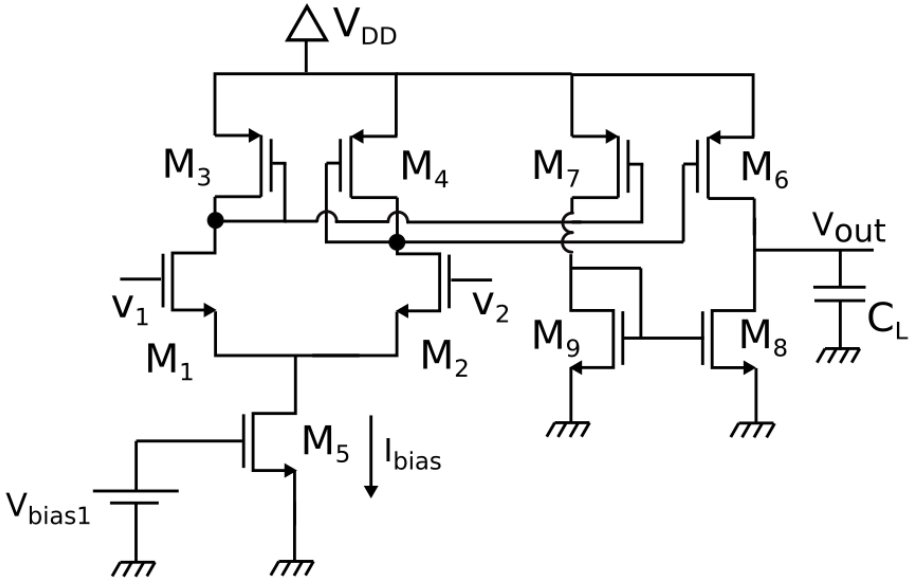
Aspect ratio increases: with a factor of 2.72 → best solution in delay
Higher aspect ratio → to reduce the number of stages



This way we can feed high C_L

2. Open-loop comparators

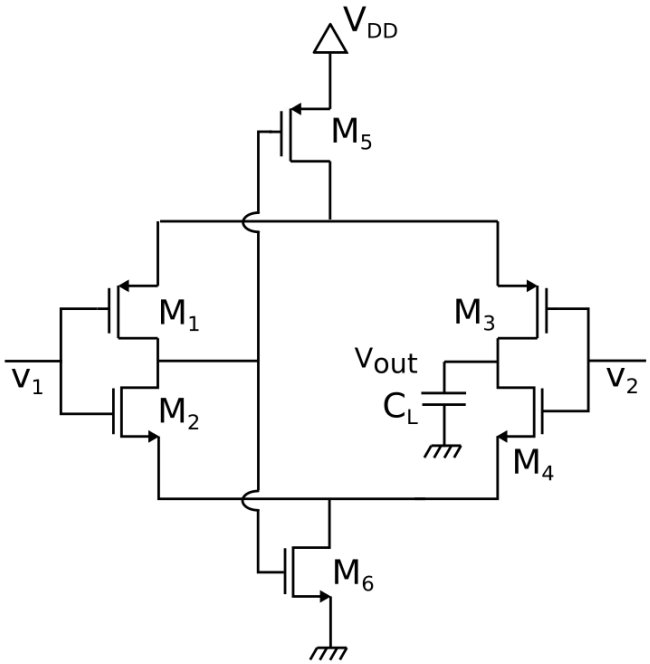
- Push-pull architecture:



- High current in C_L.
- High output resistance → slow comparator due to a pole in the second stage.

2. Open-loop comparators

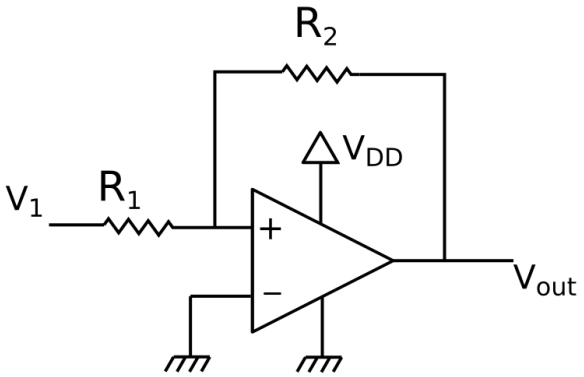
- Self-supply architecture:



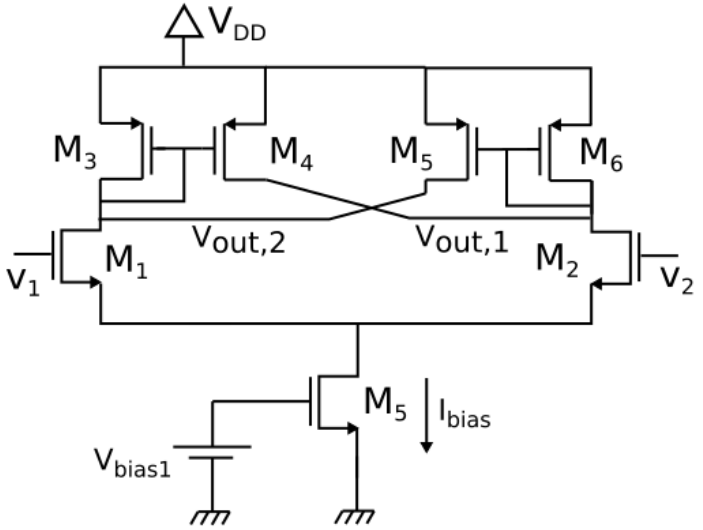
- High current in C_L, with lower power consumption.
- Asymmetry, lower propagation delay from the negative input (V_2).

3. Hysteresis

- External hysteresis: with positive feedback.

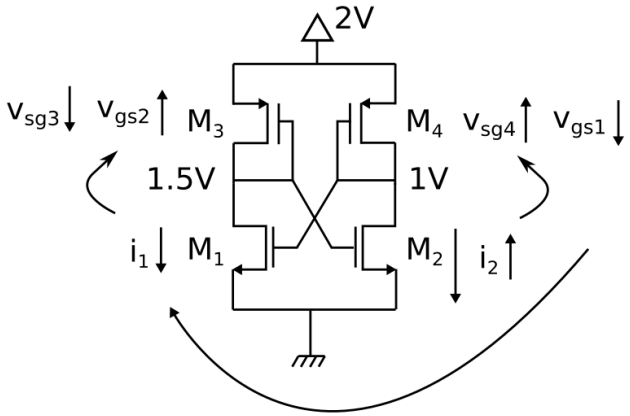


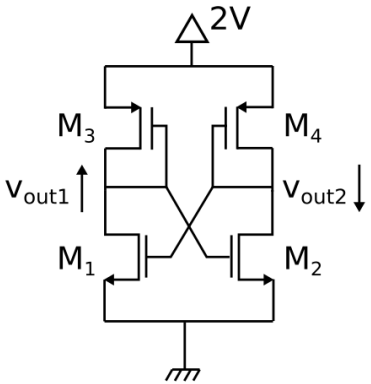
- Internal hysteresis: with positive feedback.

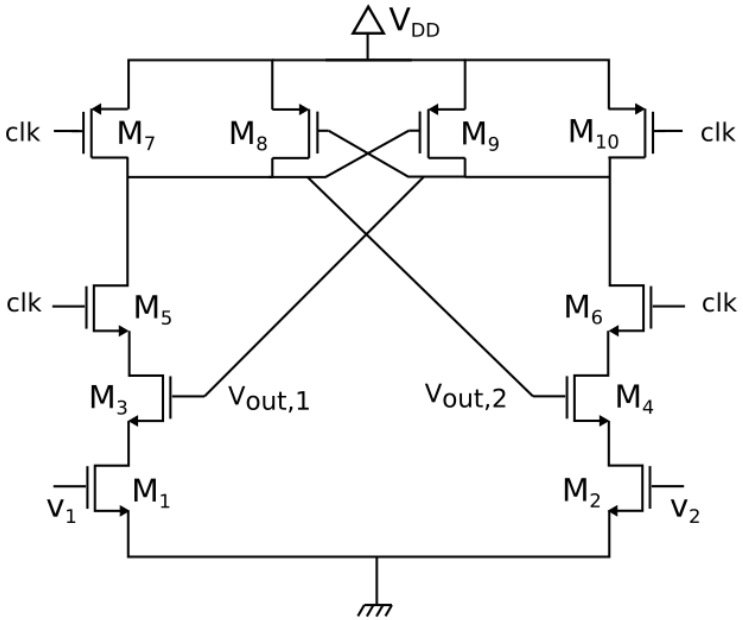


4. Regenerative or latched comparators

- They make use of a positive feedback.
- Two phases consecutive in time: firstly, the value of the inputs is stored and the comparison between them is started, and secondly, the comparison is finished.
- To distinguish between both phases a clock signal is used.

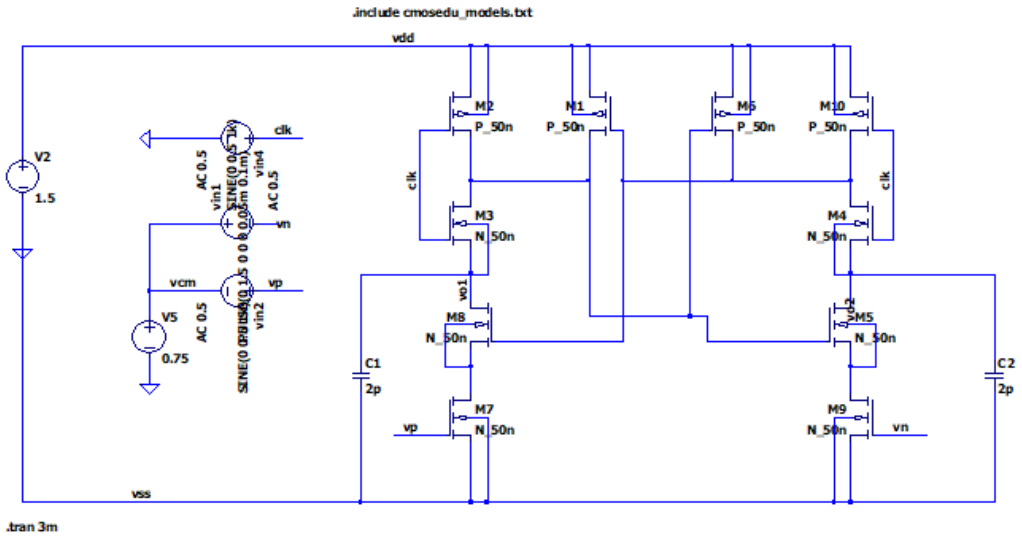


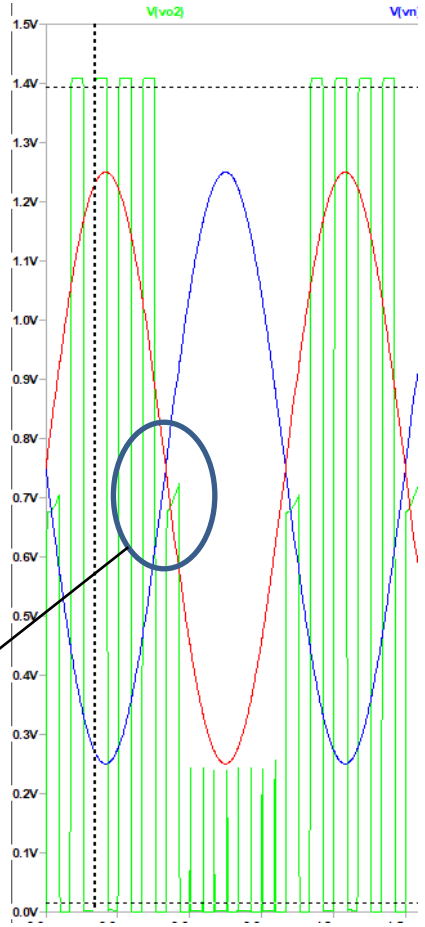




4. Regenerative or latched comparators

- Example in 50-nm:



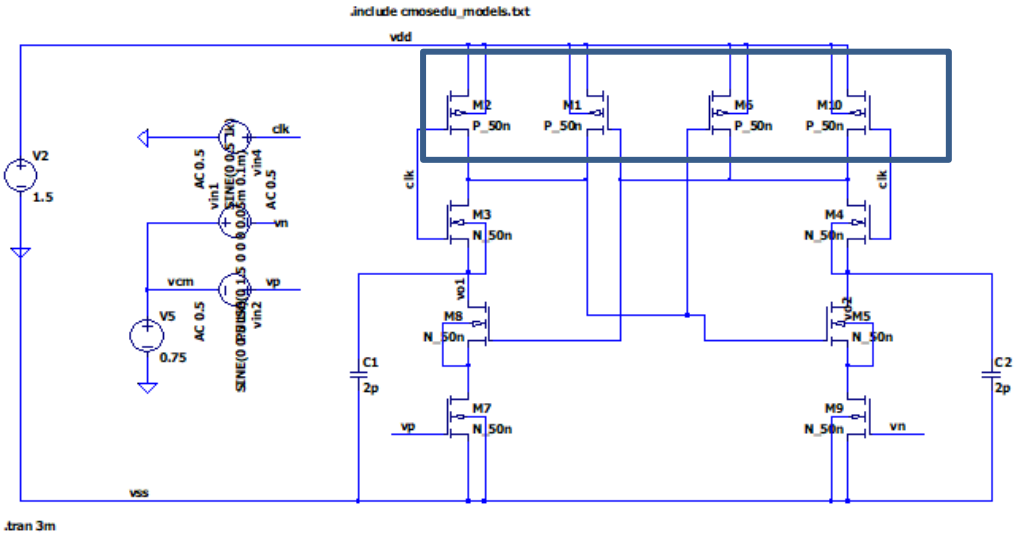


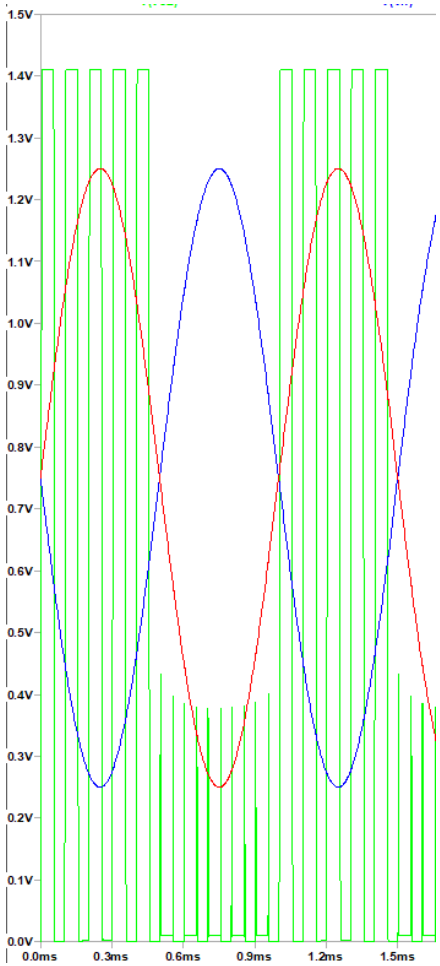
Finite gain

4. Regenerative or latched comparators

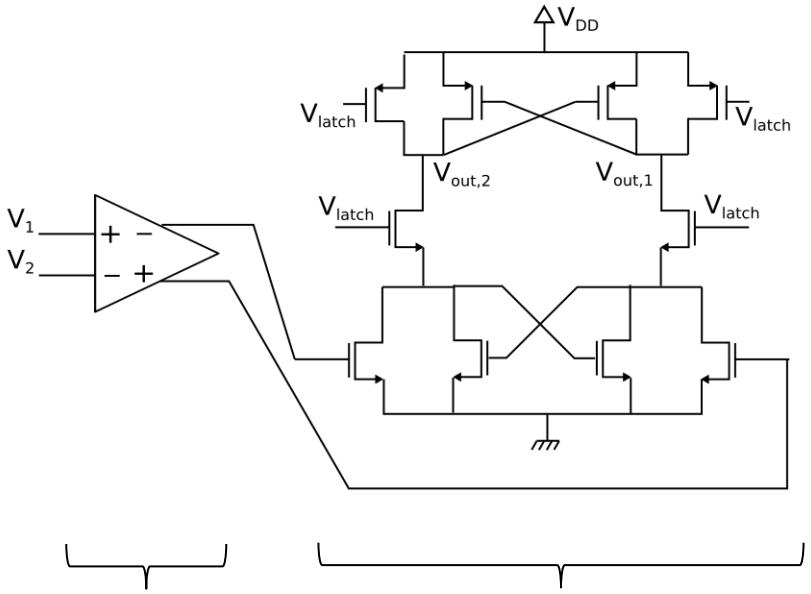
- Example in 50-nm:

Increased W/L





4. Regenerative or latched comparators



It is the most common structure nowadays.
The preamplifier is just a differential pair or a buffer with small gain (10 or so)
A switched capacitor input can still be used to mitigate offset and 1/f noise.

Simple preamplifier to mitigate kickback and reduce requirements of latch stage. The latch stage alternates between a reset phase and a positive feedback phase that quickly generates saturated digital signals.

Bibliography

- Allen, P. E., & Holberg, D. R. (2002). CMOS analog circuit design. New York: Oxford University Press.
- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Simulations are performed through software LTSPice, provided courtesy of Analog Devices and authored by Mike Engelhardt.

Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.