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Unit 7. Inverter-based circuits

System-on-Chip and efficient electronic circuit integration techniques

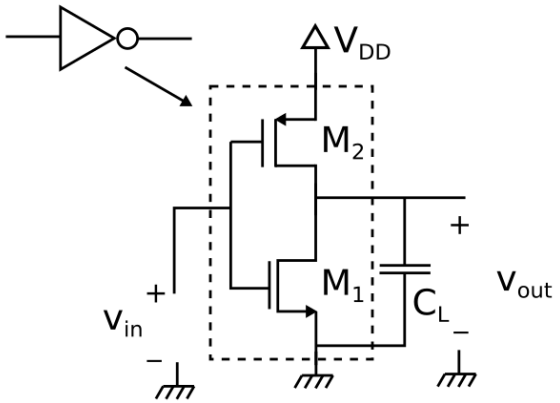
Carlos III University of Madrid, Spain

Electronics Technology Department

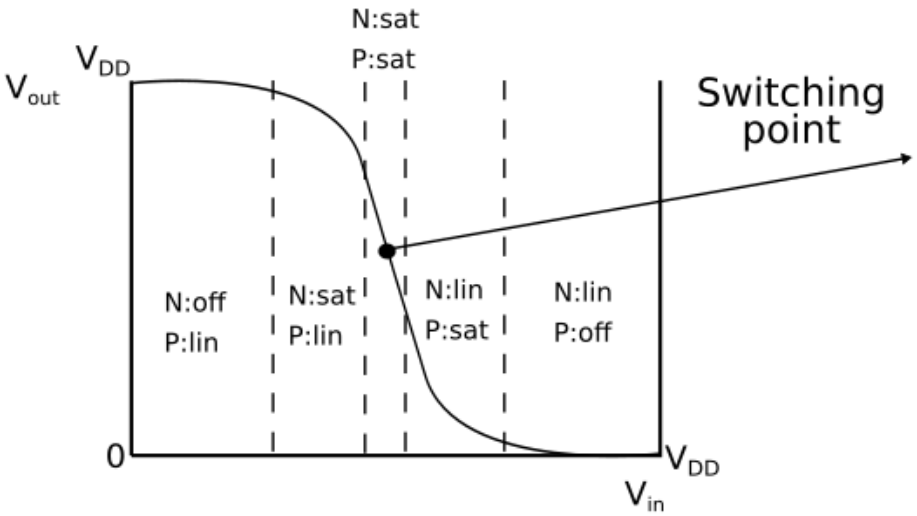
Outline

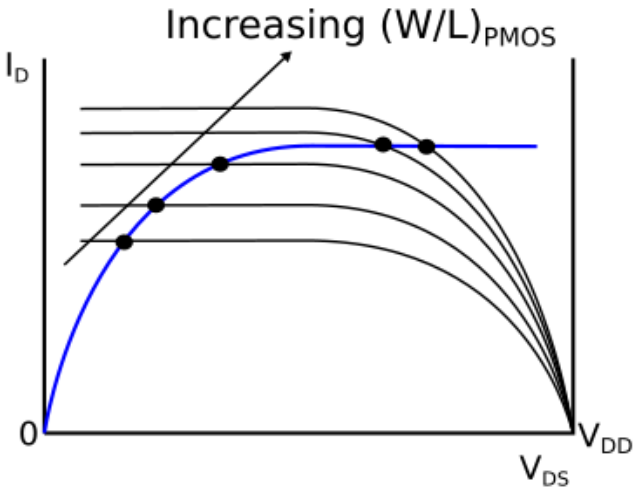
1. The CMOS inverter cell
2. The ring-oscillator
3. Buffers
4. Distributed drivers
5. Digital-Phase Locked Loops (DPLLs)
6. Delay Locked Loops (DLLs)
7. VCO-ADCs
8. Time-to-Digital Converters (TDCs)

1. The CMOS inverter cell

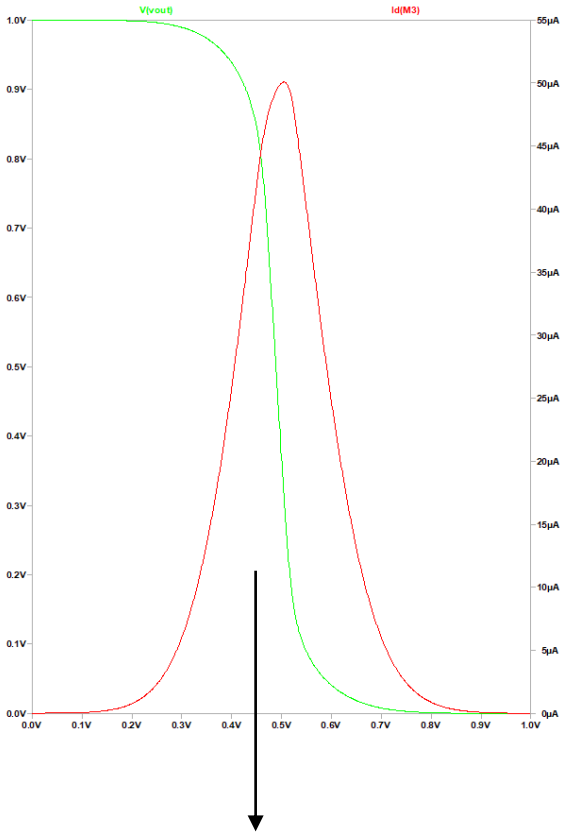


- It performs an inverter digital logic operation.
- Unlike other logic families, it is a rail-to-rail circuit.
- Only dynamic power consumption at the switching times.
- M1 and M2 can be sized to give equal sourcing and sinking capabilities → rising and falling times similar.



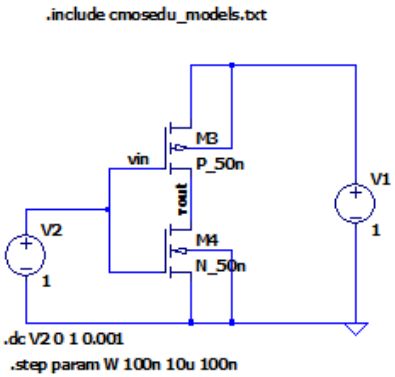


1. The CMOS inverter cell

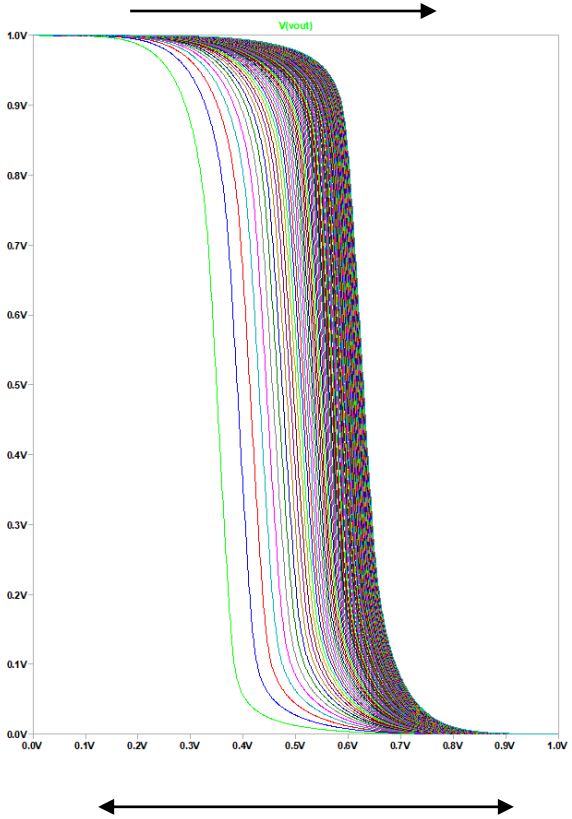


Only power consumption when switching

If input transition is fast → low power consumption



Increasing $(W/L)_{PMOS}$



Switching output is limited to $[V_{thn}, V_{DD}-V_{thp}]$

1. The CMOS inverter cell

- For long-channel devices (L>120 nm) → to establish the switching point at $V_{DD}/2$:

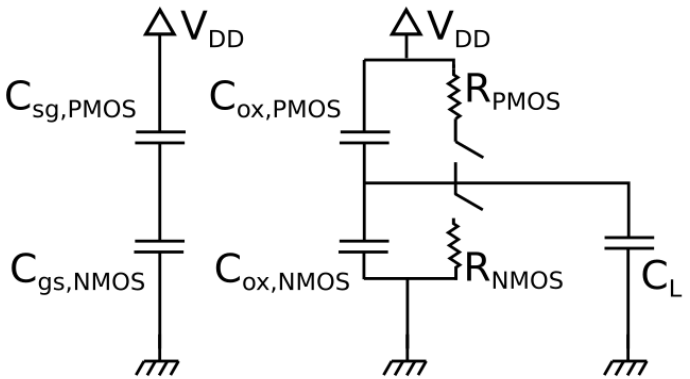
$$\frac{W}{L}_{PMOS} = 3\frac{W}{L}_{NMOS}$$

because $K_N = 3K_P$

- For short-channel devices (L<120 nm) → to establish the switching point at $V_{DD}/2$:

$$\frac{W}{L}_{PMOS} = 2\frac{W}{L}_{NMOS}$$

- Switching characteristics:

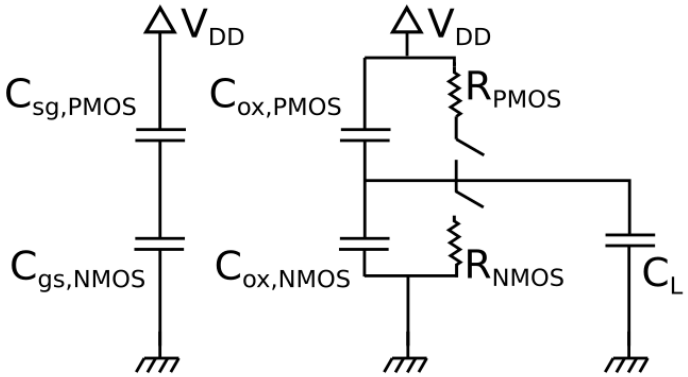


The higher W/L the faster the CMOS inverter

$$t_{ph} = 0.7R_{PMOS}\left(C_{ox,PMOS} + C_{ox,NMOS} + C_L\right)$$

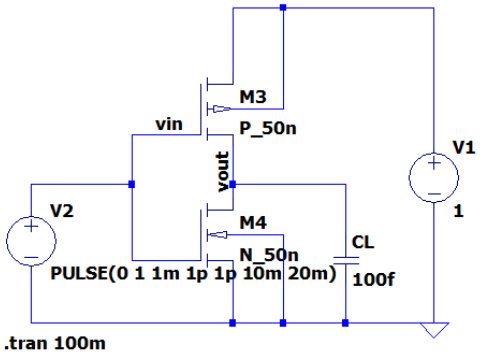
$$t_{pl} = 0.7R_{NMOS}\left(C_{ox,PMOS} + C_{ox,NMOS} + C_L\right)$$

1. The CMOS inverter cell



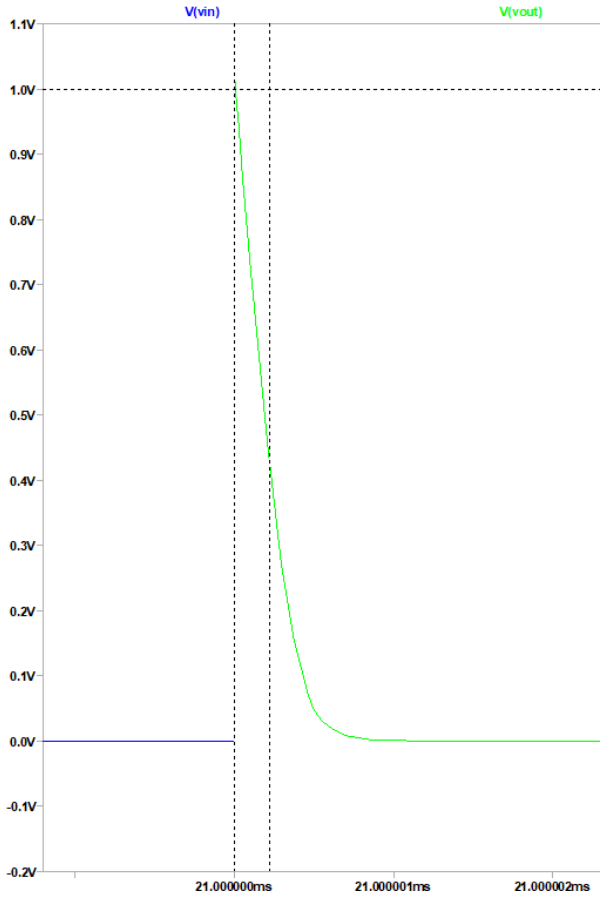
Capacitance	Off	Linear	Saturation
C_{GS}	$C_{ov}\cdot W$	$\mathbf{0{,}5\cdot C_{ox}\cdot W\cdot L}$	$\mathbf{(2/3)\cdot C_{ox}\cdot W\cdot L}$
C_{GD}	$C_{ov}\cdot W$	$\mathbf{0{,}5\cdot C_{ox}\cdot W\cdot L}$	$\mathbf{C_{ov}\cdot W}$
C_{GB}	$C_{ox}\cdot W\cdot L$	CGBO·L	CGBO·L
C_{DB}	C_{jd}	C_{jd}	C_{jd}
C_{SB}	C_{js}	C_{js}	C_{js}

1. The CMOS inverter cell

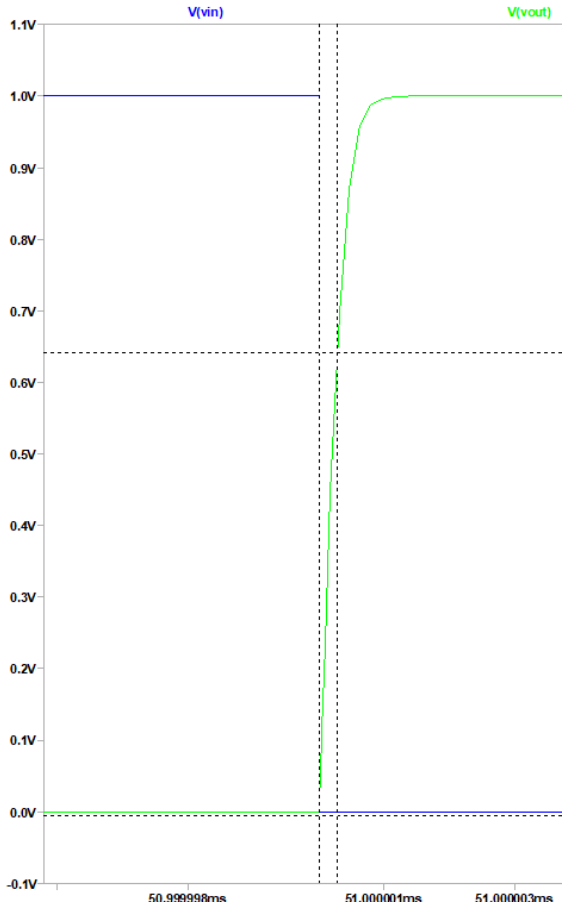


W/L_{PMOS}= 1u/50n

W/L_{NMOS}= 500n/50n

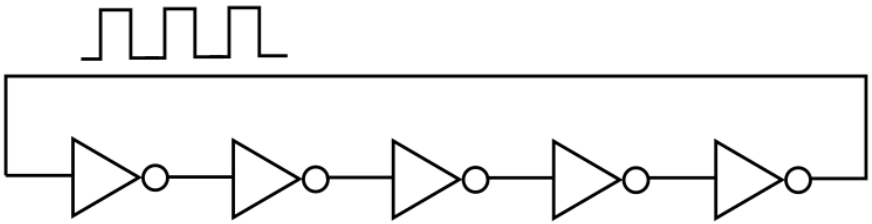


t_{pl} = 215 ps



t_{ph} = 280 ps

2. The ring-oscillator

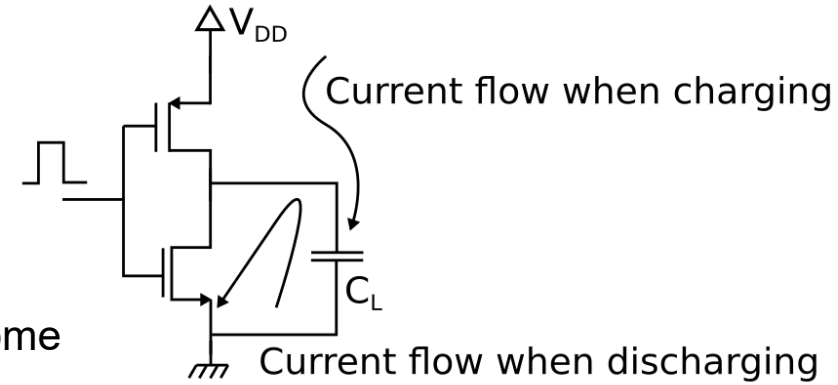


$$f_{osc} = \frac{1}{N \cdot (t_{ph} + t_{pl})}$$

$$t_{ph} + t_{pl} = 0.69 \cdot (R_{PMOS} + R_{NMOS})(C_{in} + C_{out})$$

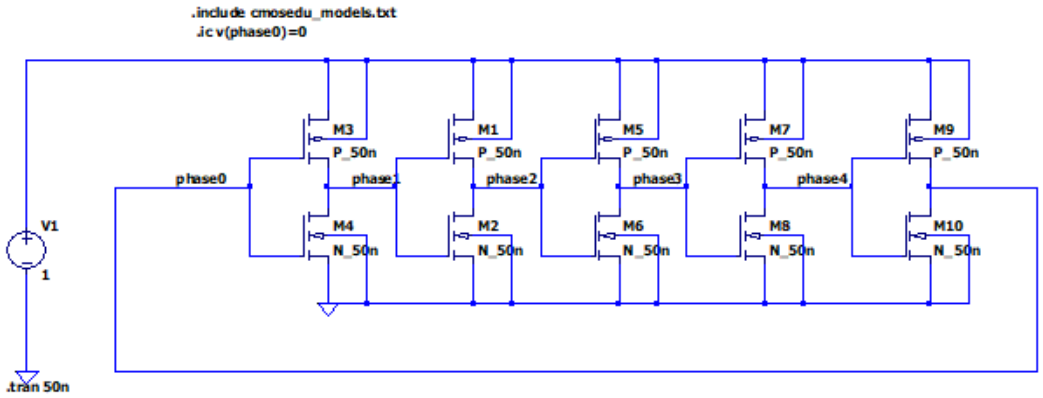
$$\propto \mathbf{WL\ scale^2}$$

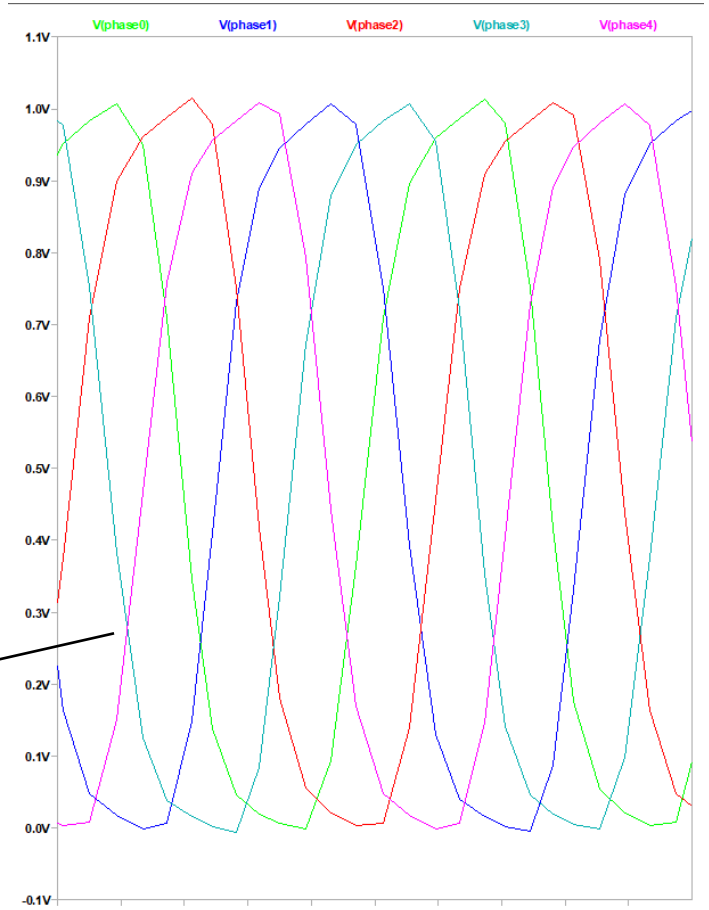
- Very basic block to implement clock signals.
- Also used to measure PVT variations on a wafer/chip.
- $P = C_T V_{DD}^2 f_{osc}$



Jitter due to thermal noise is an issue to overcome

2. The ring-oscillator

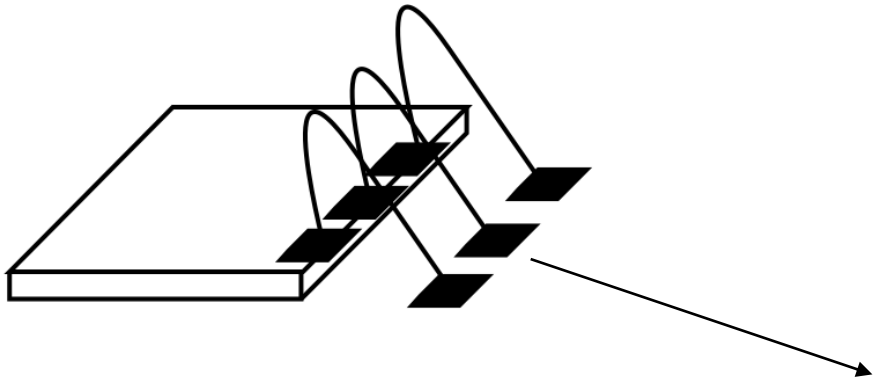


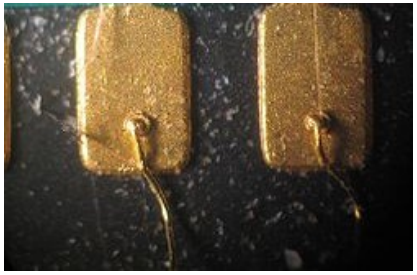


Phases are uniformly distributed in time

$T_d = 231\ ps$ $f_{osc} = 4.3\ GHz$

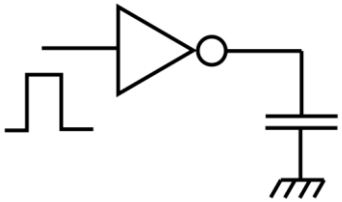
3. Buffers





Chip pads: used to interface the CMOS logic within the IC to the outside world.

→ the simplest circuit for them is a large capacitance (between 20 and 100 pF)



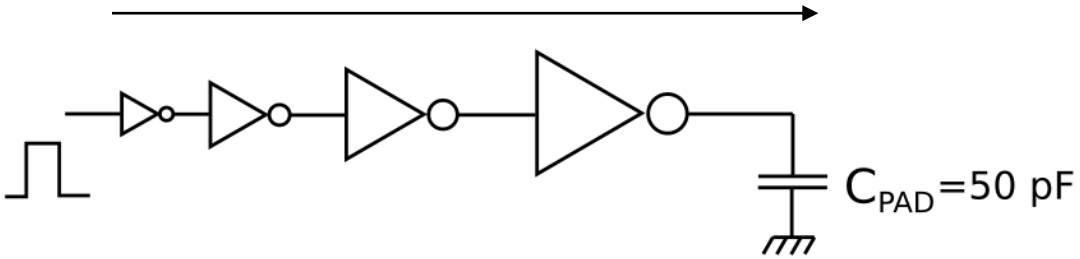
C_{PAD}=50 pF $\quad t_p = 0.7 \cdot 5k \cdot 50pF = \mathbf{172\ ns\ !!}$ ⟶ Huge delay

→ previously we had a period around 200 ps → if we connect the ring oscillator to the PAD we will not see any signal out of the chip.

3. Buffers

- We add a string of inverters to feed the load → a buffer.

To keep the same delay for all of them, we need to increase the size of the inverters



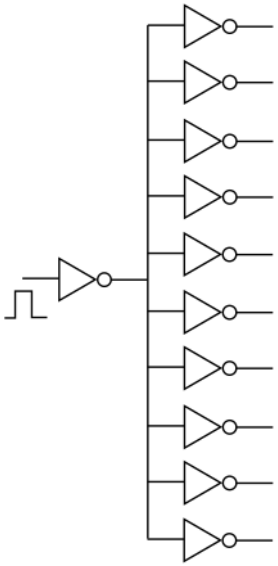
How much do we need to increase the size for each inverter and how many taps are required?

Optimal solution:

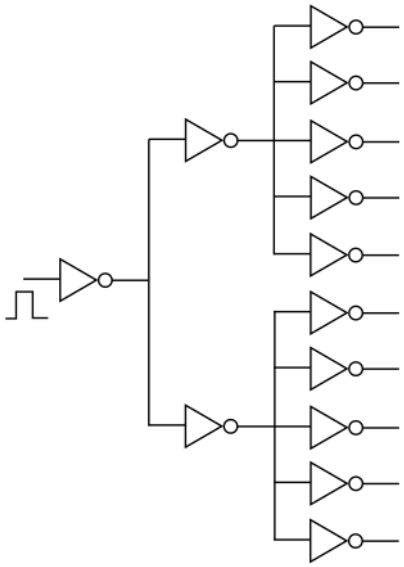
$$A = \left(\frac{C_{PAD}}{C_{in1}}\right)^{1/N} \qquad N = \ln\frac{C_{PAD}}{C_{in1}}$$

4. Distributed drivers

- When we want to distribute a digital signal over different places we use a tree-based distribution.
- Very common for the clock distribution.



(a)



(b)

- If we assume that all the inverters are sized similar and always feed the same capacitance C_{in}:

(a)

$$t_{p1} = 0.7R_{eq} \cdot 10C_{in}$$
$$t_{p2} = 0.7R_{eq} \cdot 1C_{in}$$
$$t_t = 11 \cdot 0.7R_{eq}C_{in}$$

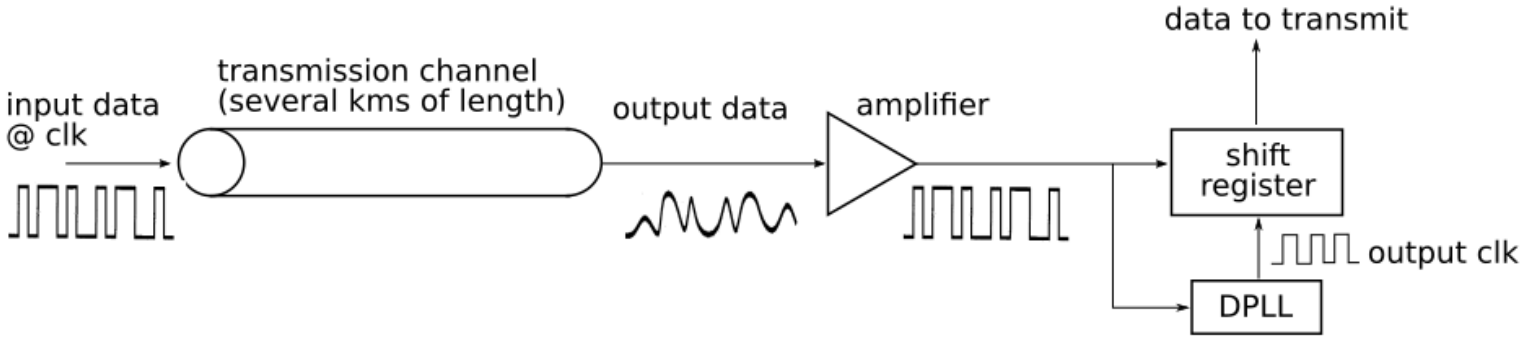
(b)

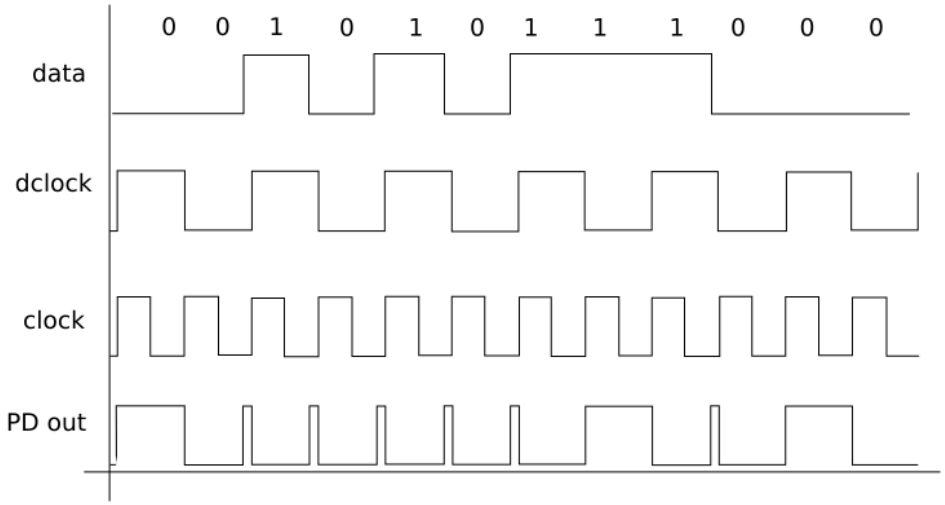
$$t_{p1} = 0.7R_{eq} \cdot 2C_{in}$$
$$t_{p2} = 0.7R_{eq} \cdot 5C_{in}$$
$$t_{p3} = 0.7R_{eq} \cdot 1C_{in}$$
$$t_t = 8 \cdot 0.7R_{eq}C_{in}$$

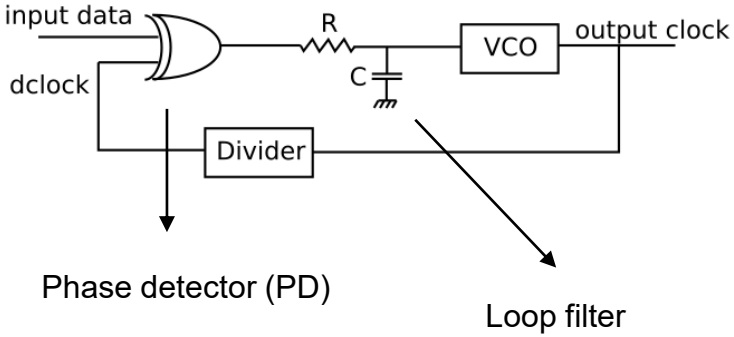
Lower delay for option (b) and sharper output signals.

5. Digital Phase-Locked Loops (DPLLs)

- Clock recovery circuit or bit synchronization circuit.

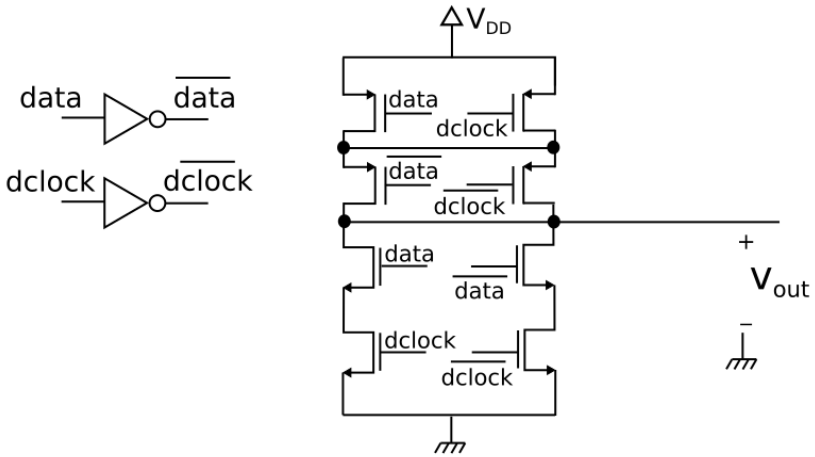




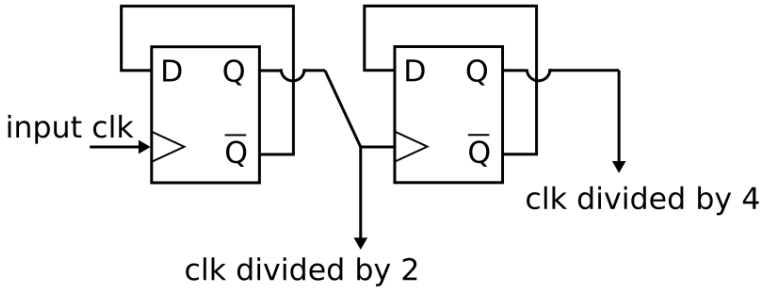


5. Digital Phase-Locked Loops (DPLLs)

Phase detector (PD), differential XOR gate



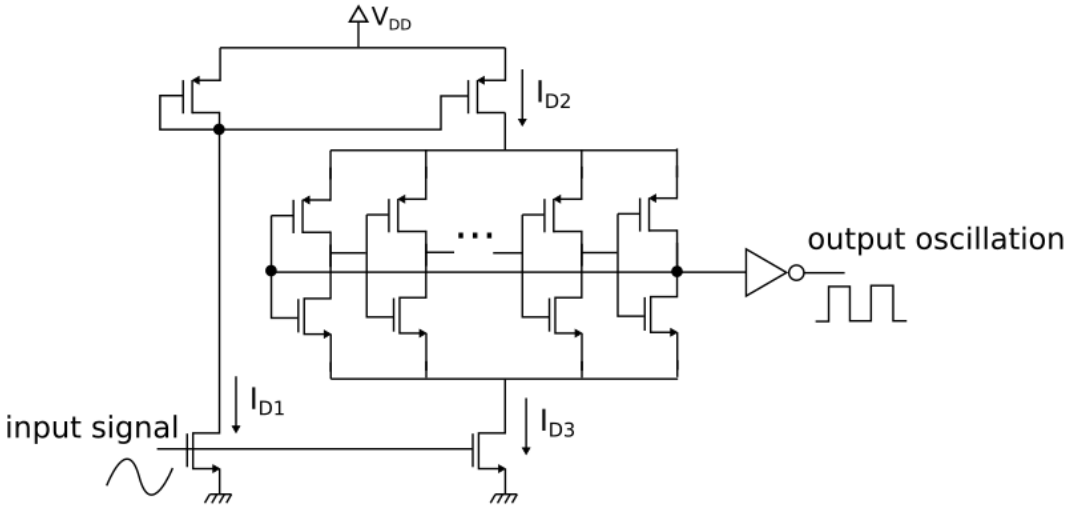
Frequency divider made with flip-flops



Current-starved VCO

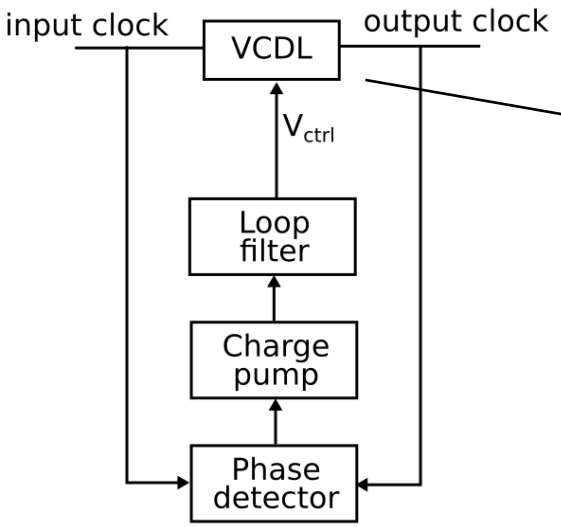
$$f_{osc} = \frac{I_D}{NC_{tot}V_{DD}} \qquad I_D = \frac{I_{D2} + I_{D3}}{2}$$

C_{tot} is the capacitance seen at the output of the inverters

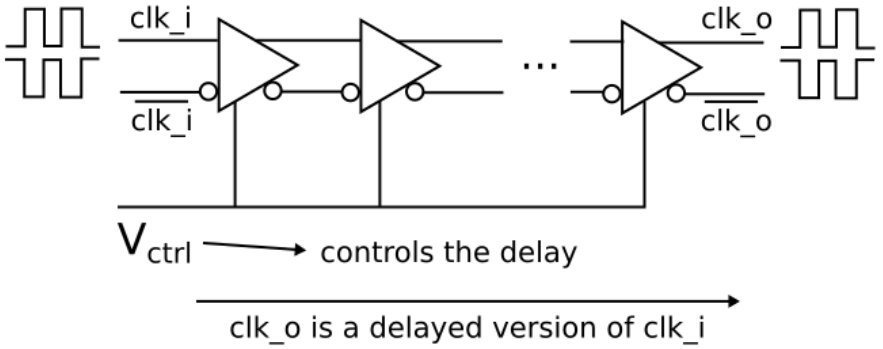


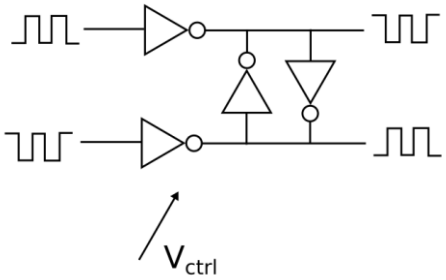
6. Delay Locked Loops (DLLs)

- If we replace the VCO with a controlled-delay digital chain → DLL
- Multiphase clocks applications or clock recovery data applications (CRDs).



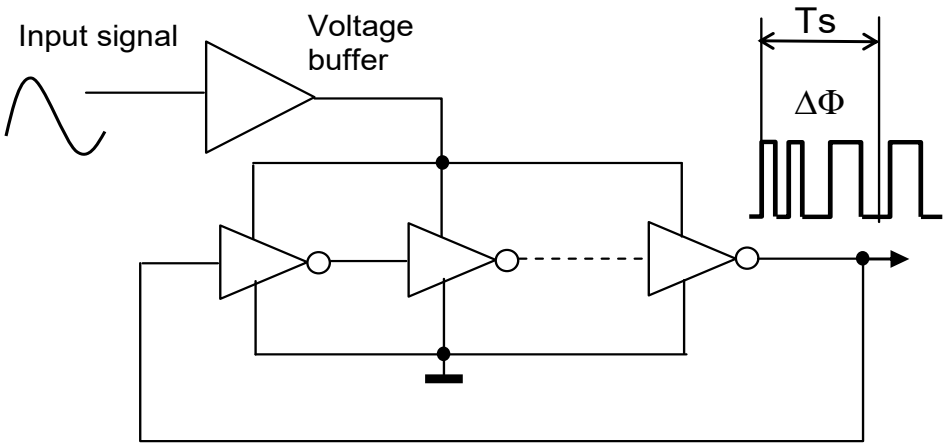
VCDL: Voltage-controlled delay line



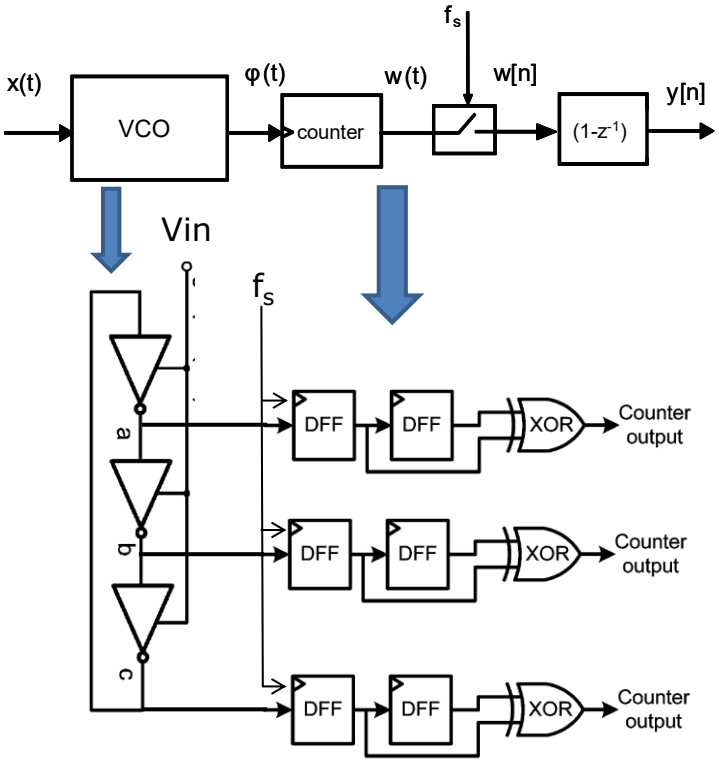


A differential VCDL is often used to minimize noise and power supply variations.

7. Voltage-Controlled-Oscillators (VCO) ADCs



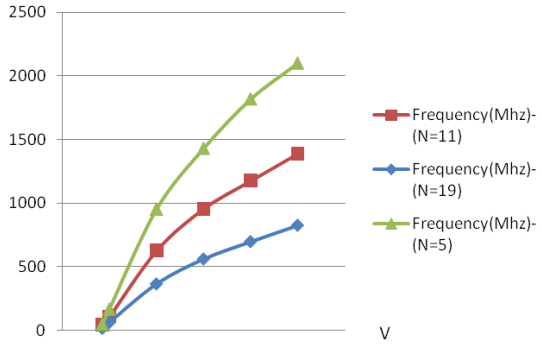
We count the number of pulses in a clock period



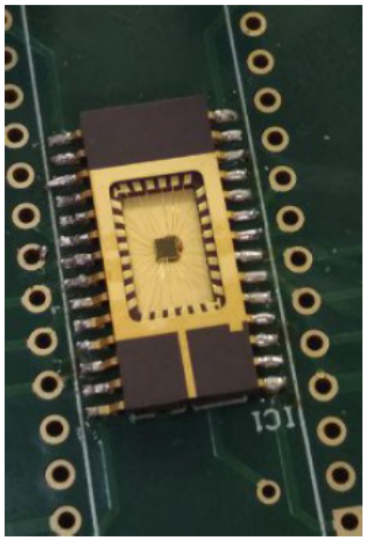
☺ **Time domain quantizer**

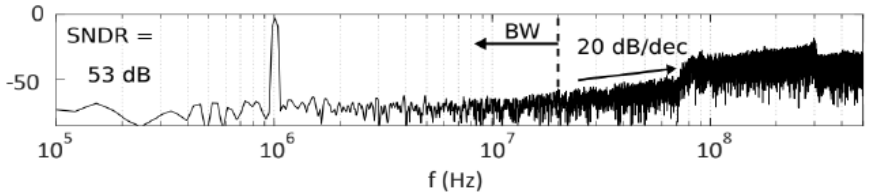
☺ **First order noise shaping**

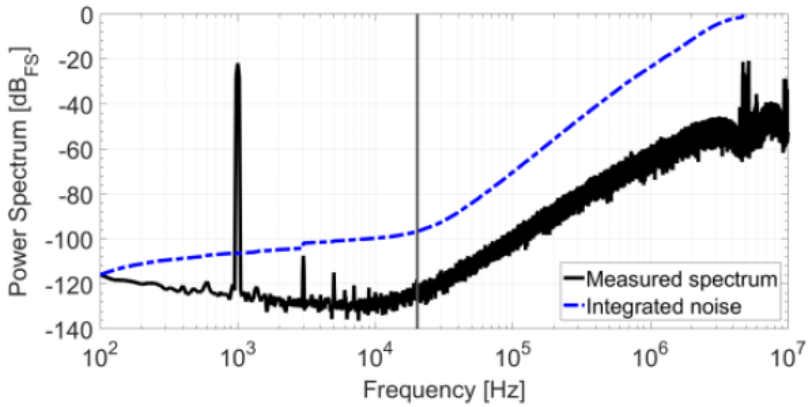
☹ **VCO linearity**



7. Voltage-Controlled-Oscillators (VCO) ADCs





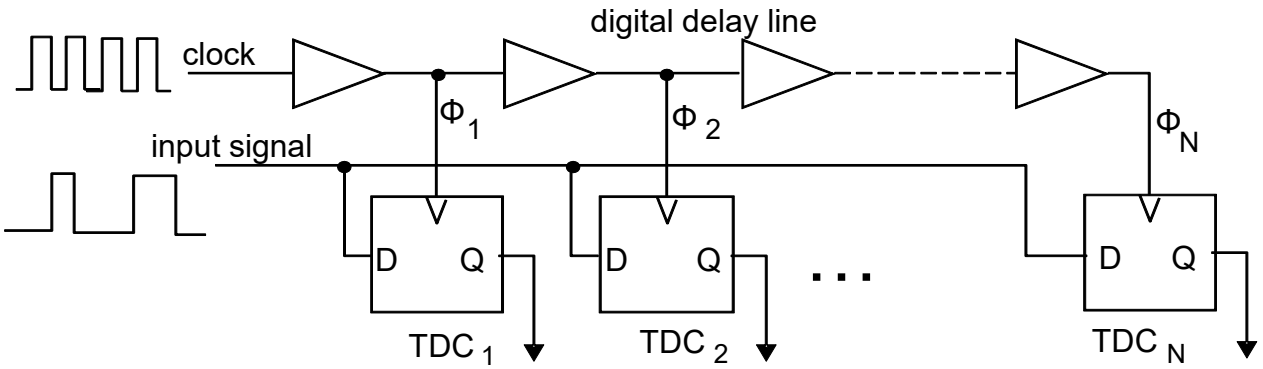


E. Gutierrez et al., "A Pulse Frequency Modulation VCO-ADC in 40 nm," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 1, pp. 51-55, Jan. 2019.

F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer and L. Hernandez, "0.04-mm2 103-dB-A Dynamic Range Second-Order VCO-Based Audio Sigma Delta ADC in 0.13-um CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1731-1742, June 2018.

8. Time-to-Digital Converters

- They measure the time spent between two phenomena with higher resolution



✓ ***Sampling period = Delay of a logic gate < 100ps***

✓***Mismatch in the delays means nonlinearity in the converter***

A DLL is usually required to overcome PVT variations

Bibliography

- R. Jacob Baker. 2010. CMOS Circuit Design, Layout, and Simulation (3rd. ed.). Wiley-IEEE Press.

Simulations are performed through software LTSPice, provided courtesy of Analog Devices and authored by Mike Engelhardt.

Spice models of transistors come from http://cmosedu.com/, website maintained by R. Jacob Baker.