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Unit 8. Robust SoC design and circuit reliability

System-on-Chip and efficient electronic circuit integration techniques

Carlos III University of Madrid, Spain

Electronics Technology Department

Outline

1. PVT variations
2. Voltage and frequency control in digital circuits
3. What is the effect on analog/mixed-signal circuits?

1. PVT variations

- When manufacturing a chip process variations (static) modify the performance of different samples, even in the wafer.
- But not only process variations, voltage supply and temperature can vary (dynamic), and the threshold voltage can vary over time (aging).
- In sub.micron technologies, it is assumed that active devices and resistors can vary ~ 20%, and capacitors ~ 10%, so an **overall 30%** has to be tolerated by the SoC, with minimum performance loss.
- Observation, control, and tuning circuitry is needed… but with an optimized AREA and POWER.
- Prediction of them?

1) Corners simulations
- Best case: fast process, high V_{DD}, low T
- Nominal
- Slow: slow process, low V_{DD}, high T

2) MonteCarlo simulations
- All components are randomly varied
- Statistical analisys

- We can not design for the worst case→ too pessimistic, we need:

Digital:

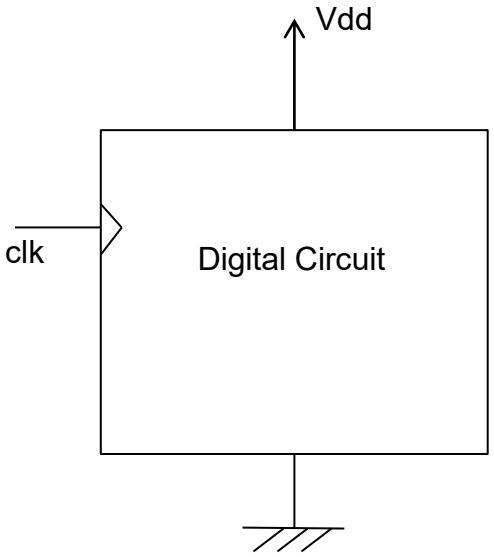
Error detection and correction circuits

Dynamic voltage and frequency scaling

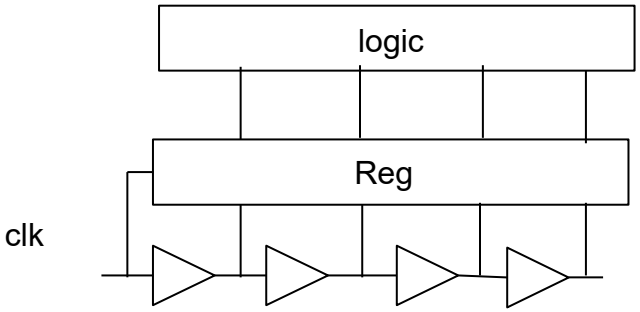
Analog and Mixed-Signal:

Calibration

2. Voltage and frequency control in digital circuits



PVT detection: Clock is measured with a TDC(Time-to-Digital Converter), and used as a hint of the deviation from the nominal circuit.



This is too simple!

We need to regulate Clock (PLL, DDS), and V_{DD} (LDO, DC-DC)

Digital Circuits has a set of “Design rules” to make the circuit “technology independent” and therefore, they are scalable and more robust than analog and mixed-signal circuits. Example: Clock tree distribution design rules.
However, performance can be improved if accurate regulation is done for Vdd and Clock.
In very deep sub-micron technologies, like 28nm, mismatches between masks design (in the lay-out) and implemented circuit are large, and circuit robustness decreases.

Some references: P. Franco, et al. VLSI Test Symp., 1994, M . Nicolaidis, VLSI Test Symp., 1999., D. Ernst, et al., MICRO, 2003.

3. What is the effect on analog/mixed-signal circuits?

We need calibration:

Calibration techniques

- Trimming and/or tuning of currents, voltages, laser trimming, etc.
- Elements selection (resistors, capacitors, current cells), programming coefficients, delays, etc
    - Background calibration: they operate continuously while the circuit is in normal operation
    - Foreground Calibration: they need a calibration phase, at start-up, or periodically (interupting normal circuit operation)

- Based on statistical properties / test based
- Direct deviation observation / Indirect deviation estimation

3. What is the effect on analog/mixed-signal circuits?

Some specific cases: filters and D/A s

Switched Capacitors Filters:

- Mismatch can be reduced by design (large transistors)

Continuous time Filters:

- Time constant tunning/trimming is needed
- background calibration techniques are common

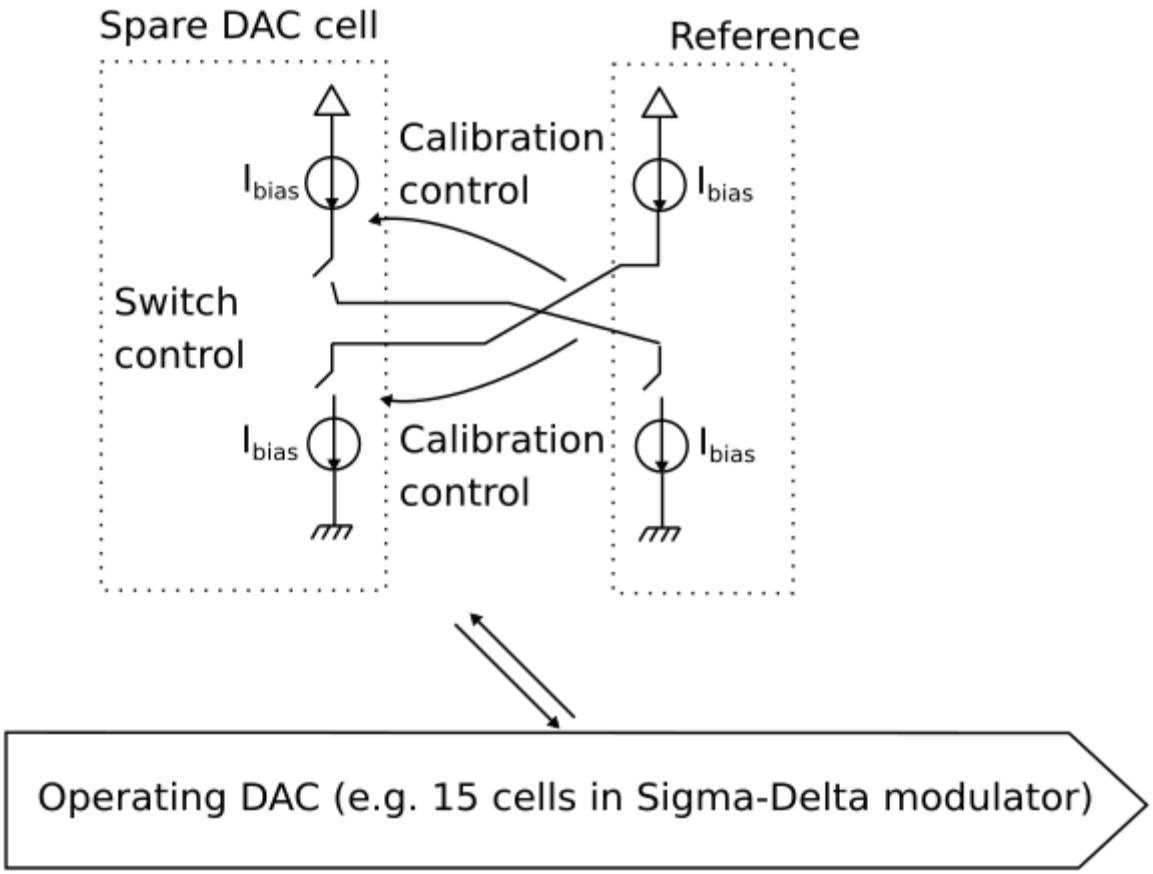
Switched current D/As:

- Mismatch can be reduced by design (large transistors)
- In Sigma Delta ADCs accuracy of D/As has to be much larger than their resolution→ calibration is needed

3. What is the effect on analog/mixed-signal circuits?

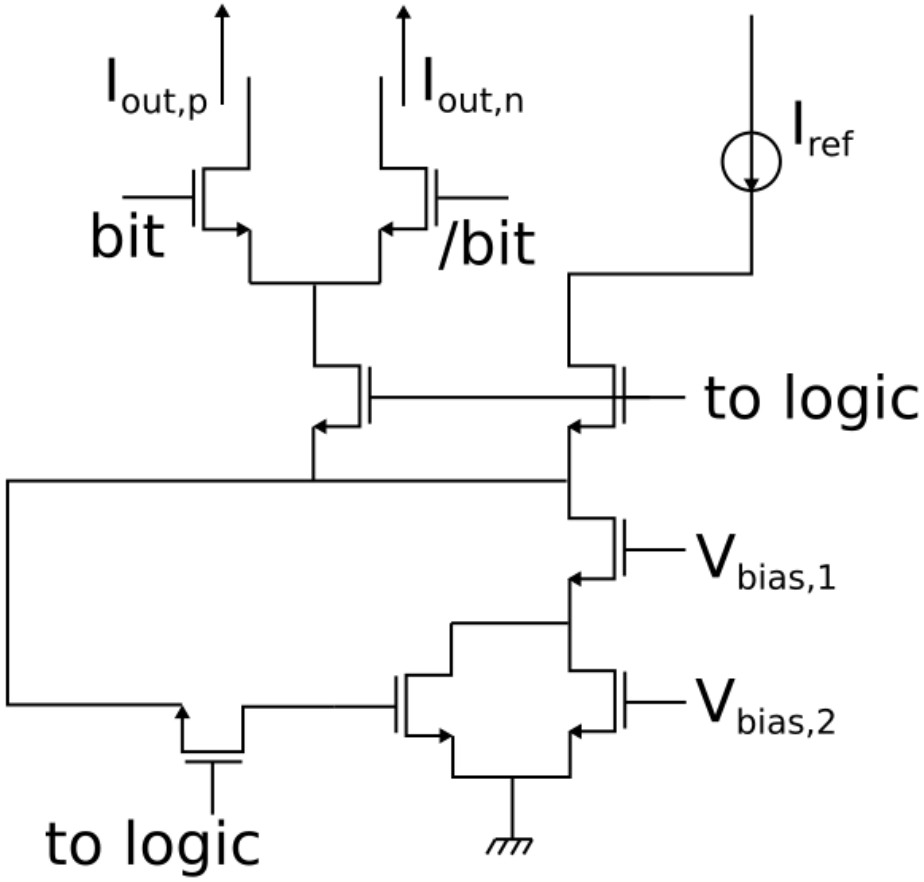
Example of a Switched-current 4-bit D/A (background calib)

- There is a spare cell that replaces another one in the DAC.



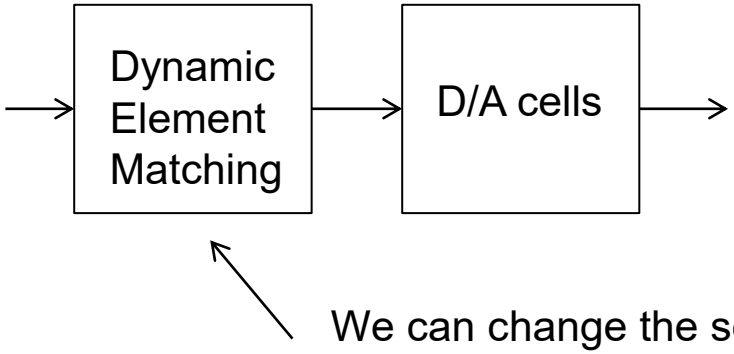
3. What is the effect on analog/mixed-signal circuits?

Self-calibration circuit:



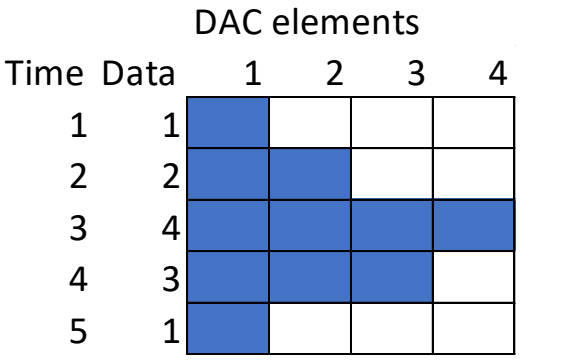
3. What is the effect on analog/mixed-signal circuits?

Dynamic Element Matching:

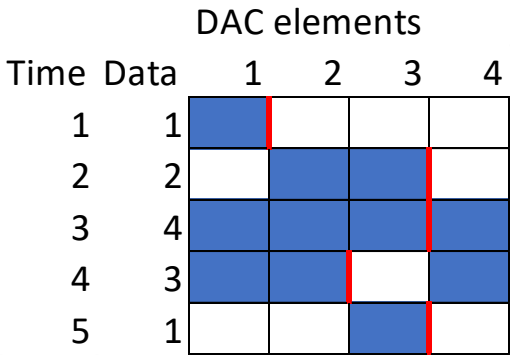


We can change the selection of the cells, to average the error in the time domain

The target is that every cell is used with the same probability



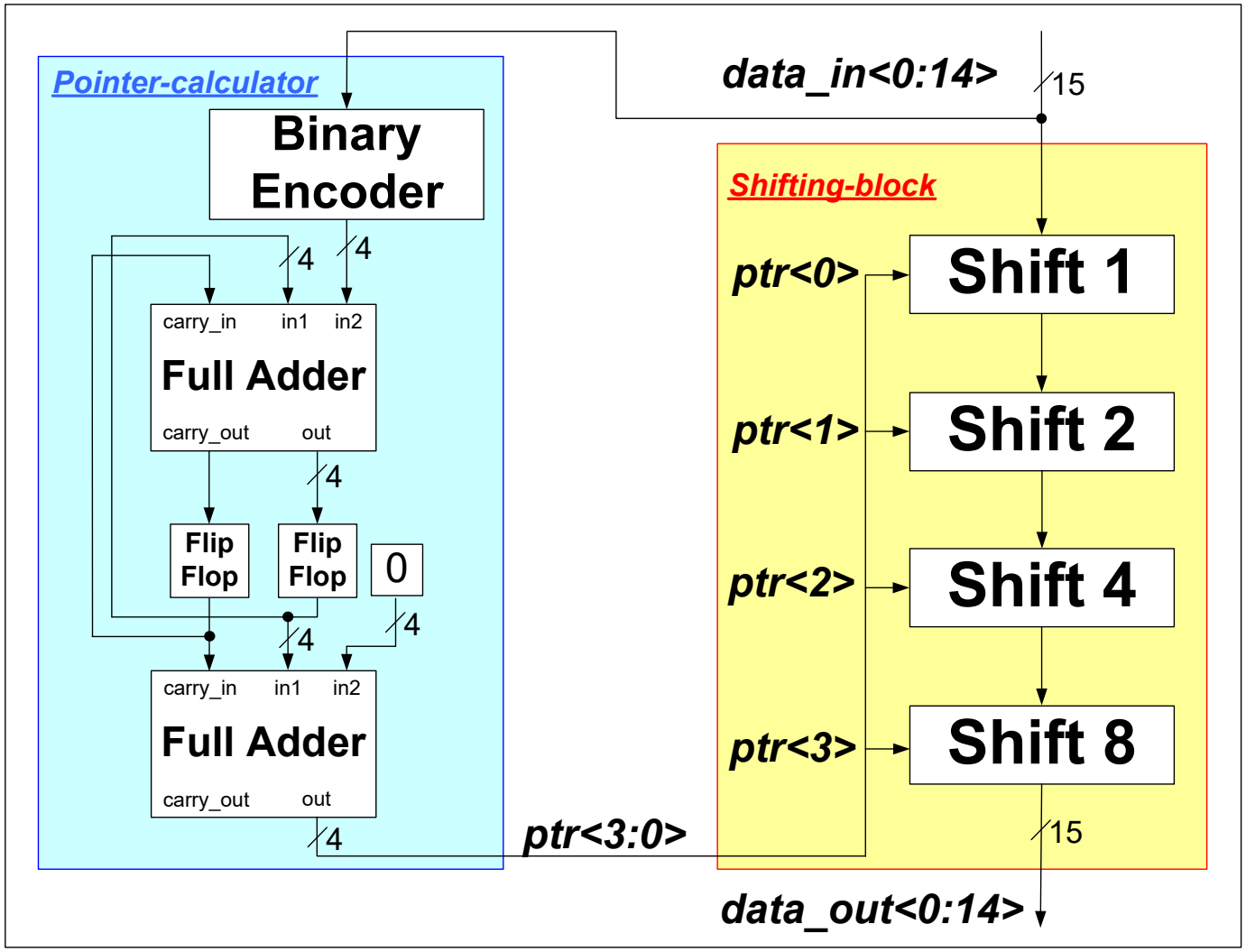
Selection with thermometer code



Selection with DEM

3. What is the effect on analog/mixed-signal circuits?

Dynamic Element Matching: implementation example, the barrel shifter

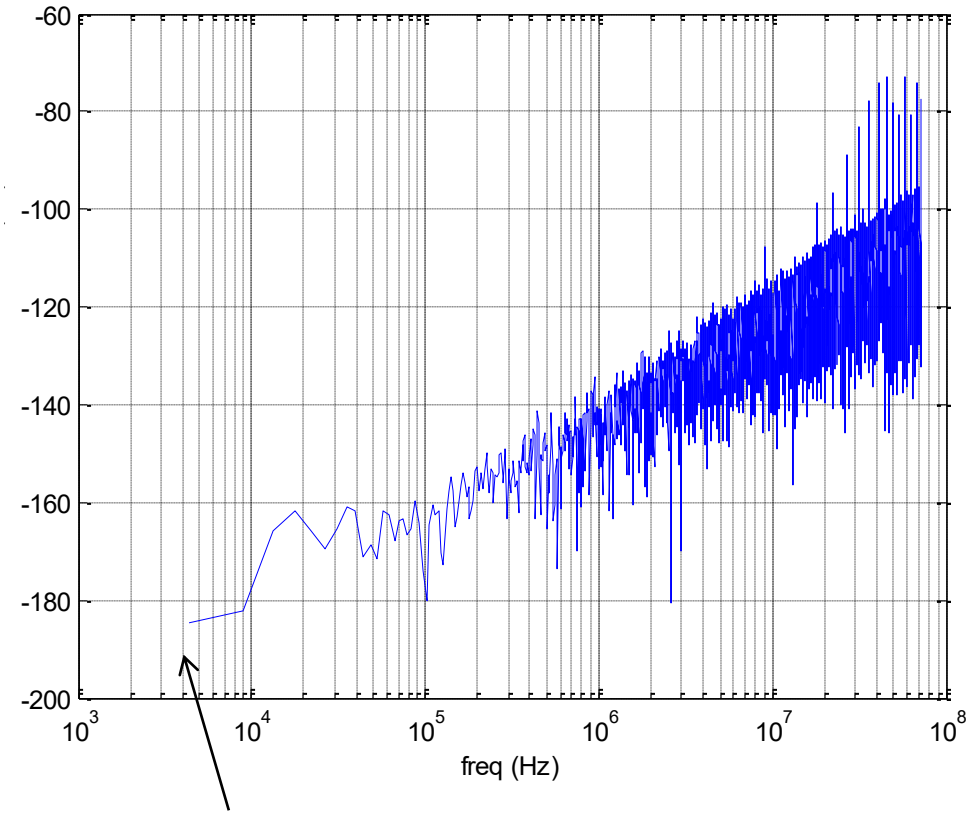


We have a pointer to indicate the last used cell

3. What is the effect on analog/mixed-signal circuits?

Dynamic Element Matching: simulation of mismatch error shaping

DAC error



It is zero in average

Bibliography

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- R. Jevtić et al., "Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 4, pp. 723-730, April 2015.
- Analog Circuit Design: Smart Data Converters, Filters on Chip, Multimode Transmitters, Ed. Arthur van Roermund,Herman Casier,Michiel Steyaert, Springer, 2010