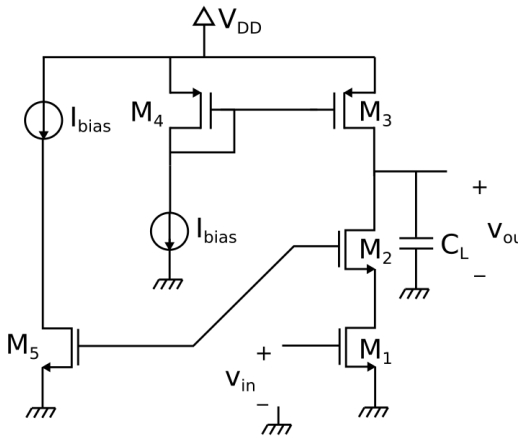
Unit 4,5: EXERCISES

Ex1. Design a single-stage amplifier that accomplishes with the next requirements:

V_{DD}	5 V
P (max)	1 mW
A_V	-50 V/V
V_{out}(max)	4 V
V_{out}(min)	1.5 V
SR	10 V/us
C_L	10 pF

Data: $\mu_n C_{ox}$ = 120 µA/V², $\mu_p C_{ox}$ = 40 µA/V², $\lambda_p = \lambda_n$=0.04 V^{-1}, $|V_{thp}| = |V_{thn}|$=0.7 V, λ_n=0.04 V^{-1}, L_{min} = 1 µm

Let's try a single-ended cascode configuration like:



1) Estimation of I_D due to SR:

$$SR = \frac{I_D}{C_L} \rightarrow I_{D,min} = 100\ \mu A$$

2) Omitting power consumption of M4 and M5 → Estimation of $I_{D,max}$ for power requirement:

$$P = V_{DD} I_D \rightarrow I_{D,max} = 200\ \mu A$$

$$100\ \mu A \leq I_D \leq 200\ \mu A$$

3) Selection of I_D: intermediate value → $I_D = I_{bias} = 150\ \mu A$
4) $V_{out,max}$ requirement:

$$V_{out,max} = V_{DD} - V_{SD3,sat} = V_{DD} - \sqrt{\frac{2I_D}{\mu_p C_{ox} \left(\frac{W}{L}\right)_3}} \rightarrow V_{SD3,sat} = 1\ V$$

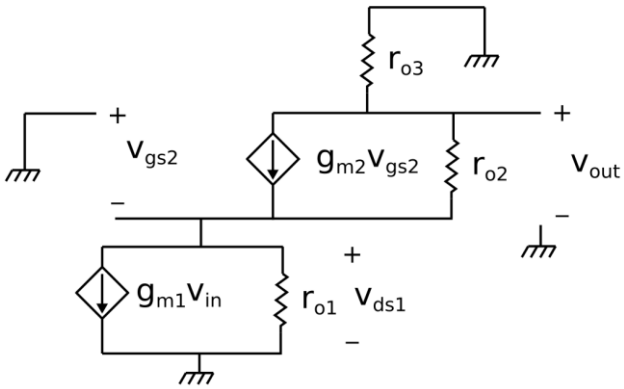
$$I_D = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_3 V_{SD,Sat}^2$$

$$\left(\frac{W}{L}\right)_3 = 7.5 \rightarrow \left(\frac{W}{L}\right)_4 = 7.5$$

5) $V_{out,min}$ requirement:

$$V_{out,min} = V_{DS1,sat} + V_{DS2,sat}$$

From the small signal model, we may assume that:



$A_V = \frac{v_{out}}{v_{in}} \approx -g_{m1}r_{o3}$ → Estimation of $(W/L)_1$

$\left(\frac{W}{L}\right)_1 \approx 2$ → highly dependent of channel modulation effect.

$$V_{DS1,sat} = \sqrt{\frac{I_D}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} = 1.11\ V$$

$$V_{DS2,sat} = 0.4\ V$$

$$\left(\frac{W}{L}\right)_3 = 15.6$$

6) $\left(\frac{W}{L}\right)_5$ estimation:

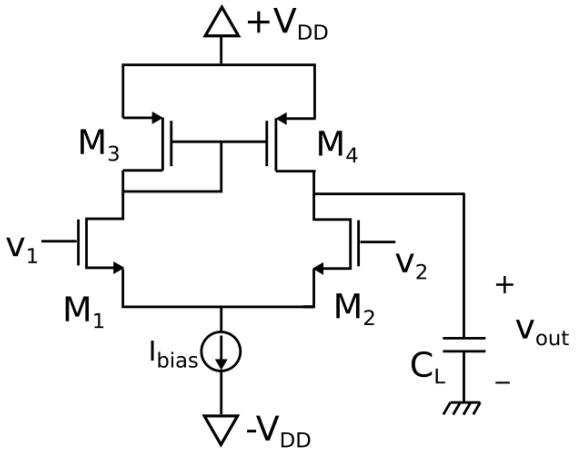
$$V_{DS2,sat} = V_{GS2} - V_{th,n} \rightarrow V_{D2} = V_{G2} - V_{th,n}$$

$$V_{G2} = \sqrt{\frac{I_D}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} + V_{DS1,sat} + V_{th,n} = 2.31\ V$$

$$V_{G2} = V_{G5}$$

$$\left(\frac{W}{L}\right)_5 \approx 1$$

Ex2. Given the following amplifier:



Provide a proper size for the each of the devices such as the following requirements are accomplished:

V_{DD}	2.5 V
P (max)	1 mW
$\|A_V\|$	100 V/V
SR	10 V/us
C_L	5 pF
BW	100 kHz
ICMR	Between -1.5 V and 2 V

Data: $\mu_n C_{ox}$ = 110 µA/V², $\mu_p C_{ox}$ = 50 µA/V², λ_p=0.05 V^{-1}, λ_n=0.04 V^{-1}, $|V_{thp}|=|V_{thn}|$=0.7 V, λ_n=0.04 V^{-1}, L_{min} = 1 µm

1) Estimation of I_D due to SR:

$$SR = \frac{I_D}{C_L} \rightarrow I_{D,min} = 50\ \mu A$$

2) Estimation of $I_{D,max}$ for power requirement:

$$P = 2V_{DD}I_D \rightarrow I_{D,max} = 200\ \mu A$$

3) BW requirement → when SR defines BW → $BW = \frac{1}{2\pi R_{out}C_L} \geq 100\ kHz$

$$R_{out} = r_{o4}||r_{o2} = \frac{1}{(\lambda_p + \lambda_n)I_D} \leq 318\ k\Omega \rightarrow\ I_D \geq 35\ \mu A \rightarrow\ I_{bias} \geq 2I_D = 70\ \mu A$$

$$70\ \mu A \leq I_{bias} \leq 200\ \mu A$$

Design choice: $I_{bias} = 100\ \mu A$

4) ICMR, max requirement:

Two paths to establish the requirement:

$$V_{ICMR,max} = V_{DD} - V_{SG3} - V_{SD,sat1} + V_{GS1} \rightarrow V_{ICMR,max} = V_{DD} - V_{SG3} + V_{THN}$$

$$V_{ICMR,max} = V_{DD} - V_{SD,sat4} + V_{THN}$$

$$V_{SG3} > V_{SD4,sat}$$

$$V_{ICMR,max} = V_{DD} - V_{SG3} + V_{THN} = 2\,V \rightarrow V_{SG3} = 1.2\,V \rightarrow \left(\frac{W}{L}\right)_3 = 8$$

Current mirror → $\left(\frac{W}{L}\right)_4 = 8$

5) ICMR, min requirement:

$$V_{ICMR,min} = V_{GS1} + V_{DS5,sat} - V_{DD}$$

M5 is the device needed to implement a simple current source.

6) Gain requirement:

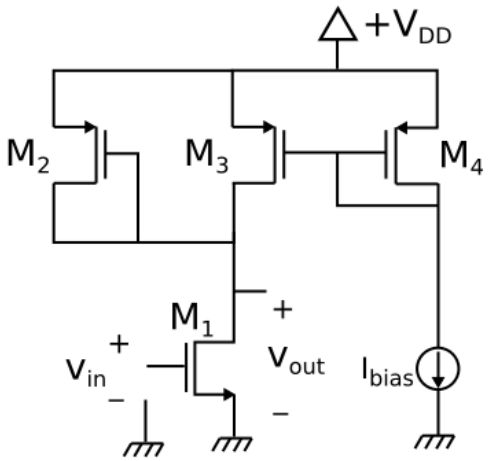
$$|A_V| = \frac{v_{out}}{v_{in}} \approx g_{m1} R_{out}$$

$$R_{out} = 222\ k\Omega$$

$$g_{m1} = \sqrt{\mu_n C_{ox} \left(\frac{W}{L}\right)_1 I_{bias}} = 450\ \mu A/V$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 18.4$$

Ex3. Given the following amplifier:



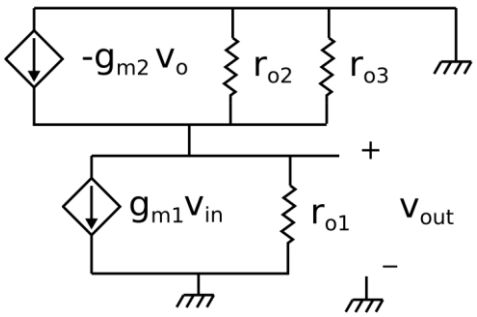
Data: $\mu_n C_{ox}$ = 110 µA/V², $\mu_p C_{ox}$ = 50 µA/V², λ_p=0.05 V⁻¹, λ_n=0.04 V⁻¹, $|V_{thp}|=|V_{thn}|$=0.7 V, λ_n=0.04 V⁻¹, L_{min} = 1 µm, $(W/L)_1$ = 2/1, $(W/L)_2=(W/L)_3=(W/L)_4$=1/1.

Find the value of Vin such that the current in M1 equals 110 uA. Compute the small-signal gain and the output resistance.

1) Estimation of V_{IN} to I_{D1} = 110 uA:

$$V_{IN} = V_{THN} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} = 1.7\ V.$$

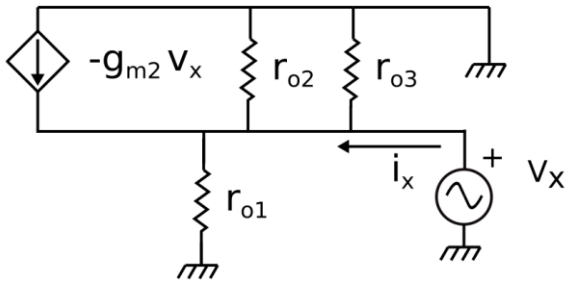
2) Small-signal model:



$$A_V = \frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}}$$

$$g_{m1} = 220\ \mu\frac{A}{V} \quad g_{m2} = 31.6\ \mu\frac{A}{V} \rightarrow\ A_V = -7\ V/V$$

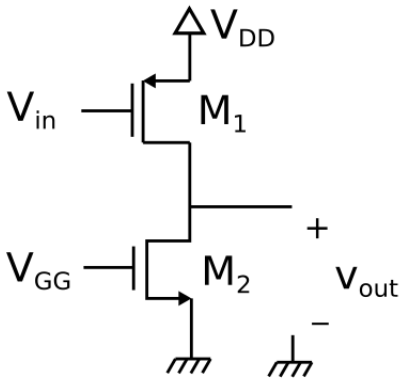
3) For output resistance:



$$R_{out} = \frac{v_x}{i_x} \approx \frac{1}{g_{m2}} = 31.6\ k\Omega$$

Similar to common-source configuration.

Ex4. Given the following amplifier:



Data: $\mu_n C_{ox}$ = 110 µA/V², $\mu_p C_{ox}$ = 50 µA/V², λ_p=0.05 V⁻¹, λ_n=0.04 V⁻¹, $|V_{thp}|=|V_{thn}|$=0.7 V, L_{min} = 1 µm, $(W/L)_1$ = 5/1, $(W/L)_2$= 1/1.

Answer the following questions:

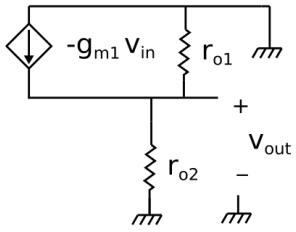
a) **What is the value of V_{GG} to make ID equal to 100 µA?**

$$V_{GG} = V_{THN} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} = 2.61\,V$$

b) **What is the DC value of V_{in}?**

$$V_{in} = V_{DD} - V_{THP} - \sqrt{\frac{2I_D}{\mu_p C_{ox}\left(\frac{W}{L}\right)_1}} = 3.03\,V$$

c) **Small-signal gain?**



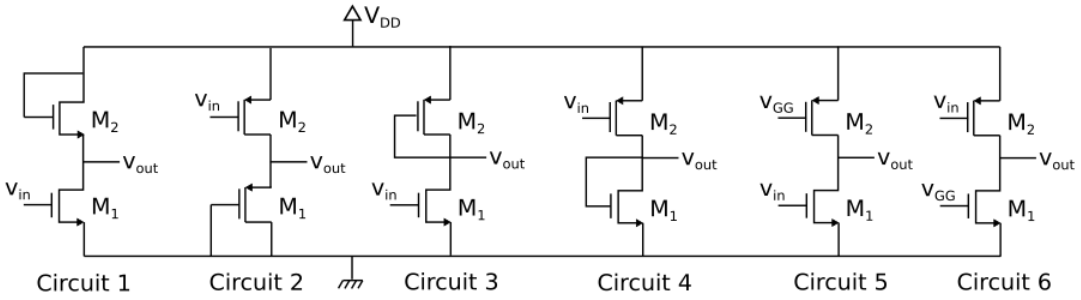
$$A_V = \frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{1/r_{o1} + 1/r_{o2}} = -17.56\,V/V$$

d) **What is the BW if C_{GD1}=C_{GD2}=5 fF, C_{BD1}=C_{BD2}=30fF and C_L=500 fF?**

Mainly due to C_L:

$$\text{BW} = \frac{1/r_{o1} + 1/r_{o2}}{2\pi C_L} = 5.72\,MHz$$

Ex5. Given the following circuits:



Assume that the bias current is the same for all the cases.

Looking at the circuits:

- Circuit 1:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m1}}{g_{m2}+1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{g_{m2}+1/r_{o1}+1/r_{o2}}$
- Circuit 2:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m2}}{g_{m1}+1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{g_{m1}+1/r_{o1}+1/r_{o2}}$
- Circuit 3:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m1}}{g_{m2}+1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{g_{m2}+1/r_{o1}+1/r_{o2}}$
- Circuit 4:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m2}}{g_{m1}+1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{g_{m1}+1/r_{o1}+1/r_{o2}}$
- Circuit 5:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m1}}{1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{1/r_{o1}+1/r_{o2}}$
- Circuit 6:
  $A_V = \frac{v_{out}}{v_{in}} \approx \frac{-g_{m2}}{1/r_{o1}+1/r_{o2}}$ $\quad R_{out} = \frac{v_x}{i_x} \approx \frac{1}{1/r_{o1}+1/r_{o2}}$

For the same configuration, the one implemented with NMOS devices will have higher gain due to the higher mobility of negative charges.

a) In which one we may expect the highest small-signal gain?

Circuit 5.

b) In which one we may expect the lowest small-signal gain?

Circuit 4.

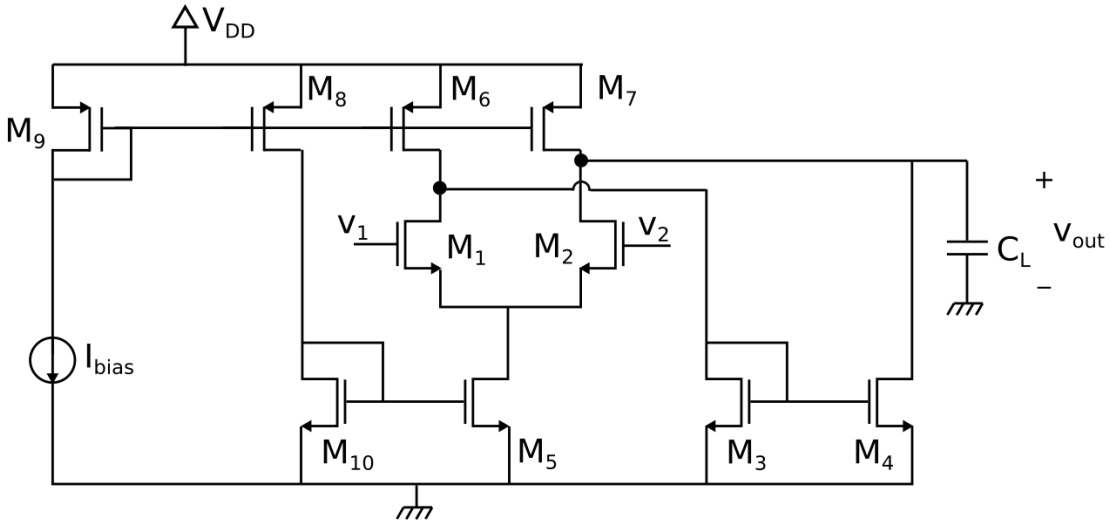
c) In which one we may expect the highest output resistance?

Circuit 5 and circuit 6 (similar value).

d) In which one we may expect the lowest output resistance?

Circuit 1 and circuit 4 (similar value).

Ex6. The following circuit is called folded-current-mirror differential amplifier and is a low-power solution for amplification tasks. Assume that all the devices are of W/L = 100um/1um.



Data: $\mu_n C_{ox}$ = 120 µA/V², $\mu_p C_{ox}$ = 40 µA/V², λ_p=0.05 V^{-1}, λ_n=0.04 V^{-1}, $|V_{thp}|=|V_{thn}|$=0.8 V, V_{DD} = 1.5 V.

a) Compute ICMR.

$$V_{ICMR,max} = V_{DD} - V_{SD6,sat} + V_{THN}$$

$$V_{SD6,sat} = \sqrt{\frac{2I_D}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6}} = 0.71\ V$$

$$V_{ICMR,max} = 1.593\ V$$

$$V_{ICMR,min} = V_{GS1} - V_{SD5,sat}$$

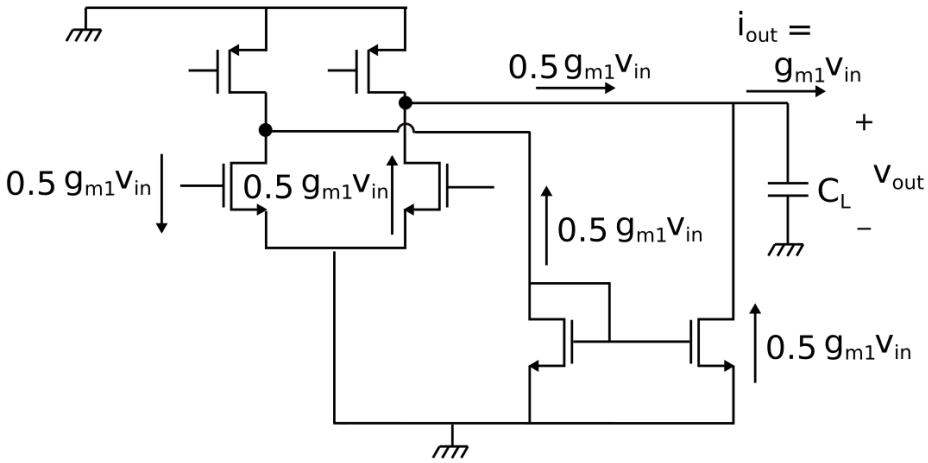
$$V_{SD5,sat} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_5}} = 0.41\ V$$

$$V_{GS1} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{THN} = 1.08\ V$$

$$V_{ICMR,min} = 1.49\ V$$

$$ICMR = 1.593 - 1.49 = 0.103\ V$$

b) Compute the differential small-signal gain.



$$R_{out} \approx \frac{1}{1/r_{o4} + 1/r_{o2} + 1/r_{o7}}$$

Defining $v_{in} = v_1 - v_2$:

$$A_v = \frac{i_{out}R_{out}}{v_{in}} = g_{m1}R_{out} = 37.7\ V/V$$ → very optimist value!

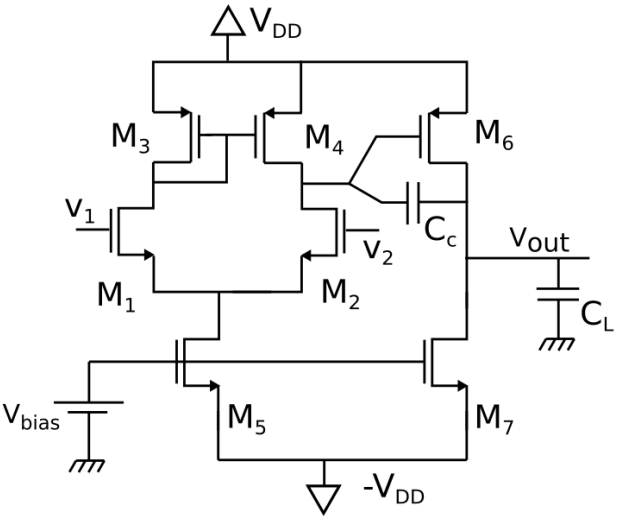
c) If C_L = 10 pF, what is the BW of the circuit considering only C_L?

$$\text{BW} = \frac{1}{2\pi R_{out}C_L} = 144\ kHz$$

Ex7. Design an opamp with Miller compensation:

V_{DD}	2.5 V
P (max)	2 mW
$\|A_V\|$	5000 V/V
SR	10 V/us
C_L	10 pF
GBW	5 MHz
ICMR	Between -1 V and 2 V
Output range	Between -2 V and 2 V
Phase margin	60º

Data: $\mu_n C_{ox}$ = 120 µA/V², $\mu_p C_{ox}$ = 40 µA/V², λ_p=0.02 V^{-1}, λ_n=0.02 V^{-1}, $|V_{thp}|$=0.9 V, $|V_{thn}|$=0.8 V, V_{DD} = 1.5 V, L_{min} = 1 µm.



1) For Mf = 60º → $C_c > 0.22C_L$

$$C_C > 2.2\,pF \rightarrow C_C = 3\,pF$$

2) Two-stage opamps → SR usually limited by the first stage:

$$SR = \frac{I_{D5}}{C_C} \rightarrow I_{D5} = 30\ \mu A$$

3) ICMR,max requirement:

$$V_{ICMR,max} = V_{DD} - V_{SG3} + V_{THN} \rightarrow V_{SG3} = 1.3\,V$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{\mu_p C_{ox}(V_{SG3} - |V_{THP}|)^2} \approx 5$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 5$$

4) GBW requirement:

$$GBW = \frac{g_{m1}}{C_C} \rightarrow g_{m1} = 94.24\ \frac{\mu A}{V}$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 3$$

5) ICMR,min requirement:

$$V_{GS1} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{THN} = 1.08\ V$$

$$V_{DS5,sat} = V_{ICMR,min} - V_{GS1} + V_{DD} = 0.42\ V$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D3}}{\mu_n C_{ox}\left(V_{DS5,sat}\right)^2} = 3$$

6) Gm_6:

$$2.2GBW = \frac{g_{m6}}{C_L} \rightarrow\ g_{m6} = 691\ \frac{\mu A}{V}$$

$$g_{m6} > 10g_{m2} \rightarrow g_{m6} = 942.4\ \frac{\mu A}{V}$$

$$g_{m6} = 942.4\ \frac{\mu A}{V}$$

7) Output voltage requirement:

$$V_{out,max} = V_{DD} - V_{DS6,sat} \rightarrow\ V_{DS6,sat} = 0.5\ V$$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{\mu_p C_{ox} V_{DS6,sat}} = 35$$

$$I_{D6} = 175\ \mu A \rightarrow\ I_{D7} = 175\ \mu A$$

$$V_{GS5} = \sqrt{\frac{2I_{D5}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_5}} + V_{THN} = 1.21\ V \rightarrow\ V_{GS5} = V_{GS7} = 1.21\ V$$

$$\left(\frac{W}{L}\right)_7 = \frac{2I_{D7}}{\mu_n C_{ox}(V_{GS7} - |V_{THN}|)^2} \approx 18$$

$$V_{out,min} = V_{DS7,sat}$$

$$V_{DS7,sat} = 1.21 - 0.8 = 0.4\ V$$

$$V_{out,min} = -2.5 + 0.4 = -2.1\ V < 2\ V$$

$V_{out,min}$ → accomplished

8) Small-signal gain requirement:

$$A_V = \frac{v_{out}}{v_{in}} \approx \frac{-2g_{m1}g_{m6}}{I_{D5}(\lambda_2 + \lambda_4)I_{D7}(\lambda_7 + \lambda_6)} = 21145.66\frac{V}{V} > 5000\frac{V}{V}$$

9) Power consumption requirement:

$$P_{diss} = 2I_{D5}V_{DD} + 2I_{D7}V_{DD} = 1.025\ mW < 2\ mW$$

10) What about other poles and zeros?

Current mirror pole → $f_p \approx \frac{g_{m3}}{2\pi\ 2C_{GS3}} = \frac{-\sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_3 I_{D3}}}{2\pi\ 2^2/_3 W_3 L_3 C_{ox}} = 1.83\ GHz$ → too high.

$$C_{ox} = 2.47\frac{fF}{\mu m^2}, L_3 = 1\ \mu m, W_3 = 5\ \mu m$$

Zero → $f_z \approx \frac{g_{m6}}{2\pi\ C_C} = 50\ MHz > 10.5\ MHz$

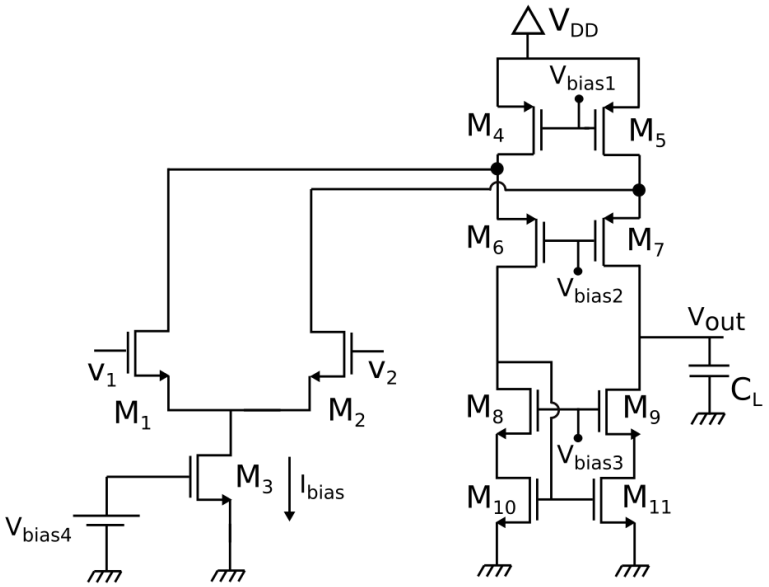
Once we have designed the sizes, we must refine the solution through behavioral simulations →

Device	W/L, before simulation	W/L, after simulation
1	3	10 with L = 2um
2	3	10 with L = 2um
3	5	5 with L = 3um
4	5	5 with L = 3um
5	3	3 with L = 2um
6	35	90
7	18	30 with L = 2um

We can compensate the right-half-plane zero with a resistance:

$$R_Z = \frac{C_C + C_L}{C_C}\frac{1}{g_{m6}} = 4600\ \Omega \rightarrow \text{MF} = 96º$$

Ex8. Design a folded-cascode opamp with the following requirements:



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V_{DD}	2.5 V
P (max)	5 mW
$\|A_V\|$	3000 V/V
SR	10 V/us
C_L	10 pF
GBW	10 MHz
ICMR	Between 1.5 V and 2 V
Output range	Between 0.5 V and 2 V

1) SR requirement:

$$SR = \frac{I_{D3}}{C_L} \rightarrow I_{D3} = 100\ \mu A$$

$I_{D5} = I_{D4}$ → typically, $I_{D5} = I_{D4}$ between 1.25-2 I_{D3}

$$I_{D5} = I_{D4} = 200\ \mu A$$

For the sake of simplicity, we assume M4=M5=M6=M7 and M8=M9=M10=M11:

2) Output voltage requirement:

$$V_{out,max} = V_{DD} - V_{SD5,sat} - V_{SD7,sat} \rightarrow V_{DS5sat} = V_{DS7sat} = 0.25\ V$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{\mu_p C_{ox}\left(V_{SD5,sat}\right|)^2} = 160 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7$$

$$V_{out,min} = V_{DS9,sat} + V_{DS11,sat} \rightarrow V_{DS9sat} = V_{DS11sat} = 0.25\ V$$

$$I_{D9} = I_{D5} - I_{D2}$$

$$\left(\frac{W}{L}\right)_9 = \frac{2I_{D9}}{\mu_n C_{ox}\left(V_{DS9,sat}\right|)^2} = 40 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11}$$

3) GBW requirement:

$$GBW = \frac{g_{m1}}{2\pi C_L} \rightarrow g_{m1} = 628.32\ \frac{\mu A}{V}$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{{g_{m1}}^2}{2\mu_n C_{ox} I_{D1}} = 33$$

4) ICMR requirement:

$$V_{ICMR,min} = V_{GS1} + V_{DS,sat3}$$

$$V_{GS1} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{THN} = 0.96\ V \rightarrow\ V_{DS3,sat} = 0.54\ V$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{D3}}{\mu_n C_{ox}\left(V_{DS3,sat}\right|)^2} = 6$$

$$V_{ICMR,max} = V_{DD} - V_{SD,sat4} + V_{THN} \rightarrow V_{SD,sat4} = 1.3\ V$$

$$\left(\frac{W}{L}\right)_4 = \frac{2I_{D4}}{\mu_p C_{ox}\left(V_{SD4,sat}\right|)^2} = 6 \ll 160 \rightarrow \left(\frac{W}{L}\right)_4 = 160$$

5) Gain requirement: maximum gain achievable:

$$A_V = \frac{v_{out}}{v_{in}} \approx g_{m1} R_{out}$$

$$R_{out} = [g_{m7} r_{o7} (r_{o5} || r_{o2})] || [g_{m9} r_{o9} r_{o11}]$$

$$A_V = 100000\frac{V}{V} \gg 3000\frac{V}{V}$$

6) Power consumption requirement:

$$P_{diss} = 1.25\ mW < 2\ mW$$

7) V_{bias}?

$$V_{bias1} = V_{DD} - V_{SG4} = 1.35\ V$$

$$V_{bias2} = V_{DD} - V_{SD4,sat} - V_{SG6} = 1.14\ V$$

$$V_{bias3} = V_{GS8} - V_{DS10,sat} = 1.03\ V$$

$$V_{bias4} = \sqrt{\frac{2I_{D3}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} + V_{THN} = 1.33\ V$$

Exercises 3, 4, 5, and 6 adapted from Allen, P. E., & Holberg, D. R. (2011). CMOS analog circuit design. New York: Oxford University Press, USA.