SIMULATION SESSION 1: AMPLIFIERS

SYSTEM-ON-CHIP AND EFFICIENT ELECTRONIC CIRCUIT INTEGRATION TECHNIQUES

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

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INTRODUCTION

In this session we will learn the design process of a Miller opamp. A Miller opamp is a two stage opamp whose frequency response can be approximated by:

$$\frac{A_v\left(\frac{s}{z_1}-1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

where

$$z_1 = \frac{gm_2}{C_C}$$
$$p_1 = \frac{GBW}{A_v}$$
$$p_2 = \frac{gm_2}{C_2}$$
$$GBW = \frac{gm_1}{C_c}$$

gm_1 is the transconductance of the first amplifier (part of diff pair)
gm_2 is the transconductance of the second amplifier.
C_C is the compensation capacitor?
C_2 is the load of the Miller amplifier?

One typical rule of thumb to compute the compensation is to start from a certain transconductance ratio, as $gm_2/gm_1 = 10$. This will push the RHP zero to high frequencies (avoiding lead compesation) and will ensure a small compensation capacitor. If we use that ratio, we can use Matlab to predict typical phase margins (PM):

$z_1 = 10GBW$ $gm_2 = 10gm_1$	
PM=45º	$p_2 = 1.2GBW$
PM=60º	$p_2 = 2.2GBW$

The design process will consist in the following steps:

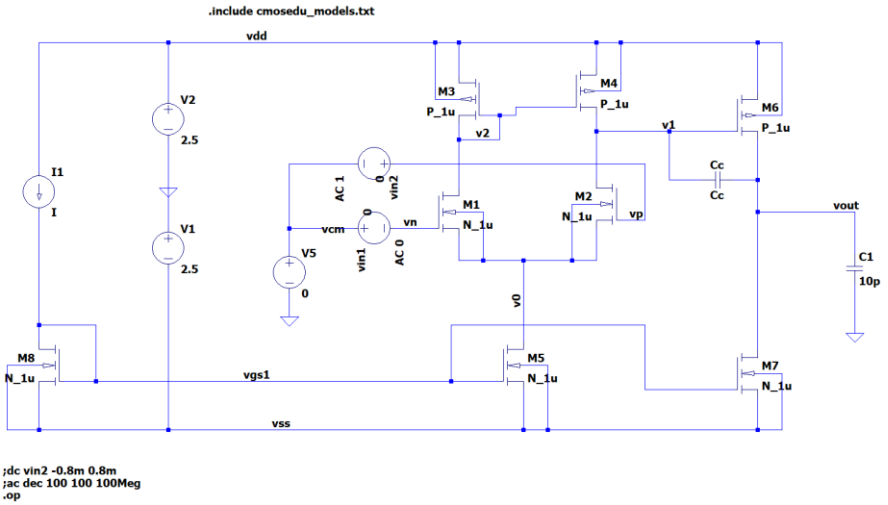
- Compute compensation
- Use specs to compute bias and sizes.
- Simulate the circuit and refine sizes.

1. Opamp Specs

Design a Miller opamp for capacitive (or large resistive) loads with the following specifications:

- DC gain>5000 V/V
- Gain-Bandwidth product > 5MHz, Phase Margin > 60º
- Slew Rate > 10V/µs
- Output swing ±2V, Supply ±2.5V, Input Common Mode Range (ICMR) -1V to 2V.
- Power consumption < 2mW

Use the following schematic and 1µm technology (available in cmosedu_models.txt)



KP = 40 µA/V, λ_P = 0.02V^{-1}, V_{thp} = - 0.9 V

KN = 120 µA/V, λ_n = 0.02V^{-1}, V_{thn} = 0.8 V

Useful equations in saturation:

$$I_D = \frac{KN}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 = \frac{KN}{2}\left(\frac{W}{L}\right)V_{DS_{sat}}^2$$

$$gm = \sqrt{2KN\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{GS} - V_{th}}$$

$$r_{ds} = \frac{1}{\lambda I_D}$$

2. Compensation

Compute C_c assuming $z_1 = 10GBW$

3. Reference current

Compute the reference for M1, assuming the amplifier is slewing when maximum current is integrated in C_c.

4. Bias and Sizes

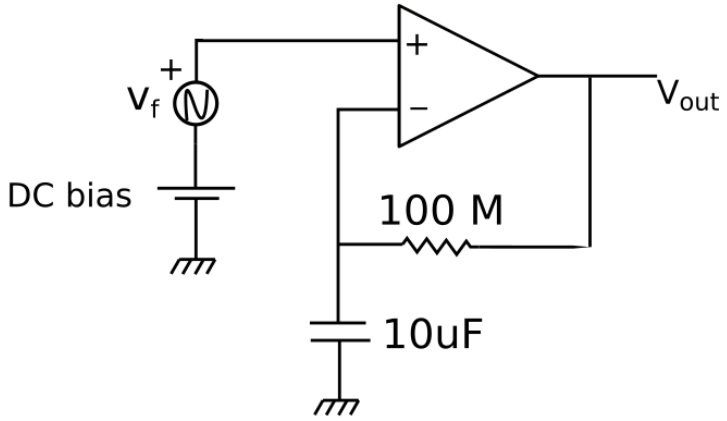
Compute the size of M3, assuming maximum input common mode
Compute gm1
Compute the size of M5, assuming minimum input common mode
Compute gm6 for the maximum output swing
Compute the size of M6 and M7

5. Simulate the amplifier

Simulate the Bias, check all the transistors in .log

6. Check all the specs, and prove them by simulation

Bias is simulated with .op command
Offset and DC gain is simulated with a DC sweep
AC response can be simulated using the following feedback and the 10pF load



Transient response can be simulated using voltage follower with the 10pF load