SIMULATION SESSION 1: AMPLIFIERS

SYSTEM-ON-CHIP AND EFFICIENT ELECTRONIC CIRCUIT INTEGRATION TECHNIQUES

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

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INTRODUCTION

In this session we will learn the design process of a Miller opamp. A Miller opamp is a two stage opamp whose frequency response can be approximated by:

$$\frac{A_v\left(\frac{s}{z_1}-1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)}$$

where

$$z_1=\frac{gm_2}{C_C}$$

$$p_1=\frac{GBW}{A_v}$$

$$p_2=\frac{gm_2}{C_2}$$

$$GBW=\frac{gm_1}{C_c}$$

gm_1 is the transconductance of the first amplifier (part of diff pair)
gm_2 is the transconductance of the second amplifier
C_C is the compensation capacitor
C_2 is the load of the Miller amplifier

One typical rule of thumb to compute the compensation is to start from a certain transconductance ratio, as $gm_2/gm_1=10$. This will push the RHP zero to high frequencies (avoiding lead compesation) and will ensure a small compensation capacitor. If we use that ratio, we can use Matlab to predict typical phase margins (PM):

$z_1=10GBW$ $gm_2=10gm_1$	
PM=45º	$p_2=1.2GBW$
PM=60º	$p_2=2.2GBW$

The design process will consist in the following steps:

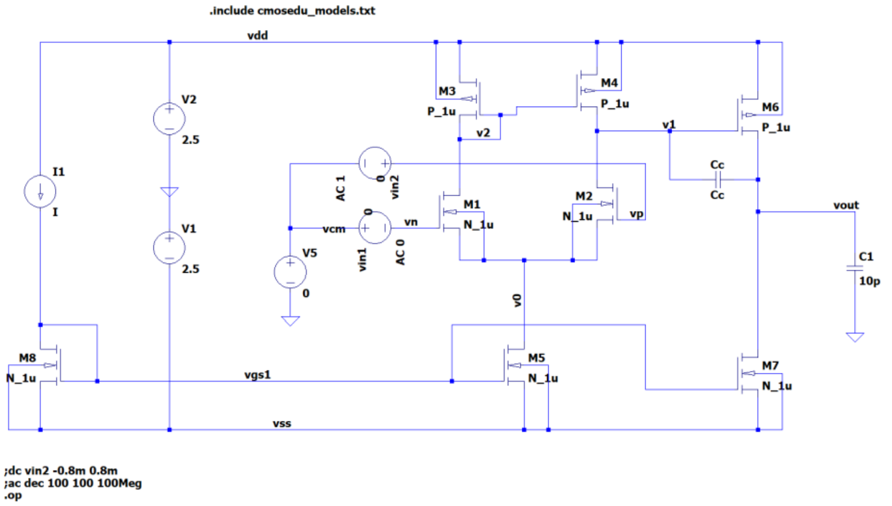
- Compute compensation
- Use specs to compute bias and sizes
- Simulate the circuit and refine sizes

1. Opamp Specs

Design a Miller opamp for capacitive (or large resistive) loads with the following specifications:

- DC gain>5000 V/V
- Gain-Bandwidth product > 5MHz, Phase Margin > 60º
- Slew Rate > 10V/µs
- Output swing ±2V, Supply ±2.5V, Input Common Mode Range(ICMR) -1V to 2V
- Power consumption < 2mW

Use the following schematic and 1µm technology (available in cmosedu_models.txt)



KP = 40 μA/V, λ_P = 0.02V^{-1}, V_{thp} = - 0.9 V

KN = 120 μA/V, λ_n = 0.02V^{-1}, V_{thn} = 0.8 V

Useful equations in saturation:

$$I_D = \frac{KN}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 = \frac{KN}{2}\left(\frac{W}{L}\right)V_{DS}{}_{sat}^2$$

$$gm = \sqrt{2KN\left(\frac{W}{L}\right)I_D} = \frac{2I_D}{V_{GS} - V_{th}}$$

$$r_{ds} = \frac{1}{\lambda I_D}$$

2. Compensation

Compute C_c assuming $z_1 = 10GBW$

$$PM = 60 \rightarrow p_2 > 2.2GBW \rightarrow \frac{10gm_1}{C_2} > \frac{2.2gm_1}{C_c} \rightarrow C_c = 3pF$$

3. Reference current

Compute the reference for M1, assuming the amplifier is slewing when maximum current is integrated in C_c.

$$SR = \frac{I_5}{C_c} \rightarrow I_5 = \frac{10V}{\mu s}3pF = 30\mu A$$

The reference for M1 will be $I_{ref} = I = 30\mu A$

4. Bias and Sizes

Compute the size of M3, assuming maximum input common mode

$$V_{IC}(max) = 2V\ (from\ specs)$$

$$V_{IC}(max) = V_{DD} - V_{SG3} - V_{DS1_{sat}} + V_{GS1} = V_{DD} - V_{SG3} + V_{th1}$$
$$V_{SG3} = 2.5 - 2 + 0.8 = 1.3V$$
$$I_{D3} = \frac{KP}{2}\left(\frac{W}{L}\right)(V_{SG3} - V_{th3})^2 = \frac{I_{ref}}{2} = 15\mu A$$
$$\left(\frac{W}{L}\right)_3 = 4.68 \cong 5 = \left(\frac{W}{L}\right)_4 \rightarrow W = 10\mu m, L = 2\mu m$$

Compute gm1

$$gm_1 = C_c GBW = 3pF(2\pi 5MHz) = 94.2\mu A/V$$

Compute the size of M5, assuming minimum input common mode

$$V_{IC}(min) = V_{DS5_{sat}} + V_{GS1} - V_{SS} = -1V \; from \; specs$$
$$V_{DS5_{sat}} = -1 + 2.5 - V_{GS1}$$
$$g_{m1} = \frac{94.2\mu A}{V} = \sqrt{2KN\left(\frac{W}{L}\right)_1 I_{D1}} \rightarrow \left(\frac{W}{L}\right)_1 = \frac{94.24^2}{2 \cdot 120 \cdot 15} = 2.46 \cong 3$$
$$I_{D1} = \frac{KN}{2}\left(\frac{W}{L}\right)(V_{GS1} - V_{th3})^2 \rightarrow V_{SG1} = 1.08V$$
$$V_{DS5_{sat}} = 0.42V \rightarrow \left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{KN \cdot V_{DS5_{sat}}^2} = 2.88 \cong 3$$
$$W = 6\mu m, L = 2\mu m$$

Compute gm6 for the maximum output swing

On one side $p_2 = gm_6/C_L$ and on the other side $gm_6 = 10gm_1 = 942\mu A/V$
This will imply that p_2 will be greater than 2.2GBW

$$V_{out}(max) = 2V \; from \; specs$$
$$V_{DS6_{ssat}} = V_{DD} - V_{out}(max) = 2.5 - 2 = 0.5V$$

Compute the size of M6 and M7

$$\left(\frac{W}{L}\right)_6 = \frac{gm_6^2}{2KP \cdot I_{D6}} = \frac{g_{m6}^2}{2KP\frac{1}{2}gm_6(V_{GS6} - V_{th})} = \frac{g_{m6}}{KP \cdot V_{DS6_{sat}}} \cong 47$$
$$W = 94\mu m, L = 2\mu m$$
$$I_{D6} = \frac{1}{2}40 \cdot 47 \cdot 0.5^2 = 235\mu A = I_{D7}$$
$$V_{GS7} = V_{GS5} = 1.21 \quad \left(I_{D5} = \frac{KN}{2}\left(\frac{W}{L}\right)_5 (V_{GS5} - V_{th})^2\right)$$
$$\left(\frac{W}{L}\right)_7 = \frac{2I_{D7}}{KN(V_{GS7} - V_{th})^2} = 2 \cdot \frac{235}{120(1.21 - 0.8)^2} = 23.2 \cong 24$$
$$W = 48\mu m, L = 2\mu m$$

5. Simulate the amplifier

Simulate the Bias, check all the transistors in .log

```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
```

Name:	m8	m7	m5	m1	m2
Model:	n_1u	n_1u	n_1u	n_1u	n_1u
Id:	3.00e-05	1.50e-04	3.01e-05	1.50e-05	1.50e-05
Vgs:	1.26e+00	1.26e+00	1.26e+00	1.03e+00	1.03e+00
Vds:	1.26e+00	1.25e-01	1.47e+00	2.24e+00	2.24e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	8.66e-01	8.37e-01	8.66e-01	8.53e-01	8.53e-01
Vdsat:	3.57e-01	3.90e-01	3.57e-01	1.95e-01	1.95e-01
Gm:	1.22e-04	3.51e-04	1.22e-04	1.22e-04	1.22e-04
Gds:	1.64e-06	9.44e-04	1.61e-06	5.08e-07	5.08e-07
Gmb:	3.71e-05	9.84e-05	3.73e-05	3.55e-05	3.55e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.20e-15	9.60e-15	1.20e-15	2.00e-15	2.00e-15
Cgdov:	1.20e-15	9.60e-15	1.20e-15	2.00e-15	2.00e-15
Cgbov:	1.80e-16	1.80e-16	1.80e-16	1.80e-16	1.80e-16
Cgs:	1.24e-14	8.31e-14	1.24e-14	2.07e-14	2.07e-14
Cgd:	0.00e+00	6.42e-14	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

Name:	m6	m3	m4
Model:	p_1u	p_1u	p_1u
Id:	1.50e-04	1.50e-05	1.50e-05
Vgs:	3.58e+00	0.00e+00	8.75e-14
Vds:	4.88e+00	1.29e+00	1.29e+00
Vbs:	4.88e+00	1.29e+00	1.29e+00
Vth:	-9.29e-01	-9.30e-01	-9.30e-01
Vdsat:	-3.43e-01	-3.43e-01	-3.43e-01
Gm:	6.77e-04	6.72e-05	6.72e-05
Gds:	5.35e-06	6.18e-07	6.18e-07
Gmb:	2.09e-04	2.08e-05	2.08e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.88e-14	2.00e-15	2.00e-15
Cgdov:	1.88e-14	2.00e-15	2.00e-15
Cgbov:	1.80e-16	1.80e-16	1.80e-16
Cgs:	0.00e+00	0.00e+00	0.00e+00
Cgd:	1.95e-13	2.07e-14	2.07e-14
Cgb:	0.00e+00	0.00e+00	0.00e+00

M/ is not in saturation, Let's increase W/L of 6.

Using $W = 190\mu m$ and $L = 2\mu m$, we have all transistors in saturation

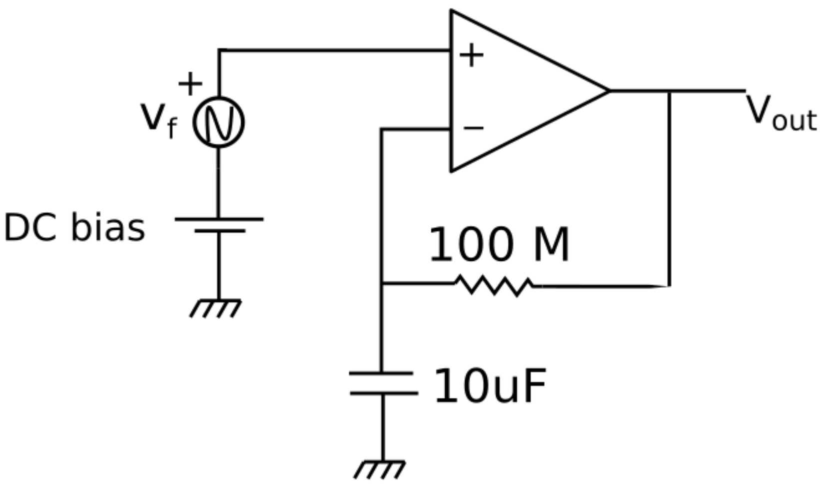
```
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- MOSFET Transistors ---
```

Name:	m8	m7	m5	m1	m2
Model:	n_1u	n_1u	n_1u	n_1u	n_1u
Id:	3.00e-05	2.86e-04	3.01e-05	1.50e-05	1.50e-05
Vgs:	1.26e+00	1.26e+00	1.26e+00	1.03e+00	1.03e+00
Vds:	1.26e+00	3.82e+00	1.47e+00	2.24e+00	2.24e+00
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	8.66e-01	8.37e-01	8.66e-01	8.53e-01	8.53e-01
Vdsat:	3.57e-01	3.90e-01	3.57e-01	1.95e-01	1.95e-01
Gm:	1.22e-04	1.09e-03	1.22e-04	1.22e-04	1.22e-04
Gds:	1.64e-06	1.44e-05	1.61e-06	5.08e-07	5.08e-07
Gmb:	3.71e-05	2.84e-04	3.73e-05	3.55e-05	3.55e-05
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.20e-15	9.60e-15	1.20e-15	2.00e-15	2.00e-15
Cgdov:	1.20e-15	9.60e-15	1.20e-15	2.00e-15	2.00e-15
Cgbov:	1.80e-16	1.80e-16	1.80e-16	1.80e-16	1.80e-16
Cgs:	1.24e-14	9.95e-14	1.24e-14	2.07e-14	2.07e-14
Cgd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgb:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

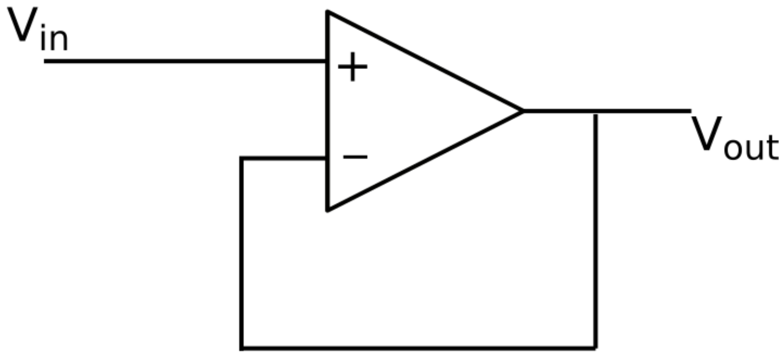
Name:	m6	m3	m4
Model:	p_1u	p_1u	p_1u
Id:	2.86e-04	1.50e-05	1.50e-05
Vgs:	-1.13e-01	0.00e+00	8.77e-14
Vds:	1.18e+00	1.29e+00	1.29e+00
Vbs:	1.18e+00	1.29e+00	1.29e+00
Vth:	-9.29e-01	-9.30e-01	-9.30e-01

6. Check all the specs, and prove them by simulation

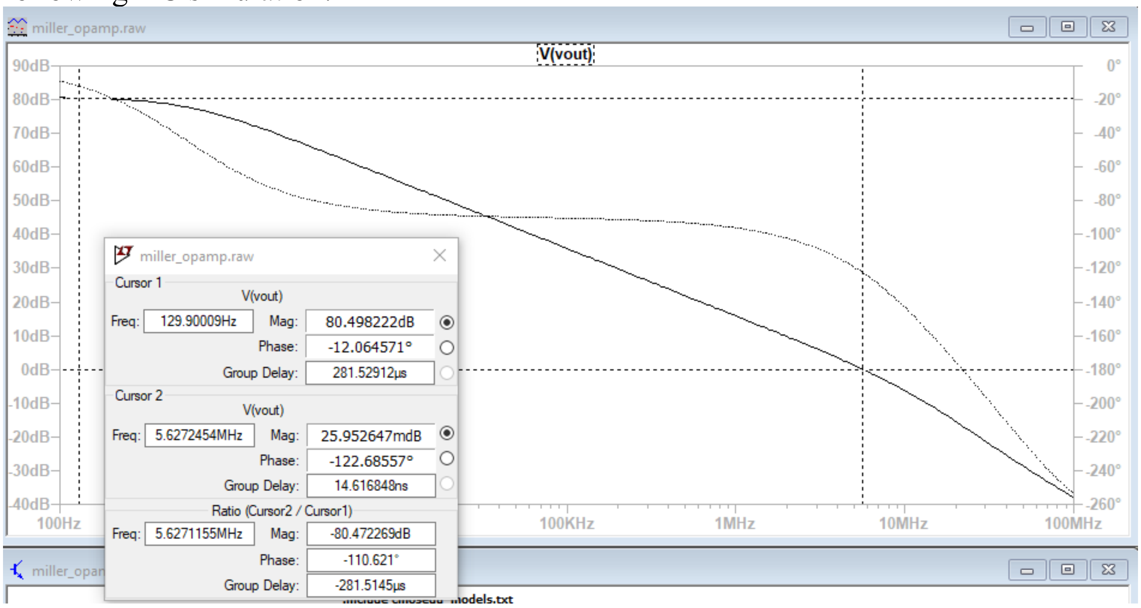
Bias is simulated with .op command
Offset and DC gain is simulated with a DC sweep
AC response can be simulated using the following feedback and the 10pF load



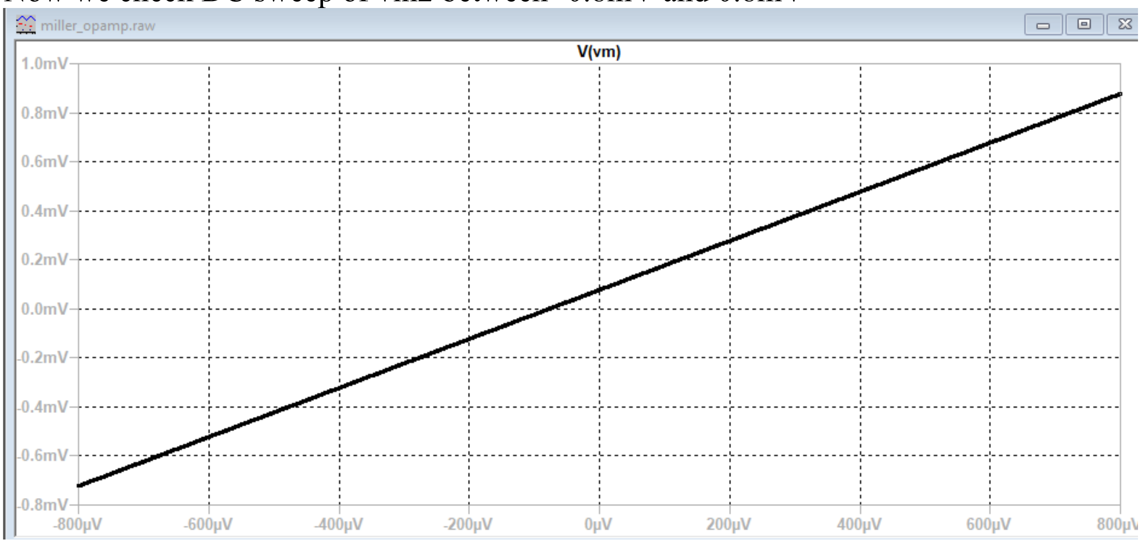
Transient response can be simulated using voltage follower with the 10pF load



The gain is not as high as expected, so following hints on point 7 we end up with the following AC simulation:



Here, we see, that voltage gain, GBW and PM are good enough
Now we check DC sweep of vin2 between -0.8mV and 0.8mV



Offset is below 0.1mV

When vin2=-2 or +2V all transsitor are still in sat region

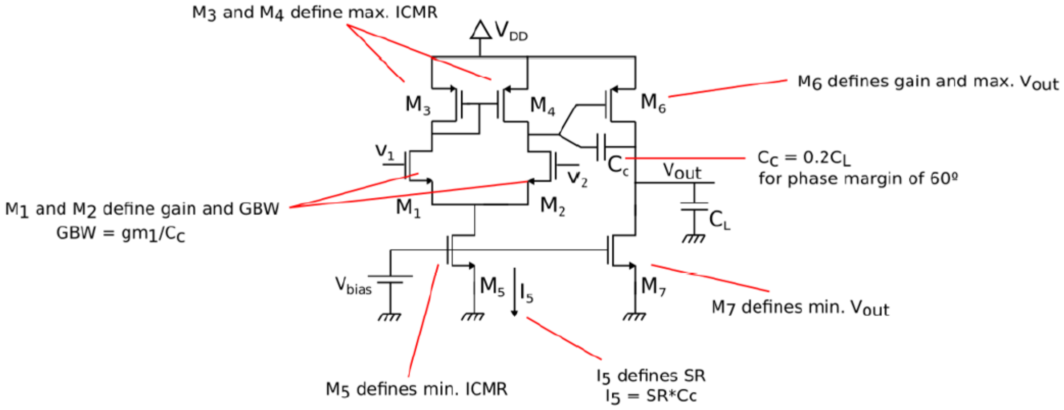
The sizes are as follows:

MOSFET	W(um)	L(um)
M1	10	2
M2	10	2
M3	15	3
M4	15	3
M5	6	2
M6	240	3
M7	36	2
M8	6	2

Power consumption is 1.35mW<2mW under specs

7. Optimizing the amplifier

Here there are some hints to optimize the amplifier:



Some tips:

- Gain defined by gm_1, gm_2, gm_6 and bias currents.
- GBW defined by I_5, gm_1 and gm_2.
- Slew-rate defined by I_5.