Departamento Tecnología Electrónica

UC3M

SIMULATION SESSION 2: DELTA-SIGMA ADC

SYSTEM-ON-CHIP AND EFFICIENT ELECTRONIC CIRCUIT INTEGRATION TECHNIQUES

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INTRODUCTION

In this session we will use the designed amplifier in a practical circuit. The chosen practical circuit is a First-Order Delta-Sigma Modulator ADC (see Fig. 1). It is an oversampled noise-shaped modulator composed of an active integrator, a latched comparator and single bit DAC (see Fig. 2).
It is recommended the reading of "The Delta-Sigma Modulator, Razavi, A circuit for all seasons (SSC Magazine)", available in Aula Global.

1. Simulations

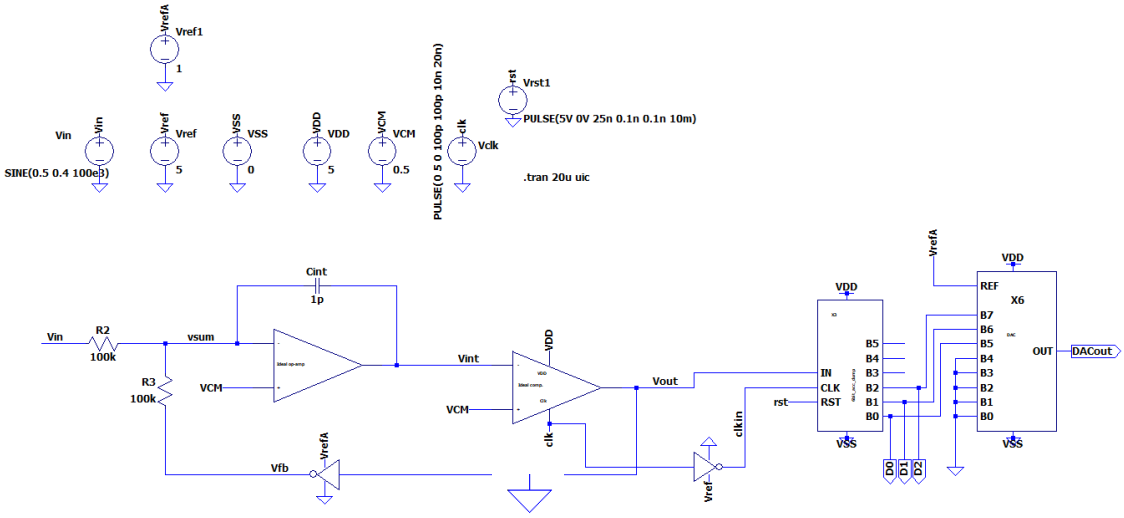
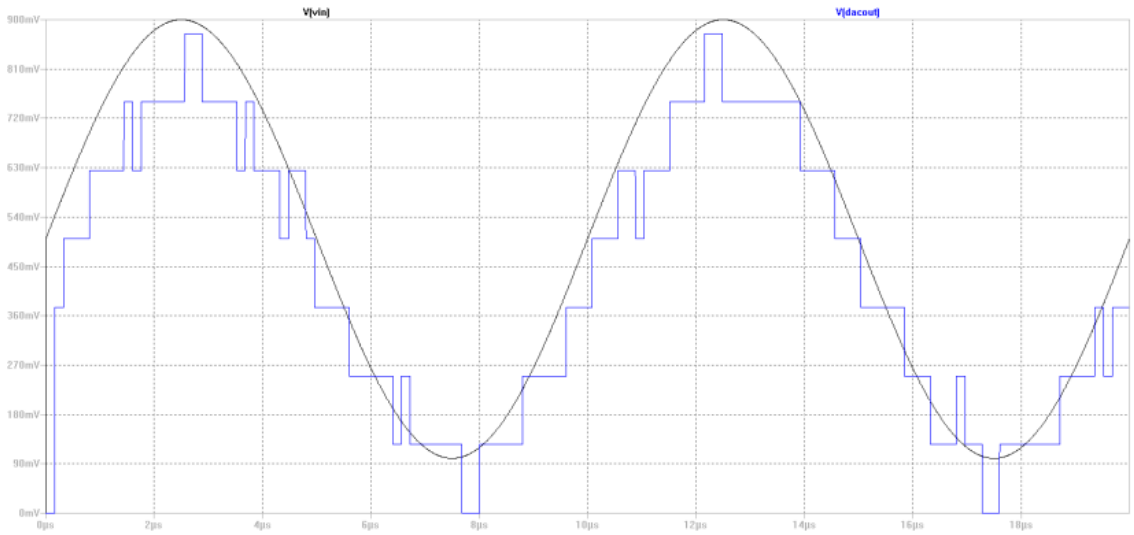


Fig. 3. Circuit to be simulated ("Ideal_DSM.asc")

Vout is the single-bit output of the Oversampled Delta-Sigma Circuit, D[2:0] is the decimated output (Decimation by 8), and DAC_out is a reconstructed analog version of D[2:0].
All the blocks are ideal.

1. Simulate circuit in Fig. 3.

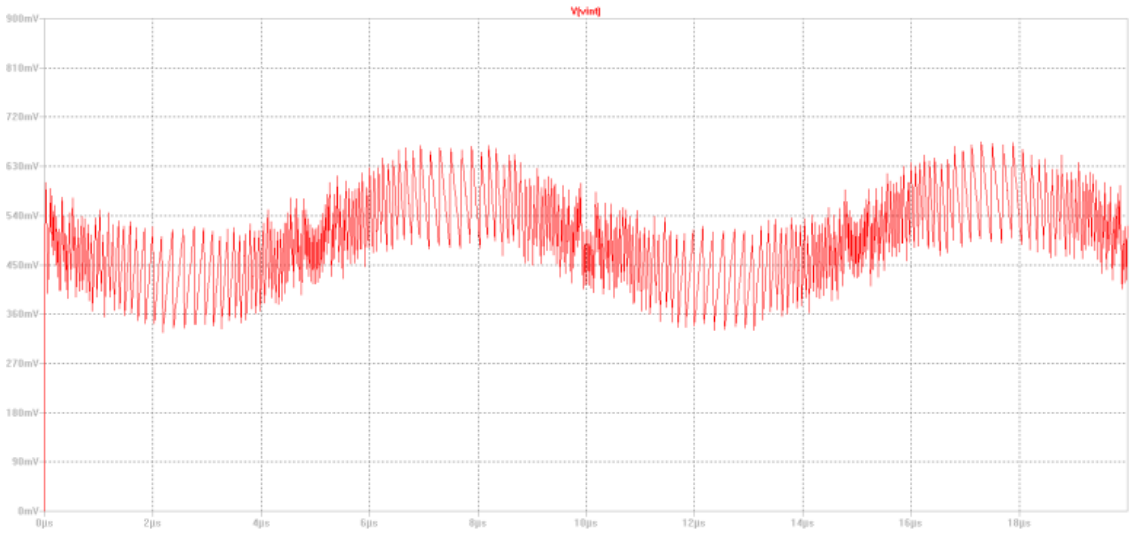
a. Plot Vin and DACout. How many levels and bits are in the digital output?



There are **8 levels.** This means that DACout is a digital output of **3 bits.**

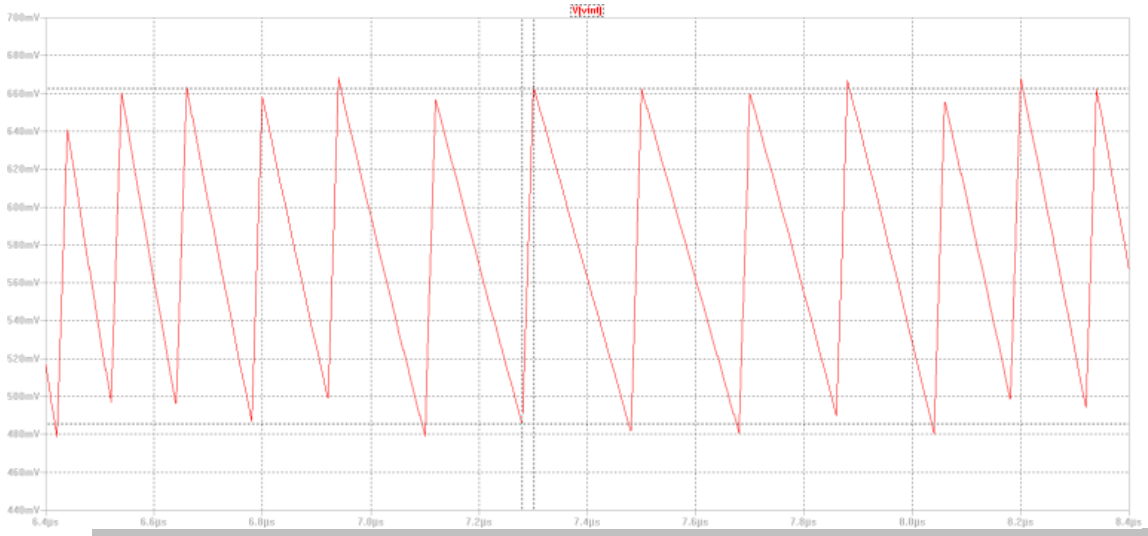
b.

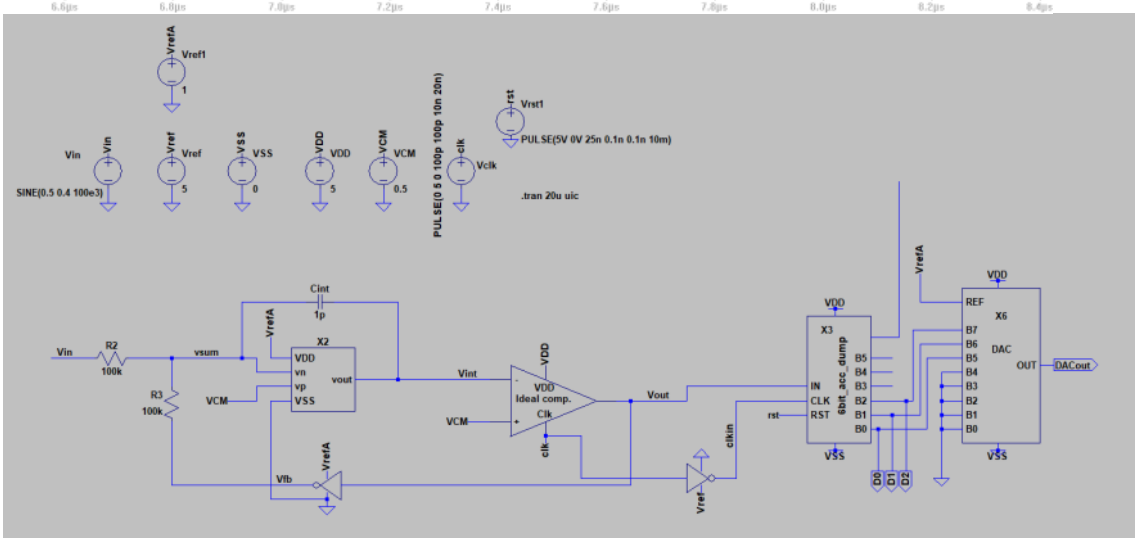
c. Plot Vint. What is the Slew-Rate of signal Vint?



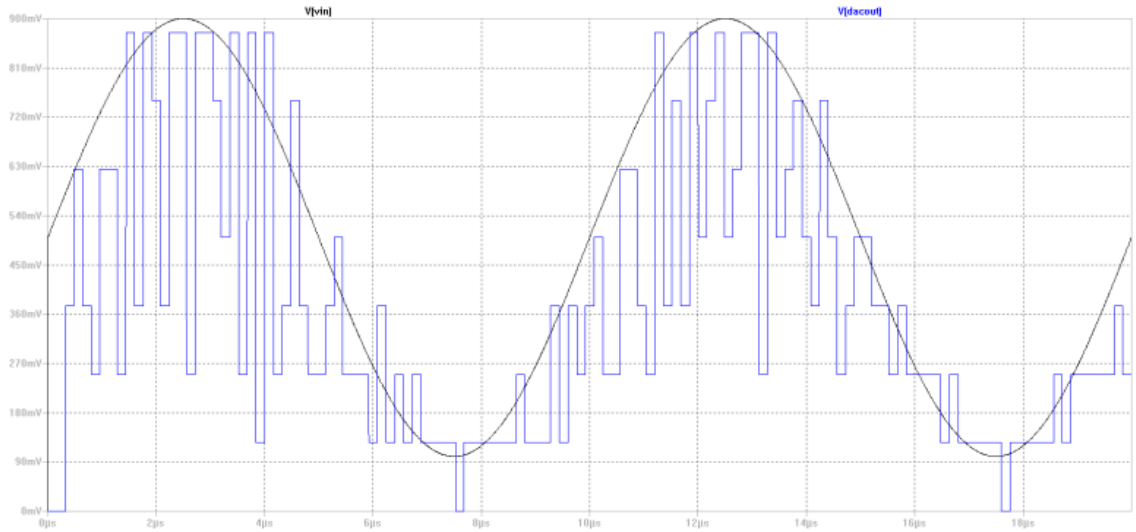
Slew Rate can be computed with the second figure (zoom of the first one), giving around 9V/us

2. Replace the ideal opamp by the Miller opamp “opamp_poor_SR.asc” designed in a similar way as in previous session. Simulate circuit of figure 1 again with the real opamp.



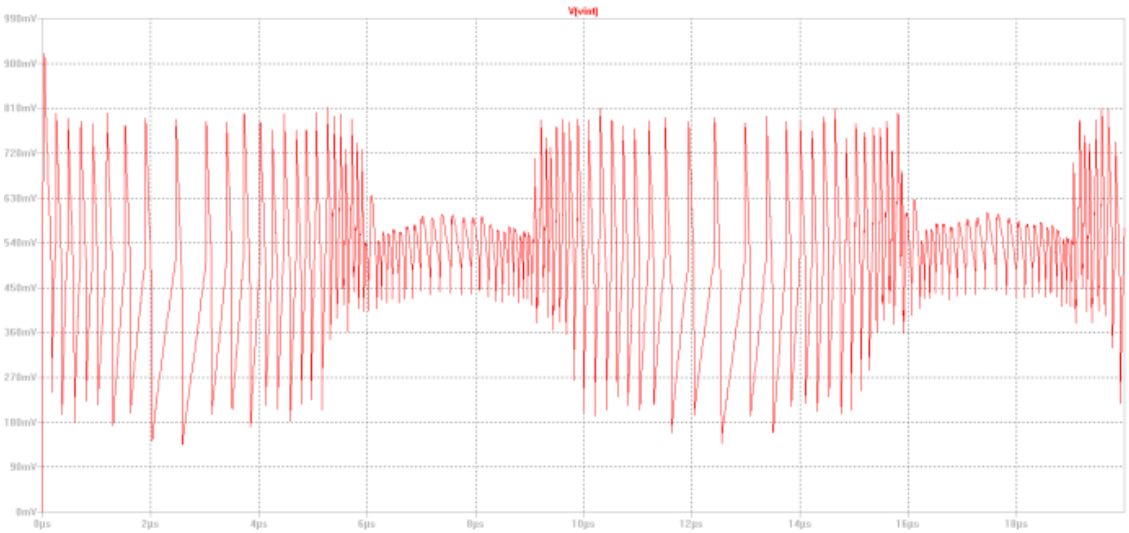


a. Plot Vin and DACout. How many levels and bits are in the digital output? Are they the same as in the ideal opamp simulation?



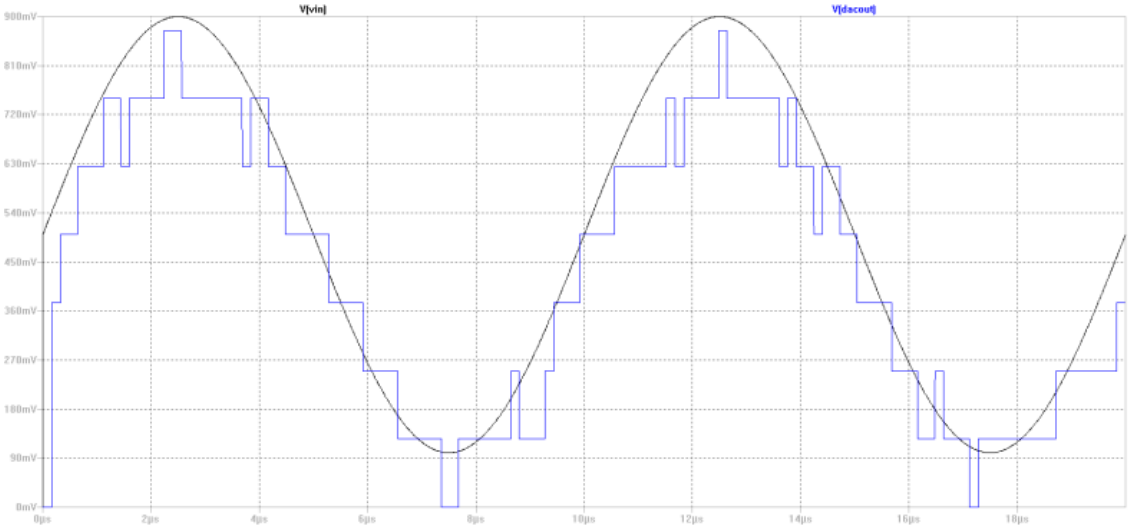
We still have 3bits but the dynamic of the signal looks quite different. The output does not encode the input properly.

b. Plot Vint. What is the Slew-Rate of signal Vint? Is there any difference with the ideal opamp simulation? Comment the results.



Now the SR is 5.7V/us which is limiting the encoding of a fast signal

3. Try now “opampmiller_v50nm_SR_100MHz.asc”

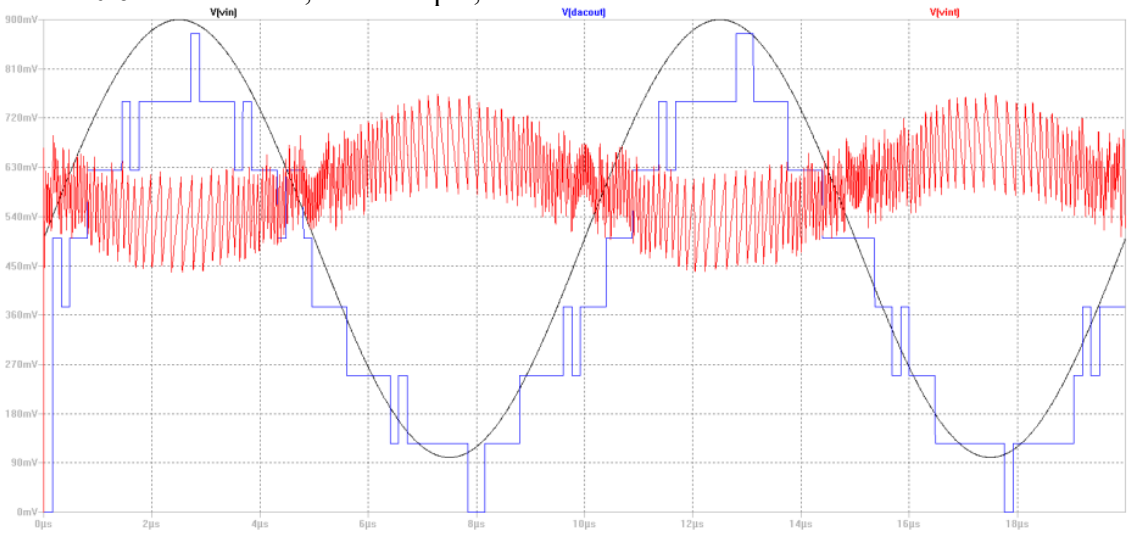


SR has been improved (SR=7.5V/us) and the output tracks the input.

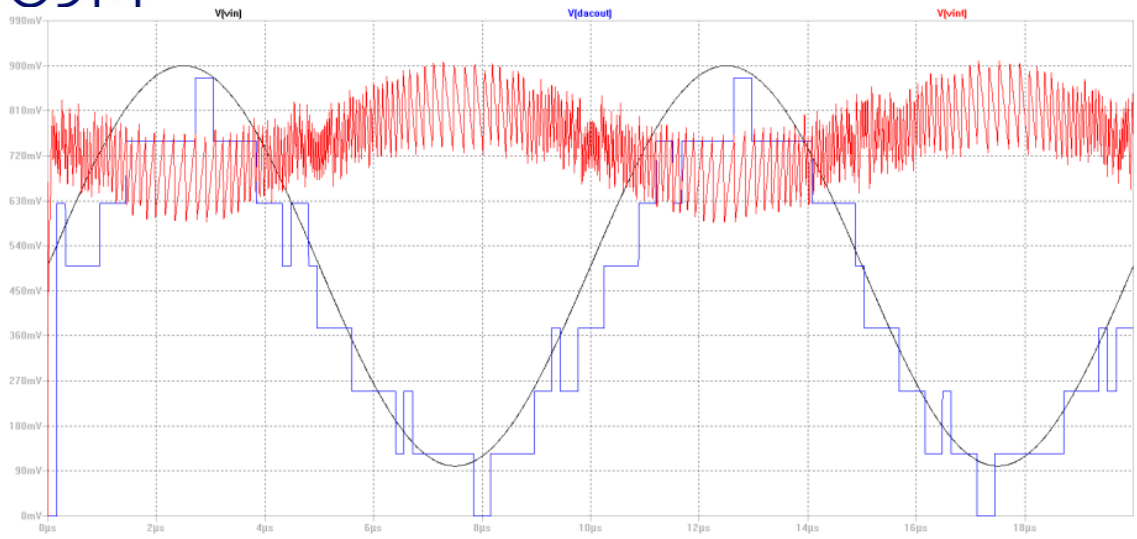
4. Introduce offset in the comparator and analyze the influence

The offset can be introduced changing the voltage value of VCM at the input of the comparator. As it can be seen in the next two figures, offset in the comparator does not change DACout, because it is compensated with the feedback loop, but it changes Vint signal, whose average value is proportional to VCM

VCM=0.6V. Black=Vin, Blue=output, Red=Vint



VCM=0.75V. Black=Vin, Blue=output, Red=Vint


V(vin)
V(dacout)
V(vint)
990mV
900mV
810mV
720mV
630mV
540mV
450mV
360mV
270mV
180mV
90mV
0mV
0µs
2µs
4µs
6µs
8µs
10µs
12µs
14µs
16µs
18µs