SIMULATION SESSION 2: DELTA-SIGMA ADC

SYSTEM-ON-CHIP AND EFFICIENT ELECTRONIC CIRCUIT INTEGRATION TECHNIQUES

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

Campus de Leganés

Avenida del Universidad 30

28911 Leganés

INTRODUCTION

In this session we will use the designed amplifier in a practical circuit. The chosen practical circuit is a First-Order Delta-Sigma Modulator ADC. It is an oversampled noise-shaped modulator composed of an active integrator, a latched comparator and single bit DAC (see Fig. 1).
It is recommended the reading of "The Delta-Sigma Modulator, Razavi, A circuit for all seasons (SSC Magazine)".

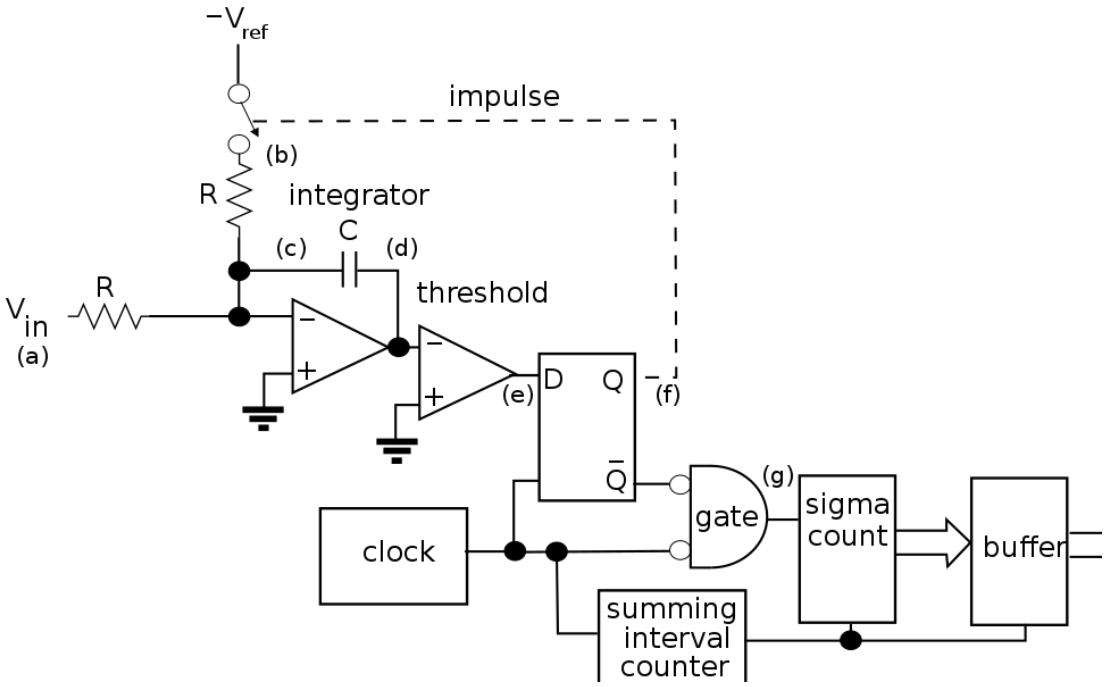

Fig. 1 First Order Delta-Sigma Moduator and Decimation Filter Example

1. Simulations

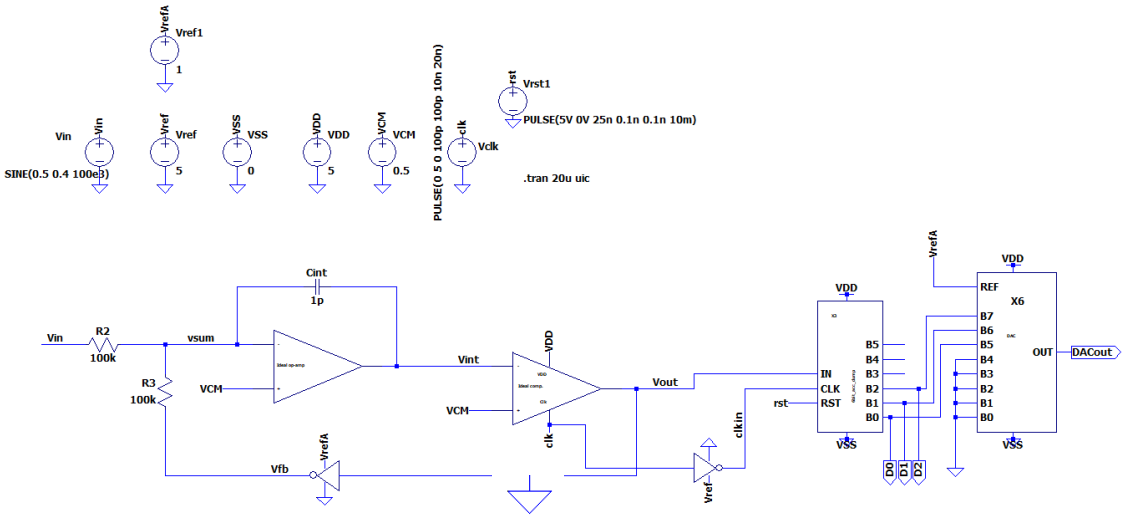

Fig. 3. Circuit to be simulated ("Ideal_DSM.asc")

Vout is the single-bit output of the Oversampled Delta-Sigma Circuit, D[2:0] is the decimated output (Decimation by 8), and DAC_out is a reconstructed analog version of D[2:0].

All the blocks are ideal.

1. Simulate circuit in Fig. 3.
    a. Plot Vin and DACout. How many levels and bits are in the digital output?
    b. Plot Vint. What is the Slew-Rate of signal Vint?
2. Replace the ideal opamp by the Miller opamp "opamp_poor_SR.asc" designed in a similar way as in previous session. Simulate circuit of figure 1 again with the real opamp.
    a. Plot Vin and DACout. How many levels and bits are in the digital output? Are they the same as in the ideal opamp simulation?
    b. Plot Vint. What is the Slew-Rate of signal Vint? Is there any difference with the ideal opamp simulation? Comment the results.
3. Try now "opampmiller_v50nm_SR_100MHz.asc"
4. Introduce offset in the comparator and analyze the influence.