

SIMULATION SESSION 3: VCO- BASED ADC

**SYSTEM-ON-CHIP AND EFFICIENT ELECTRONIC CIRCUIT
INTEGRATION TECHNIQUES**

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

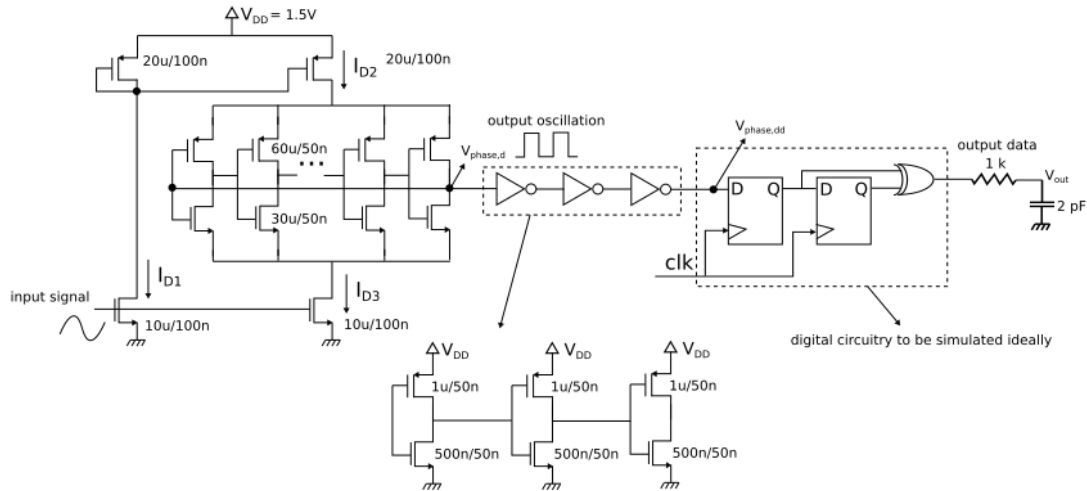
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Follow the next steps and, please, make a report with all the answers required.

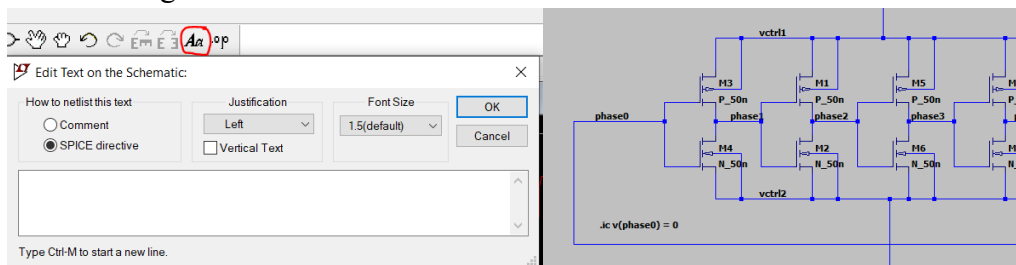
Today we will implement in LTSpice a VCO-based ADC with a current-starved ring-oscillator. The circuit to be implemented is depicted in the following figure:



1. Download the file vco_adc.asc from Aula Global. If you open it, you will see the models of transistors to be used (50-nm technology) and the digital circuitry implemented with ideal models. Implement the circuit shown above along with the indicates sizes for all the transistors. Add the signals required to make it work according to the following parameters:
 - a. Input signal: sinusoidal function with a DC component of 0.7 V and a frequency of 25 MHz. Keep the amplitude equal to zero.
 - b. Clock signal: square wave with an oscillation frequency of 2 GHz.
 - c. Connect the bulk of all the transistors in such a way that there is no body effect.

Finally, add a photo to the report of the complete implemented circuit.

2. Set a transient simulation of 0.5μs-length.
 - a. Does the oscillator work? If not, add an initial condition to LTSpice through a directive.



- b. Plot I_{D1} and I_{D2} . Do they have exactly the same value? Why? Justify your answer.

- c. Plot $V_{\text{phase,d}}$ and $V_{\text{phase,dd}}$. Looking at both signals, why do we need three inverters connected in cascade before sampling the signal?
 - d. What is the output frequency of the VCO?
3. Set a transient simulation of $2\mu\text{s}$ -length and include an amplitude of 150 mV for the input signal.
 - a. Plot V_{out} . Provide an explanation about what you are looking at.
 - b. Plot the FFT of V_{out} . Note: to do that once you have plotted V_{out} go to View/FFT. Keep the default settings. You should observe the input tone at 25 MHz and first-order noise shaping.
 - c. Is there any distortion? Justify your answer.
4. Set the input amplitude to 0 V again. Set a transient simulation of $0.2\mu\text{s}$ -length. Repeat the simulation for a DC input component of 0.55, 0.6, 0.65, 0.7, 0.75, 0.8 and 0.85 V; and calculate the oscillation frequency for each of the cases. Plot the oscillation frequency versus the DC input component. Do you get a linear relationship?
5. Set the DC input component to 0.7 V. Set a transient simulation of $0.2\mu\text{s}$ -length. Reduce the width (W) of the PMOS and the NMOS transistors of the oscillator to 30u and 15u, respectively. Is the oscillation frequency increased or decreased? Why do you get that behavior? Justify your answer.