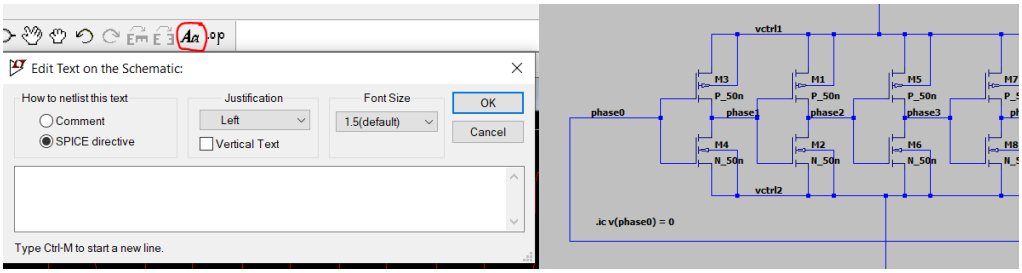
1. Download the file vco_adc.asc from Aula Global. If you open it, you will see the models of transistors to be used (50-nm technology) and the digital circuitry implemented with ideal models. Implement the circuit shown above along with the indicates sizes for all the transistors. Add the signals required to make it work according to the following parameters:
    a. Input signal: sinusoidal function with a DC component of 0.7 V and a frequency of 25 MHz. Keep the amplitude equal to cero.
    b. Clock signal: square wave with an oscillation frequency of 2 GHz.
    c. Connect the bulk of all the transistors in such a way that there is no body effect.

    Finally, add a photo to the report of the complete implemented circuit.

2. Set a transient simulation of 0.5µs-length.
    a. Does the oscillator work? If not, add an initial condition to LTSpice through a directive.



    b. Plot I_{D1} and I_{D2}. Do they have exactly the same value? Why? Justify your answer.

    Both have a current of approximately 1 mA. They must be equal because the current mirror has a size ratio of 1. Variations due to channel modulation.

    c. Plot $V_{phase,d}$ and $V_{phase,dd}$. Looking at both signals, why do we need three inverters connected in cascade before sampling the signal?

    Inverters needed to saturate the output signal.

    d. What is the output frequency of the VCO?

    Aprox. 850 MHz

3. Set a transient simulation of 2µs-length and include an amplitude of 150 mV for the input signal.
    a. Plot V_{out}. Provide an explanation about what you are looking at.

    V_{out} is a low-pass filtered signal with the input tone at low frequencies and the filtered modulation components.

    b. Plot the FFT of $V_{out.}$ Note: to do that once you have plotted V_{out} go to View/FFT. Keep the default settings. You should observe the input tone at 25 MHz and first-order noise shaping.
    c. Is there any distortion? Justify your answer.

    Distortion coming from the oscillator. Non-linear current to frequency conversion.

4. Set the input amplitude to 0 V again. Set a transient simulation of 0.2µs-length. Repeat the simulation for a DC input component of 0.55, 0.6, 0.65, 0.7, 0.75, 0.8 and 0.85 V; and calculate the oscillation frequency for each of the cases. Plot the oscillation frequency versus the DC input component. Do you get a linear relationship?

    There is no linear relation.

5. Set the DC input component to 0.7 V. Set a transient simulation of 0.2µs-length. Reduce the width (W) of the PMOS and the NMOS transistors of the oscillator to 30u and 15u, respectively. Is the oscillation frequency increased or decreased? Why do you get that behavior? Justify your answer.

    The oscillator frequency increases due to the decreased input capacitance in the taps of the oscillator.